Micro-Transfer Printing for cm-scale Heterogeneous Integration of Lithium Niobate

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For decades, photonic integrated circuits have been designed for CMOS-compatible platforms, such as silicon (Si) or silicon nitride (SiN). CMOS-compatibility allows for low loss, smooth integration with electronic components and manufacturing in existing foundries. Although these platforms can accommodate passive structures very well, they lack some interesting features like higher order non-linearity or gain. To add these features, other materials can be heterogeneously integrated into the CMOS-compatible platforms.

Reliable micro-transfer printing techniques to integrate non-linear materials on CMOS-compatible platforms have been demonstrated before. However, we demonstrate a process to enable the printing of cm-scale devices to allow for enhanced modulation efficiency.

Introduction

Throughout the history, photonic integrated circuits have been designed for many different platforms. The CMOS-compatible platforms, such as silicon (Si) or silicon nitride (SiN), have in the meantime grown to mature platforms using existing CMOS-technology. CMOS-compatibility allows for the smooth integration with electronic components and manufacturing in existing foundries. They also show low loss in interesting bandwidths such as the telecom bandwidth at 1550 nm. Although these platforms can accommodate passive structures very well, they lack some critical components like intrinsic second-order nonlinearity, Pockels effects or second harmonic generation.

Other materials, like lithium niobate (LN), would be able to offer some of these features. LN-based devices can, among other nonlinear optical processes, for example enable wavelength conversion [1], frequency doubling [2], and parametric amplification [3]. However, one of the key motivations for the integration of LN on CMOS-compatible platforms is its strong electro-optic properties, enabling efficient high-speed modulation. By integrating LN modulators on CMOS-compatible platforms, it becomes possible to achieve high-speed and low-power optical modulation, enabling advanced optical communication systems, while still keeping the advantages that the CMOS compatibility offers.

Several integration techniques have been established before for other materials: flip-chip bonding, where a prefabricated device on chip is directly bonded to the target wafer; epitaxial growth, where a full layer of the device material is grown on the target wafer, after which the device is patterned; and die-to-wafer or wafer-to-wafer bonding, where the device material is first bonded on the target wafer, then the substrate is removed and the device is patterned.

An up-and-coming heterogeneous integration technique is a fusion of the flip-chip and die-to-wafer bonding techniques, named micro-transfer printing (µTP) [4]. Using this concept, a device is first created on a source wafer, after which this device can be released and pick-and-placed on the target wafer. Benefits to this approach are that many devices of the same material can be prepared on the same source wafer, independent from the circuit layout on the target wafer(s). Also, the devices could be inspected and even tested prior to the integration (known-good die concept). The processing line of the target wafer, moreover, will not be affected, nor contaminated by the added material as barely any post-processing is needed after integration. This technique, furthermore, doesn't limit itself to only one extra material or device. Many different devices can be integrated as an add-on to the platform, without influencing each other's production flow or functionality.

Since the back-end level integration of LN by µTP does not affect the processing of the CMOS-compatible target wafer, it offers opportunities for large-scale and cost-effective manufacturing by leveraging established CMOS foundries and fabrication techniques, whilst obtaining strong second order functionality on the chip. This scalability and cost-effectiveness are crucial for accelerating the adoption of LN integration in practical applications, making it accessible to a wider range of industries and applications.

Micro-transfer printing of cm-scale lithium niobate thin films

The use of micro-transfer printing for heterogeneous integration of LN has been reported before [5, 6, 7, 8]. Some of the earlier work has proven the ability to create resonators using this technique [6, 7]. Transfer printed LN enabling modulation of a SiN platform was also demonstrated in an earlier report [8]. However, the interaction length of these devices can still be elongated much more to allow for longer light-matter interaction length, enabling for instance lower driving voltages and therefore a lower power consumption. This lower power consumption may make the devices CMOS compatible, hence, easier to integrate with existing electronics.

To demonstrate the feasibility of the process, simple rectangular devices (also called coupons later on) were created on an LNOI chip (LN/SiO_2/Si) and subsequently transfer printed on a bare Si chip. This printing was conducted both on a Si chip with an additional adhesive layer of benzocyclobutene (BCB) and a bare Si chip (direct bonding Si/LN). The process flow is depicted in Figure 1.

First, the LN-layer itself is etched using reactive-ion etching (RIE) to create the LN device. For this etching, a hydrogenated amorphous silicon (a-Si:H) hard mask was deposited, patterned using UV lithography and dry etched using RIE. The oxide layer underneath is, thereafter, also patterned applying UV lithography followed by a dry etch. After that, a resist encapsulation is added which keeps the coupon suspended as well as protects the coupon during the printing process (Figure 1.a). The encapsulation must also be able to break easily at controlled points when picking up the coupon. The part of the encapsulation that is designed to break at a certain point and keeps the coupon suspended,

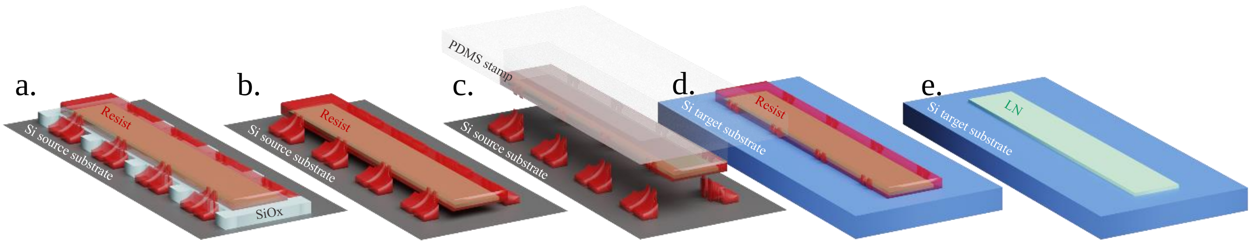

Figure 1: Process flow for printing of LN on a Si dummy sample

is called the tethers. As a last step in the creation of the device, the oxide is removed in an HF-based wet etch (Figure 1.b). The coupon is now suspended and after drying, it is ready to be picked up by an elastomeric PDMS stamp (Figure 1.c). After picking, the device can be printed on the target Si sample (Figure 1.d). To improve the adhesion between the coupon and the receiving sample, BCB can be used as an adhesive layer. Lastly, the resist encapsulation is removed (Figure 1.e) such that only the LN device is left. When using BCB as an adhesive layer, this is done through oxygen plasma based dry etching. When printing on a bare Si sample, however, the resist can be washed away with acetone, which tends to be better in terms of roughness of the coupon surface after printing.

Practical results and future work

The aforementioned processing steps are put into practice using a design of many 30µm wide coupons with different lengths, ranging from 1.5 mm to 1 cm. Some of the printing results are illustrated in Figure 2. After picking, the source chip looks clean, without any debris from the tethers breaking (Figure 2.d). Figure 2.d additionally shows all coupons were suspended well. Also on the target chip, a uniform print of 5 mm coupons on a bare Si sample (Figure 2.a) and 1 cm on a BCB cladded Si sample (Figure 2.c) are demonstrated. When removing the resist encapsulation (Figure 2.b), no traces of the resist are left. It should be noted that these results are obtained by heating the chuck under the target sample, which facilitates better adhesion.

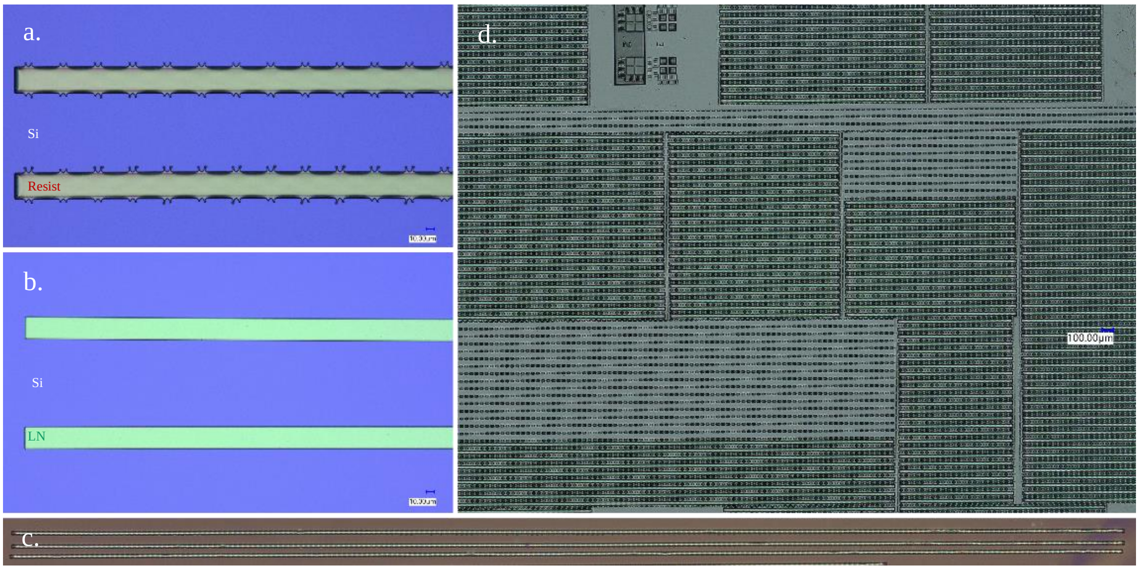

Figure 2: Practical results for µTP of LN on Si

These results are promising, but can still be optimised in the pursuit for scalable µTP. As the target chip had to be heated during transfer printing to allow for uniform printing, this process is not yet scalable: when printing multiple coupons at the same time (array printing) the target can not be heated as the PDMS stamp would expand and the pitch between the coupons would differ from the pitch the target wafer was designed for. The next goal is therefore to optimise the design of the encapsulation to be able to print without having to heat the target.

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