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ABSTRACT

We present our work in the European project MORPHIC to extend an established silicon photonics platform with low-power and non-volatile *micro-electromechanical* (MEMS) actuators to demonstrate large-scale programmable *photonic integrated circuits* (PICs).

Keywords: silicon photonics, MEMS, programmable photonics

1. INTRODUCTION

The application base for photonics has broadened with the recent progress in the field. Photonics is now used for a range of applications from optical communications to sensing.[1–4] Broadening of the applications base has resulted into the development of different material platforms such as group IV semiconductors (silicon and germanium),[5,6] compound III-V semiconductors (indium phosphide and gallium arsenide),[7,8] silica *planar lightwave circuits* (PLC),[9] silicon nitride (TriPlex is one of the available flavours),[10–12] different polymers,[13] and more exotic materials.[14,15] Out of these platforms, *silicon photonics* has emerged as one of the most promising technologies for *photonic integrated circuits* (PIC). A key selling point for silicon photonics is the high integration density due to the large index contrast between the light guiding silicon (the device layer) and the surrounding oxide (the cladding) of the *silicon-on-insulator* (SOI) wafers. The use of the already established *complementary metal oxide semiconductor* (CMOS) manufacturing infrastructure makes this platform industrially scalable.

Currently, rapid prototyping platforms are not available for photonics corresponding to the *field-programmable gate arrays* (FPGA) familiar from electronics. So, the standard platform is itself used for the fabrication of

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application specific chips in low volumes which makes it difficult to fully capitalize on the advantages of the CMOS infrastructure in terms of scaling and cost reduction. This highlights the need for rapid prototyping platforms to develop general purpose programmable photonic chips that can be configured using software and electronics to perform an application specific circuit for quick prototyping.

In this manuscript, we present the recent developments and progress from the MORPHIC project which focuses on realizing low-power programmable circuits using a commercially available silicon photonics platform enhanced with custom MEMS post processing.

2. TUNING ELEMENTS

Tuning elements like phase shifters and tunable power couplers along with other high performance components such as modulators and detectors are required to make programmable photonic circuits.[16–18] Different tunable components based on the thermal,[19–21] carrier-based,[22, 23] liquid crystal,[24–31] and Pockels effects[32, 33] have already been investigated. Among these, thermal based tuning mechanism is mostly used for silicon photonics. A general purpose programmable circuit can require up to thousands of tuners on a chip. It is a challenge to integrate tuners in large numbers, even for the commonly used thermal tuners, because thermal tuners consume significant power (5-30 mW), require sufficient spacing to avoid thermal cross-talk and are relatively slow with response time in the milliseconds. So, a more efficient (low power consumption, low insertion loss, small footprint) tuning mechanism is required that can be integrated directly with other functional building blocks of the silicon photonics platform.

In the MORPHIC project, we are enhancing an existing silicon photonics platform from IMEC, iSiPP50G,[34] with low power and non-volatile *micro-electromechanical system* (MEMS) tuners. In contrast to standard silicon photonics components, free-standing optical waveguides are required for MEMS tuning. So, a wafer-level post-processing flow is developed to selectively etch the *back-end-of-line* (BEOL) dielectric stack and the oxide underneath the optical waveguides using different masking and *hydrofluoric acid* (HF) etching steps.[35, 36] The sketches in Figure 1 show the state of the material stack before and after the post-processing.

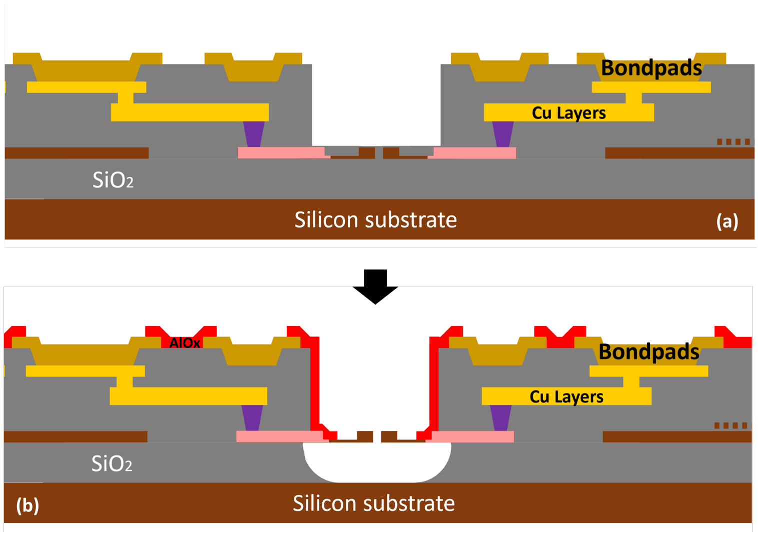

Figure 1. Cross-section of the iSiPP50G chip (a) before and (b) after the post-processing.

2.1 Tunable Coupler

It is important to distribute the light within a programmable circuit to realize connectivity of different components. Optical components like *directional couplers* (DC)[37–39] or *multi mode interferometers* (MMI)[40–43] are commonly used to distribute light within a circuit. The coupling ratios for these components are fixed so *Mach-Zehnder interferometers* (MZI) using heater based phase shifters are usually used in the circuits to attain tunable coupling.[44–46] This tunability comes at a cost of larger footprint and power consumption of several milliwatts. MEMS actuation can be used to tune directional couplers instead, with much smaller footprint and lower power consumption than heater-based tunable MZI circuits. We have demonstrated a very low-power MEMS based broadband 2×2 tunable directional coupler.[47] The gap between suspended waveguides in the evanescent coupling region is varied with comb-drive actuation to attain different coupling ratios. Our tunable coupler shows a broadband (> 35 nm) optical power coupling with an extinction ratio of 25 dB at the designed wavelength of $\lambda = 1550$ nm.

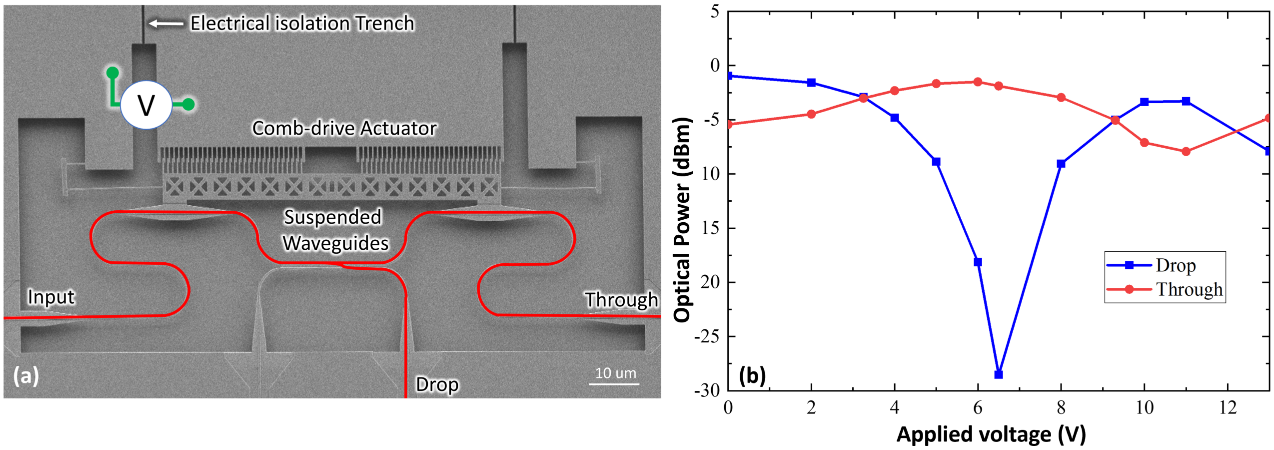

Figure 2. (a) Scanning electron microscope (SEM) picture of the MEMS based tunable coupler implemented on the standard silicon photonic platform iSiPP50G. Light paths within the coupler and other key parts are annotated. With application of a bias, the comb-drive actuates and changes the coupling gap between the waveguides. The change in gap changes the power split between the output ports. (b) Measured optical power from both drop and through ports for different applied actuation voltages.

2.2 Phase shifter

Generic programmable photonic circuits demand a control over both the power distribution and the phase. State-of-the-art phase shifters for silicon photonics are also heater-based, and consume several milliwatts of power and suffer from other issues related to the thermal cross-talk. MEMS actuation can also be used as a low-power substitute, by modifying the effective index of propagating modes in suspended waveguides via a change in geometry.[48–52] We have demonstrated low-power MEMS based phase shifters on our post-processed iSiPP50G silicon photonic platform, with low insertion loss and 2 µs response time.[53] A comb-drive is used for in-plane movement of a suspended narrow silicon beam as shown in Figure 3 (a). An attractive force between the H-shaped shuttle and the fixed anchored electrode of the comb-drive is generated on application of a bias voltage. This attractive force pulls away the narrow silicon beam from the waveguide resulting in tuning of the effective index of the guided mode inside the waveguide. Measured phase shift for different variations of the devices are shown in Figure 3 (b). Finally, we have also demonstrated a nonvolatile phase switch based on our phase shifter, where the phase can be set/reset between two stable states using adhesion forces and opposing comb-drive actuators.[54]

3. PROGRAMMABLE CIRCUITS USING MEMS COMPONENTS

We have designed both application specific and programmable circuits using the developed MEMS building blocks i.e. 2×2 tunable coupler and phase shifter. The designed application specific demonstrator circuits include beamforming, switching and microwave photonics circuits. These circuits would be used to benchmark the performance of the programmable circuits. For the programmable circuits, we have used both feed-forward and circulating topologies. The layout and schematic of the designed circulating mesh circuit is shown in Figure 4 below. The circuit is designed by arranging the optical gates consisting of a 2×2 tunable coupler and phase

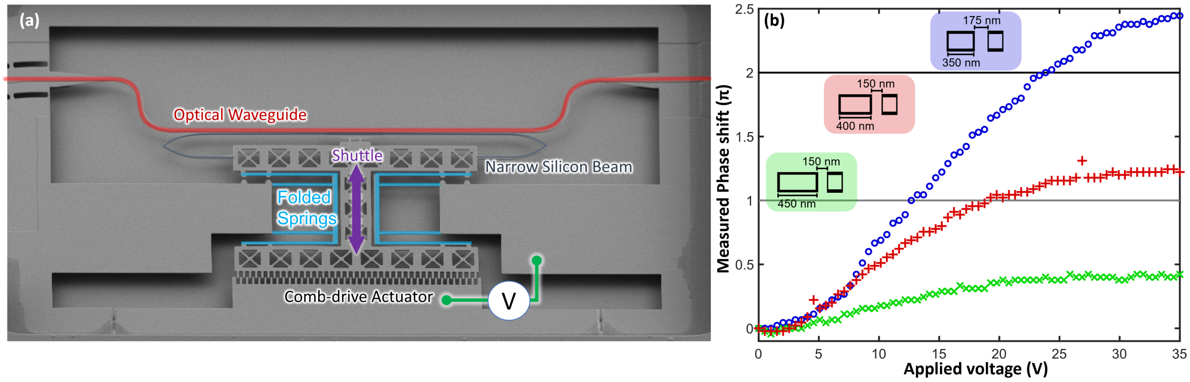

Figure 3. (a) Scanning electron microscope (SEM) image of the fabricated MEMS based phase shifter, implemented on a standard silicon photonic platform iSiPP50G. Light path within the phase shifter and other key parts are annotated. (b) Measured phase shift versus voltage for different variations of the waveguide cross-section.

shifters in hexagonal arrangement. This circuit is analogous to a *field-programmable gate array* (FPGA) in electronics. In some circuits, such as microwave filters, the combination of multiple discrete building blocks in a circulating mesh leads to long optical lengths, and thus limits the achievable Free Spectral Range (FSR). We have therefore also developed higher-level MEMS building blocks based on ring resonators, with much shorter optical length, that could be added as a modular extension to our generic mesh topology.[55] The use of a standard silicon photonics platform has enabled us to access other high-performance components like high-speed modulators, detectors and optical amplifiers in these circuits to perform (electro-)optical functions for different applications. Detectors are placed at different locations inside the hexagonal mesh to find out the current state of the gates.

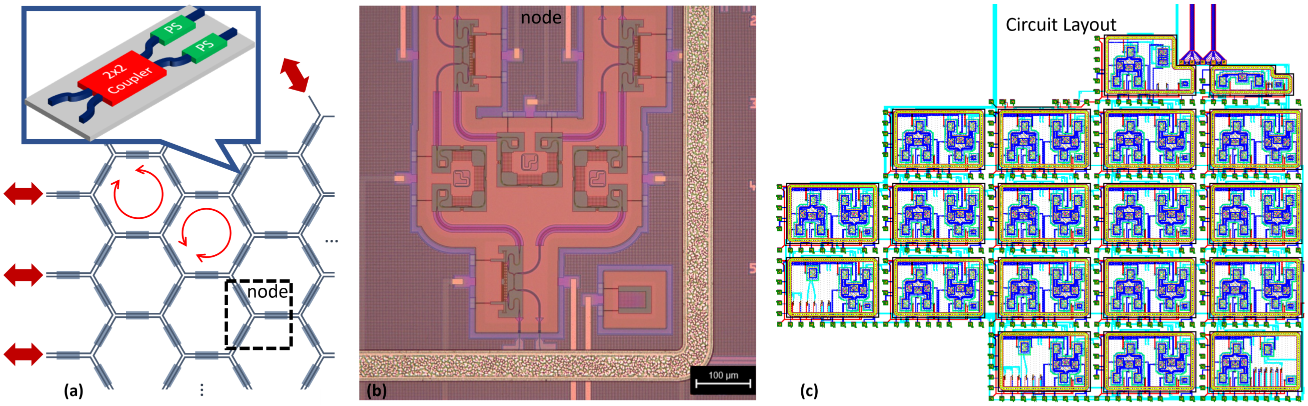

Figure 4. (a) Schematic of hexagonal mesh topology. The inset shows an optical gate consisting of a 2×2 tunable coupler and phase shifters. A node consisting of 3 optical gates is annotated. (b) Microscope image of a node consisting of three tunable couplers and three phase shifters. (c) Layout of the general purpose programmable circuit.

4. PACKAGING

A programmable circuit contains hundreds or even thousands of tuning elements with multiple optical ports. Our designed chips supports up to 3300 electrical connections on a regular bond pad grid pattern and two arrays of 72 fiber ports. Both optical and electrical interfaces from the circuits need to be accessible to the outside world for characterization of these programmable circuits. A packaging scheme is required for reliable operation of these circuits.

4.1 Sealing of the MEMS cavities

The optical waveguides inside the MEMS cavities are free-standing, making them susceptible to environmental influences. In order to protect the MEMS cavities from the environment, we have developed a wafer-level hermetic sealing process.[56,57] A thermo-compression bonding process in a wafer bonder is used to create a metal-to-metal bond between 2 µm thick Au/TiW layer on the sealing cap and the aluminum top layer on the silicon photonic device wafer. As the bonding process is carried out in a vacuum chamber, there is vacuum inside the hermetically sealed cavities.[58] A photograph of a fully processed 100mm wafer, a schematic cross-section and SEM recordings of a post-processed sealed chip are shown in Figure 5.

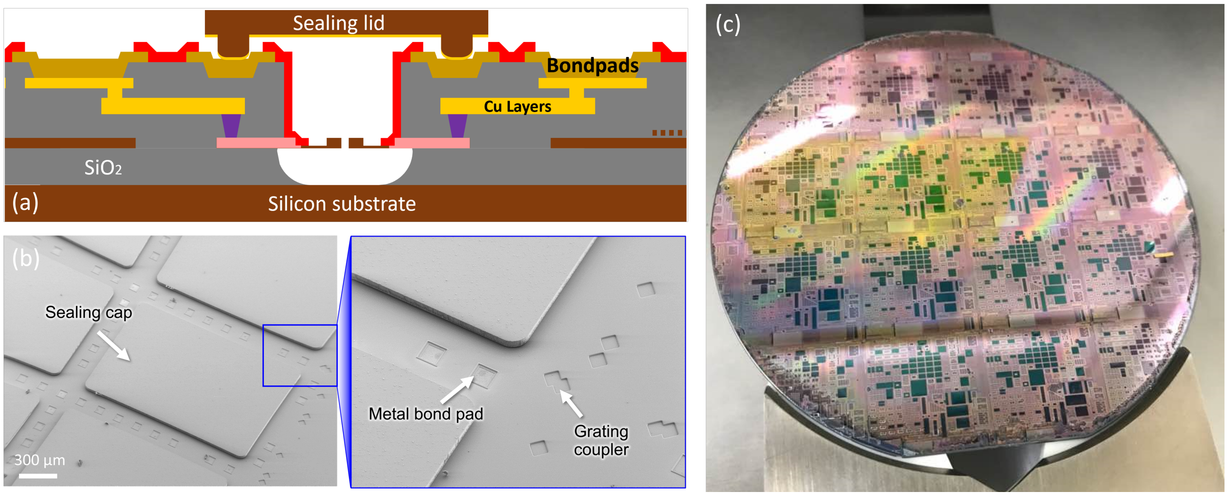

Figure 5. (a) A sketch showing the cross-section of a hermetically sealed post-processed chip. (b) Scanning electron microscope (SEM) picture showing the silicon sealing caps on top of the MEMS cavities. Grating coupler and metal bond pads are annotated to put things into perspective. (c) Picture of a post-processed hermetically sealed wafer.

4.2 Mini-demonstrator

In order to package only a few circuits on the chip, we have adopted a simple approach in which a single layer glass interposer is designed to fan-out the electrical connections from the chip to the edge of the interposer. Wire-bonds as shown in Figure 6 (c) are used from the edge of the interposer to the bond-pads on the *printed circuit board* (PCB) to make them accessible to the outside world. Additionally, a 72 channels fiber array is glued to one of the optical port arrays to facilitate the optical characterization of the circuits. Pictures after the flip-chip and fully packaged demonstrator are shown in Figure 6 (a) and (b) respectively.

4.3 Full-demonstrator

To package all the circuits from the chip, a packaging scheme using a high density state-of-the-art ceramic interposer is devised. Design rules concerning the position of the bond-pads, *trans-impedance amplifiers* (TIA),[59] modulators, high speed monitors and optical ports on the chip are defined as shown in Figure 7 (a). A hermetically sealed chip is flip-chipped onto a 22 layer ceramic interposer to fan-out all the available 3300 electrical connections including the high frequency connections. The ceramic interposer before and after the flip-chip is shown in Figure 7 (b) and (c), respectively. An interconnect PCB is used to fan out the pads from the interposer to the outside using connectors. As explained above, a 72 channels fiber array is glued to one of the optical ports arrays to facilitate the optical characterization of the circuits.

5. DRIVER ELECTRONICS AND FEEDBACK LOOPS

It is a challenge to actuate the tuners and read out the monitors in large numbers from a programmable circuit. We have opted for a modular approach for electrical read-out and actuation of these large programmable photonic

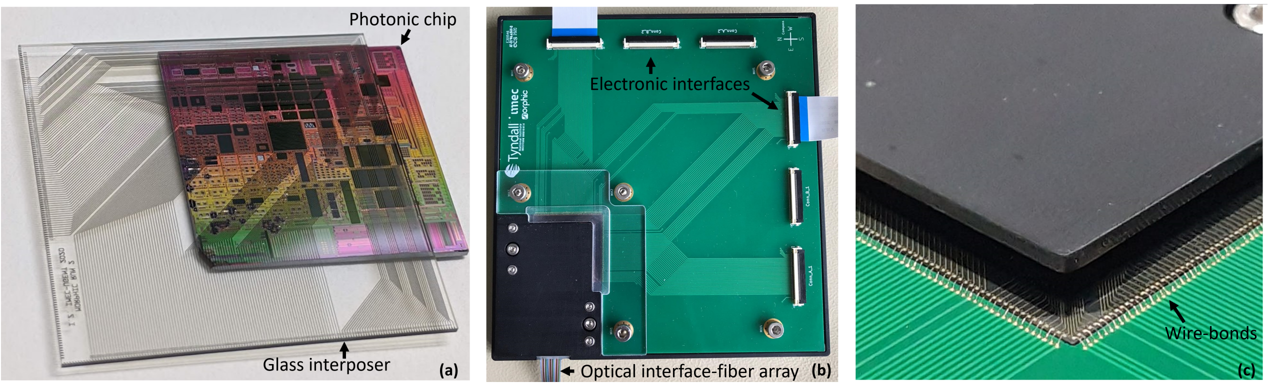

Figure 6. (a) Sealed photonic integrated chip flip-chipped onto a glass interposer. The interposer is used to fan-out the electrical connections from the photonic chip to the edge of the interposer. (b) Picture of the packaged mini-demonstrator. Optical and electrical interfaces are annotated. (c) The wire-bonds from the pads at the edge of the glass interposer to the pads on the printed circuits board.

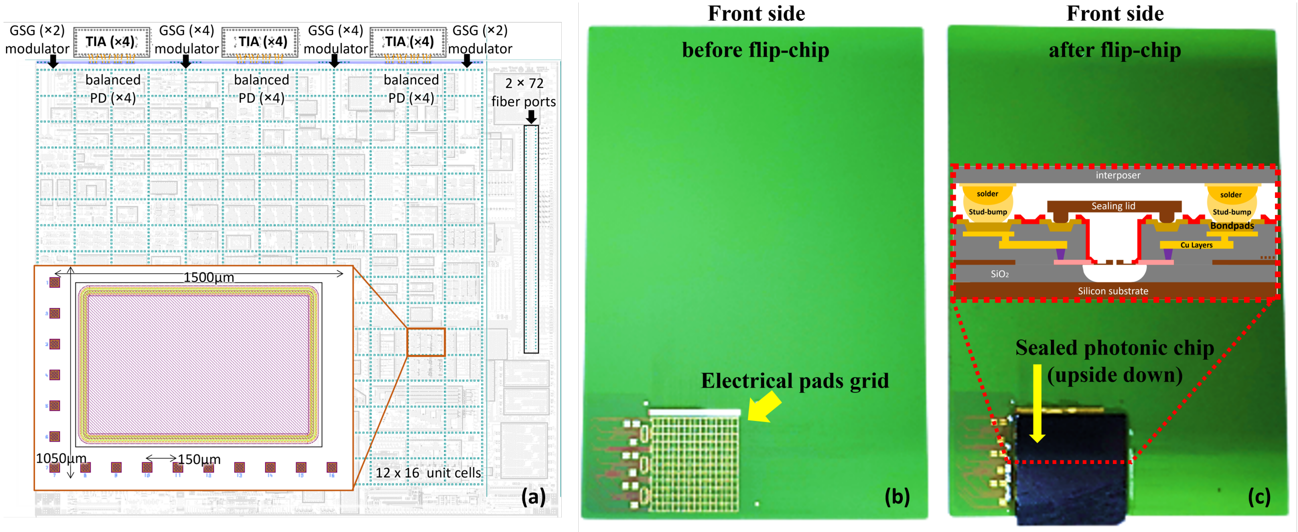

Figure 7. (a) Electrical pad grid on the photonic chip. Positions of the trans-impedance amplifiers, modulators, balanced photo-diodes and the fiber ports are annotated. Pictures of the high density ceramic interposer (b) before and (c) after the flip-chip of the sealed photonic chip. The inset shows the cross-section of a post-processed sealed chip flip-chipped on to the interposer.

circuits. Electronic interfacing cards (EIC) capable of actuating 64 MEMS tuners and reading-out 32 monitors are designed. Different boards can be combined to drive a large circuit. Our general purpose programmable circuit requires up to 12 EIC boards for full configuration. It is almost impossible to manually configure such a big circuit so we have developed a software framework to automatically implement different application circuits on these circuits using the EIC boards.

6. SUMMARY

This paper reports the progress of the MORPHIC project on MEMS based tunable components, low-power programmable circuits, packaging, driver electronics, and the software framework developed for design and configuration of the programmable circuits.

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