Micro-Transfer-Printed III-V-on-Silicon C-Band Semiconductor Optical Amplifiers

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The micro-transfer-printing of prefabricated C-band semiconductor optical amplifiers (SOAs) on a silicon waveguide circuit is reported. The SOAs are 1.35 mm in length and 40 µm in width. Dense arrays of III-V SOAs are fabricated on the source InP wafer. These can then be micro-transfer-printed on the target SOI photonic circuits in a massively parallel fashion. Additionally, this approach allows for greater flexibility in terms of integrating different epitaxial layer structures on the same SOI waveguide circuit. The technique allows integrating SOAs on a complex silicon photonic circuit platform without changing the foundry process-flow. Two different SOA designs with different optical confinement factor in the quantum wells of the III-V waveguide are discussed. This allows tuning the small-signal gain and output saturation power of the SOA. The design with higher optical confinement in the quantum wells has a small-signal gain of up to 23 dB and an on-chip saturation power of 9.2 mW at 140 mA bias current and the lower optical confinement factor design has a small-signal gain of 17 dB and power saturation of 15 mW at 160 mA of bias current.

1. Introduction

Photonic integrated circuits (PICs) have become a commercial reality in a number of markets, especially in telecom and datacom.[1] PICs enable complex optical and opto-electronic functions on a very compact footprint with high reliability.[2–4] And because of wafer-scale manufacturing, the cost of a PIC can be significantly lower than with conventional technologies (relying on bulk optical or other assembly platforms) for the same function. Silicon photonics is the field that takes advantage of more than 50 years of massive investment in silicon technology for electronic ICs. It leverages the vast know-how of the CMOS world to develop PICs in the technologies of existing CMOS fabs.[5] It is a relatively young field: research activities geared up less than 20 years ago and widespread industrial interest less than 10 years ago. Nevertheless, the field of silicon photonics has been growing at an amazing rate, both scientifically and industrially.[6–8] Today more than 15 CMOS fabs (industrial fabs or semi-industrial R&D fabs) around the world have developed a mature process flow for silicon photonics.[5] Some of them manufacture products that are competitive in the market today.[7,8]

While state-of-the-art silicon photonic integration platforms are being developed by various companies and research institutes, having integrated light sources at wafer level is still a stumble block. This limits the functionalities that can be implemented on a single chip. However, several approaches for wafer-level light source integration are being pursued, each with their own advantages and drawbacks, and with different technology readiness levels (TRL). There is a consensus that monolithically integrated Group IV lasers are still far from being practical, and that III-V semiconductor materials and devices are needed. Currently, the method that has the highest maturity-pioneered by Luxtera-is the use of a micro-packaged laser (coined a LaMP), comprising a III-V laser diode on a micro-optical bench with a ball lens, isolator and mirror to focus the light on a grating coupler on the Si PIC.[9] While this approach has several advantages (mature InP technology, wafer-level assembly, packaging, test and burn-in), the complexity of the LaMP itself and its sequential active alignment on the silicon photonic wafer make it an expensive solution. Moreover, the use of a grating coupler as an optical interfacing limits the coupling efficiency and bandwidth. Also, waveguide-in/waveguide-out components such as semiconductor optical amplifiers (SOAs) are quite difficult to realize this way, and these are key components in advanced PICs. Therefore, more intimate integration approaches are being pursued, ranging from flip-chip integration of III-V optoelectronic devices over III-V die-to-wafer/wafer-to-wafer bonding to hetero-epitaxial growth. Front-end hetero-epitaxial growth of III-V semiconductors represents the ultimate path to integrate light sources on silicon photonics and proof-of-concept devices have been demonstrated,[10] but many technological hurdles need to

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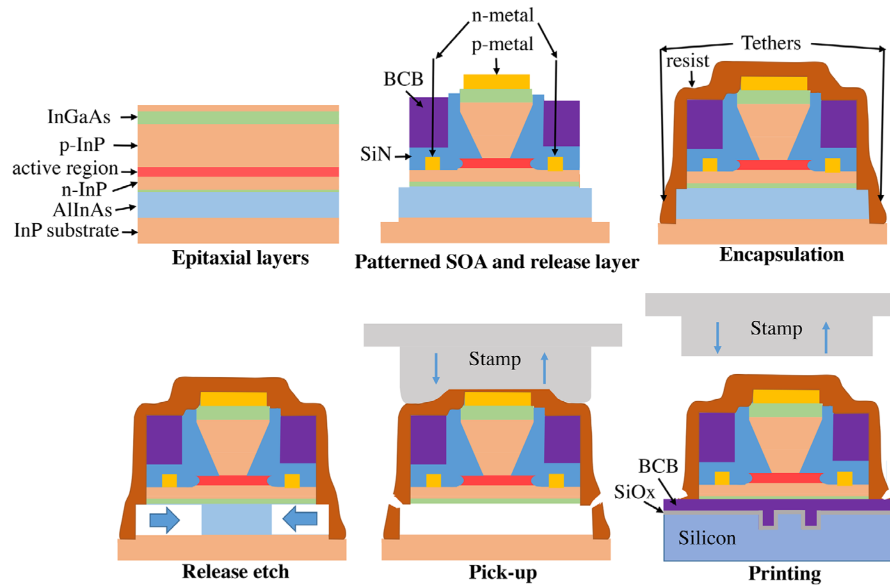

Figure 1. The micro-transfer printing process flow for SOA integration includes patterning of the device functional layers on the InP substrate, encapsulation of the device layers and the formation of the tethers to hold the device layers during the release etch and a selective release etch. Finally, the released devices are picked with an elastomer stamp and printed on the target site on an SOI wafer.

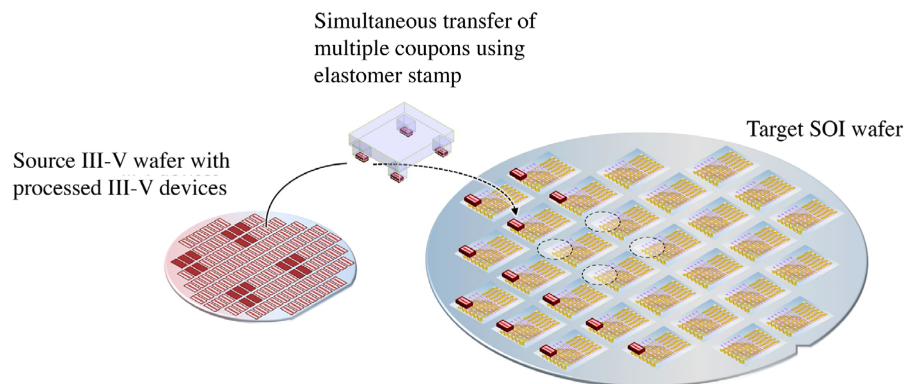

Figure 2. Concept of wafer-scale parallel printing of processed III-V devices to a target SOI wafer using a multiple post elastomer stamp.

be overcome before this becomes a viable technology. In the case of flip-chip integration mature III-V technology can be used and with efficient optical coupling devices such as semiconductor optical amplifiers (SOAs) can be realized. Testing the devices on the source wafer prior to integration is possible, but the sequential assembly (using active or passive alignment) can be a bottleneck and double-sided coupling is difficult for III-V chips with a cleaving tolerance of several micrometer.

The die-to-wafer bonding approach has the advantage of high throughput integration: with die-to-wafer bonding unstructured III-V dies are bonded epi-side down to a silicon photonic wafer. The unpatterned wafers do not need accurate alignment, making this a low-cost approach. After bonding and III-V substrate removal the III-V epitaxial layers can be processed on wafer-scale, lithographically aligned to the underlying silicon (Si) waveguides, thus removing the need for active alignment. While this enables dense integration of efficient light sources and optical amplifiers, the silicon photonics back-end flow needs to be modified for the III-V integration.[11–13] Therefore, there is a need for an alternative approach that combines the advantages of flip-chip integration (processing of III-V devices on the III-V source wafer, pre-testing) and die-to-wafer bonding (high throughput integration, straightforward integration of waveguide-in/waveguide-out devices such as SOAs). In this paper, we present the use of micro-transfer-printing for the integration of pre-processed III-V semiconductor optical amplifiers on a silicon photonic integrated circuit.

2. Micro-Transfer-Printing Technology

The concept of micro-transfer-printing (μTP) is illustrated in **Figures 1** and **2**. μTP combines advantages of flip-chip integration and wafer bonding. The process starts with the definition of the III-V opto-electronic components (SOAs, lasers) on a III-V source wafer, which has the active epitaxial layer stack grown

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Table 1. III-V SOA epitaxial layer stack.

Layer	Layer type	Material	Thickness [nm]	Doping level [cm^{-3}]	Dopant
27	Cap layer	InP	100	nid	
26	Contact P	InGaAs(lattice matched)	100	$> 1 \times 10^{19}$	Zn/C
25	Contact P	InGaAs (lattice matched)	100	$\approx 1 \times 10^{19}$	Zn
24	Cladding P	InP	1000	$\approx 1 \times 10^{18}$	Zn
23	Cladding P	InP	500	$\approx 5 \times 10^{17}$	Zn
22	etch stop	InGaAsP (λ_g = 1.17 µm)	25	$\approx 5 \times 10^{17}$	Zn
21	Transition	$(Al_{0.9}Ga_{0.1})_{0.47}In_{0.53}As$	40		
20	SCH	$(Al_{0.7}Ga_{0.3})_{0.47}In_{0.53}As$	75		
9x6	barrier	$(Al_{0.45}Ga_{0.65})_{0.51}In_{0.49}As$	10		
8x6	well	$(Al_{0.25}Ga_{0.75})_{0.3}In_{0.7}As$	7.5		
7	barrier	$(Al_{0.45}Ga_{0.65})_{0.51}In_{0.49}As$	6		
6	SCH	$(Al_{0.7}Ga_{0.3})_{0.47}In_{0.53}As$	75		
5	Transition	$(Al_{0.9}Ga_{0.1})_{0.47}In_{0.53}As$	40	1×10^{18}	Si
4	Cladding N	InP	200	2×10^{18}	Si
3	Cladding N	InP	60	nid	
2	Sacrifical	InGaAs (lattice matched)	50	nid	
1	Sacrifical	AlInAs (lattice matched)	500	$\approx 0.5 \times 10^{18}$	Si
0	Buffer layer	InP	150		

on top of a release layer (for example, InGaAs or InAlAs for the InP material system). After patterning of the device and the release layer, the structures are encapsulated and the release layer is selectively removed using $FeCl_3$:H_2O (1 g per 2 mL) wet etching, leaving the III-V components attached to the III-V substrate by 3.0–3.5 µm thin tethers. With a polydimethylsiloxane (PDMS) stamp, one or more thin-film III-V components can be picked up from the source wafer and printed on an SOI target wafer. Then, the encapsulation is removed with a dry etching process and the III-V devices are electrically contacted on wafer level. This approach enables pretesting of the III-V devices on the source wafer, similar to flip-chip integration, but also massively parallel integration, similar to the die-to-wafer bonding approach. The III-V devices are micro-scale, so the Si photonics back-end flow is not disturbed. Only a local opening to the Si device layer is needed, similar to the flip-chip integration approach. The III-V material is also used in a very efficient way. Because micro-scale devices are transfer printed, different III-V devices can be intimately integrated together on a single PIC. While originally pursued for applications other than integrated circuits, in recent years the technique has gained attention for heterogeneous PICs.[14] The transfer printing process flow for the SOA is illustrated in more detail in Figure 1.

The bonding of the SOA coupons to the SOI target wafer can be realized using molecular bonding or using an adhesive bonding agent.[15] In this paper, a DVS-BCB adhesive bonding layer is used. Commercial state-of-the-art micro-transfer-printing tools provide an alignment accuracy of (3σ) of ±1.5 µm. A better alignment accuracy of less than 1 µm is possible in the case of individual coupons as opposed to the array printing. In most of the III-V waveguide-coupled opto-electronic devices integrated on the Si waveguide circuits adiabatic taper structures are used to couple light between the III-V waveguide and the Si waveguide.[16] The micron-scale accuracy of the transfer printing tool imposes a limit on the alignment tolerance of the adiabatic taper structure.[17]

In this work, we demonstrate the first III-V-on-Si SOAs integrated through micro-transfer-printing. We discuss two distinct SOA designs with different confinement factor in the multiple-quantum well stack (MQW). We discuss the design of the adiabatic taper structure to have sufficient alignment tolerance in both cases. We also discuss the fabrication process including patterning of the SOA on the InP substrate, release, micro-transfer-printing and post-processing. We report on the performance of the SOAs and discuss the future prospects. This work substantiates the micro-transfer-printing technique for heterogeneous integration of III-V devices on Si photonics platforms enabling the creation of more complex and powerful chip-scale photonic systems.

3. Design of the III-V-on-Si SOA

The III-V epitaxial layer structure used to simulate, design, and fabricate the SOAs is described in **Table 1** and is also illustrated in Figure 1. The SOA epitaxial stack has a 200 nm highly doped p-InGaAs contact layer, a 1.5 µm p-InP cladding, a 25 nm etch stop InGaAsP layer, a pair of 40 nm AlGaInAs transition layers separating InP from SCH layers, a pair of 75 nm AlGaInAs SCH layers, an active region with 6 AlGaInAs QWs sandwiched between AlGaInAs barrier layers, a 200 nm n-InP contact layer with 60 nm intrinsic InP layer underneath and a 50 /500 nm InGaAs/AlInAs release layer grown on the InP substrate.[15]

As discussed in the previous section, we report two III-V-on-Si SOA designs that have different Si waveguide width in the gain section of the SOA. This allows to vary the confinement of the optical mode in the quantum wells and hence tune the small-signal gain and output saturation power. The Si waveguide layer

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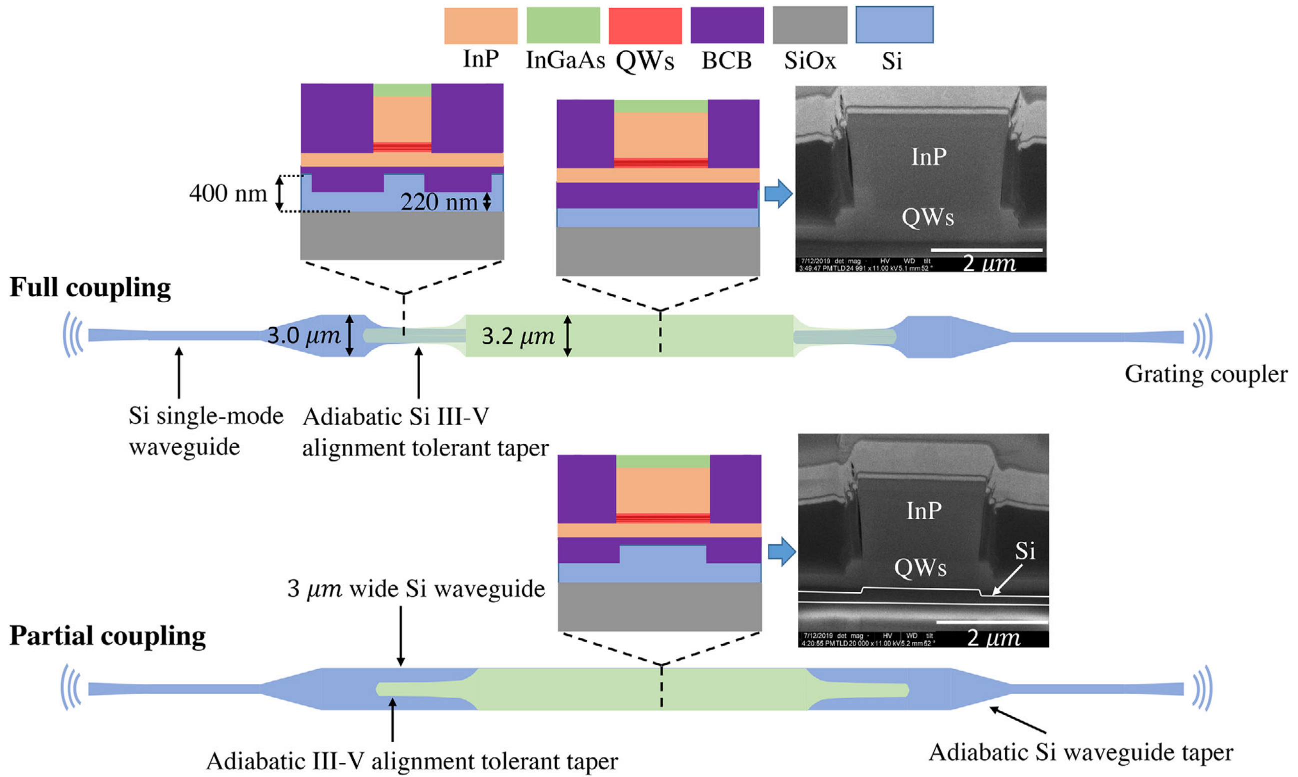

Figure 3. Schematics and FIB cross sections illustrating the design of the full-coupling and partial-coupling III-V-on-Si SOAs.

is 400 nm thick and has an 180 nm etch depth. The buried oxide (BOX) layer is 2 µm thick underneath the Si waveguide layer. Both SOA designs, full-coupling (higher optical confinement in the QWs) and partial coupling (lower optical confinement in the QWs), are illustrated in **Figure 3**. In the full-coupling case, the light couples from the Si waveguide to the III-V waveguide using an alignment tolerant Si/III-V adiabatic taper structure (discussed in the next section) and there is no Si waveguide underneath the III-V active region as shown by the cross sections. In contrast, the partial coupling design uses the same adiabatic III-V alignment tolerant taper to partially couple the light from the Si waveguide to the III-V/Si waveguide section of the SOA. A focussed ion beam (FIB) cross section in the gain section of the SOA for both types is also shown in Figure 3.

We are using the same III-V SOA device (coupon) on two different Si waveguide designs (based on full coupling and partial coupling to the III-V device layer). This tunes the confinement factor in the active region of the SOA. In the full-coupling SOA design, there is no Si waveguide underneath the III-V waveguide gain section and light fully couples into the III-V waveguide. The partial-coupling design has a 3-µm wide Si waveguide underneath and light is only partially coupled to the III-V active region of the SOA. The taper is designed (discussed in detail in the next section) to overcome the coupling losses due to the lateral misalignment, inherent to the transfer printing tool, between the prefabricated III-V SOA and the Si waveguide. Outside the III-V/Si SOA, the wide Si waveguide is adiabatically tapered to a single mode waveguide. Focusing grating couplers are used for fiber interfacing on both sides of the SOA.

4. Alignment-Tolerant Taper Design

The adiabatic taper is designed using the formalism discussed in ref. [18]. It is given that an adiabatic taper designed to follow Equation (1) can transform the mode from one waveguide into the other waveguide with a lost power fraction less than ϵ.

$$\gamma = \tan\left[\arcsin\left(2\epsilon^{\frac{1}{2}}\int_{z_0}^{z}\kappa(z')dz'\right)\right] \tag{1}$$

where $\gamma \equiv \frac{\beta_2-\beta_1}{2\kappa}$, $\beta_2 - \beta_1$ is the propagation constant mismatch between the individual uncoupled waveguide modes, ϵ is the fraction of power in the unwanted mode, z are the points along the length of the taper and $z = z_0$ is the phase matching point, κ is the coupling strength between the two waveguide modes and is defined as

$$\begin{aligned}
\kappa_{mp} &= \frac{k_0^2}{2\beta}\int\int_{-\infty}^{+\infty}(n'^2 - n_p^2)F_m F_p^* dxdy \\
\kappa_{pm} &= \frac{k_0^2}{2\beta}\int\int_{-\infty}^{+\infty}(n'^2 - n_m^2)F_p F_m^* dxdy \\
\kappa &= \sqrt{\kappa_{mp}\kappa_{pm}}
\end{aligned} \tag{2}$$

where F_m and F_p are the normalized eigenmodes of each uncoupled waveguide and must be normalized such that $\int\int_{-\infty}^{+\infty}|F_m(x,y)|^2dxdy = 1$, where n' is the refractive index profile of the coupled waveguide system, n_p and n_m are the refractive

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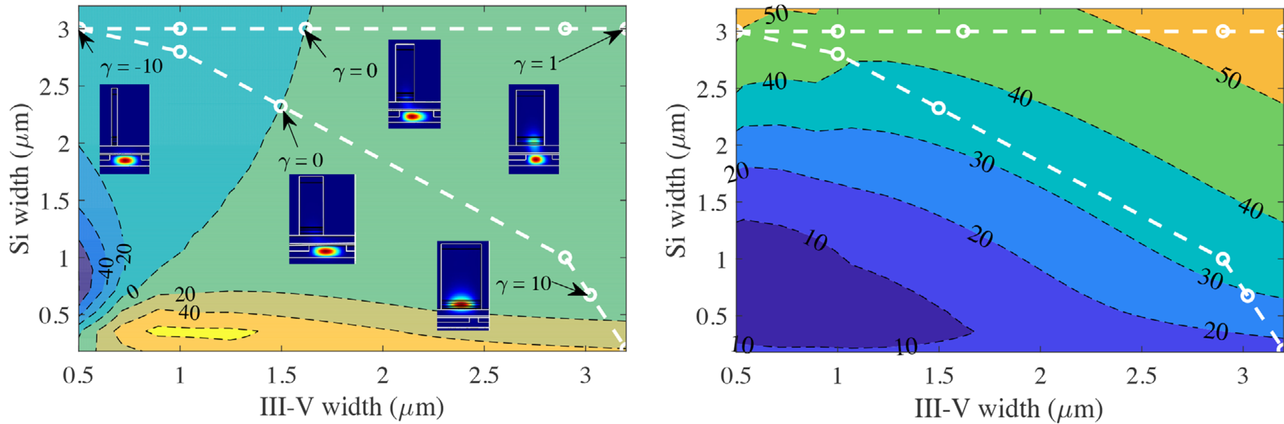

Figure 4. (Left) Calculated map of γ for several width combinations of the III-V and Si waveguide. The white dashed lines represent the trajectory of the points chosen to design the adiabatic tapers. The insets are the optical modal profiles found using simulations at $\gamma = -10$ (the optical mode is mostly confined in Si waveguide), $\gamma = 0$ (this is the phase matching point at which the coupling takes place), $\gamma = 1$ (the optical mode is distributed unevenly in both Si and III-V waveguide, and $\gamma = 10$ (the optical mode is confined in the III-V waveguide), (Right) Calculated map of κ in mm^{-1} for several width combinations of the III-V and Si waveguide.

index profiles of the uncoupled waveguides, k_0 is the free-space propagation constant and β is the propagation constant of the coupled mode. Equation (1) gives the γ distribution along the length of the III-V and Si adiabatic taper structure, assumed to be along the z-axis. Subsequently, it can be rewritten by assuming κ to be linearly varying between two consecutive points along z and making z as the subject of the expression

$$z_N = \frac{\sin(\arctan(\gamma_N))}{\epsilon^{\frac{1}{2}}(\kappa_{N-1} + \kappa_N)} - \frac{2}{\kappa_{N-1} + \kappa_N} \sum_{i=0}^{N-1} A_i + z_{N-1} \tag{3}$$

where $z = z_N$ is a point N along the length of the taper, $A_i = \frac{1}{2}(\kappa_{i-1} + \kappa_i)(z_i - z_{i-1})$ and γ_N is the value of γ at $z = z_N$. Equation (3) gives the location z along the length of the taper for a given set of κ and γ value which are related to the width of III-V and Si waveguides in a coupled waveguide system.

In order to design the taper structure a map of κ and γ is calculated, using the Lumerical Mode waveguide simulator,[19] for all possible width combinations of III-V and Si waveguide, assuming a lateral misalignment of 1 µm as the worst case. A DVS-BCB bonding layer thickness of 60 nm is assumed in the simulation. Equation (2) together with the eigenmode solver is used to calculate κ. Similarly, the γ and β values are also computed with the eigenmode solver. The maps of κ and γ for various III-V waveguide and Si waveguide widths are illustrated in **Figure 4**. To completely transform an optical mode confined in the Si waveguide to an optical mode confined in the III-V waveguide, γ should follow a trajectory from negative to positive values crossing the zero line on the map. The zero line indicates the III-V and Si width combinations at which the optical modes in both waveguides are phase matched. It can be seen from the optical mode profiles in the inset of the Figure 4, when $\gamma = -10$ that the light is confined in the Si waveguide. Alternatively, when $\gamma = 10$ the optical mode is confined in the III-V waveguide. The two different trajectories chosen to design the III-V and Si adiabatic taper (for full coupling and partial coupling) are shown with a white dashed line on the γ map in Figure 4.

In one of the two trajectories, (full-coupling with higher confinement factor) γ varies from −10 to 40 and the optical mode is completely transformed from the Si waveguide to the III-V waveguide and vice versa. The next step in designing the adiabatic taper is to insert the chosen values of the γ and κ trajectory into Equation (3). This will give us their corresponding z location along the length of the adiabatic taper, hence, defining the taper geometry. The value of ϵ is set to be 0.02 and 0.01 for the calculation of taper geometry in the case of full coupling design and partial coupling design, respectively. The smaller value of ϵ results in longer adiabatic taper length. However, the adiabatic Si and III-V taper should follow one more criterion to avoid power coupling into higher order modes. The local half angle of the Si and III-V taper must satisfy $\theta < \frac{\lambda_0}{2Wn_{eff}}$.[20] This means that the tapering should be slower than the diffraction of the fundamental mode of each waveguide. The taper geometry calculated from Equation (3) violates this criterion at the end of the taper, where the variation of κ along z is rapid and the mode is mostly confined in the III-V waveguide. Therefore, the values of z at the end of III-V and Si adiabatic taper waveguides are adjusted to follow the aforementioned formula. This slows down the tapering and thus prevents the transformation of fundamental mode into the higher order mode. The shape of the adiabatic tapers is shown in **Figure 5** (left). The blue curve and the left vertical axis represents the III-V adiabatic taper for both designs. The initial width of the III-V adiabatic tapers is 0.5 µm and the final width is 3.2 µm. The length of partial coupling and full coupling adiabatic tapers are 210 µm and 225 µm, respectively. The partial coupling taper is shorter because of the higher κ values when the Si waveguide is 3.0 µm wide. However, to simplify the fabrication and development, full coupling adiabatic taper design is used for both SOAs and only the Si waveguide is adapted. In the full-coupling design, the Si adiabatic waveguide taper narrows down from 3 to 0.2 µm over 225 µm length and for the partial coupling SOA, it is a constant width 3.0 µm waveguide, shown in red curve and on the right vertical axis. The final taper structures are then exported into the Lumerical 3D-EME solver[19] and the

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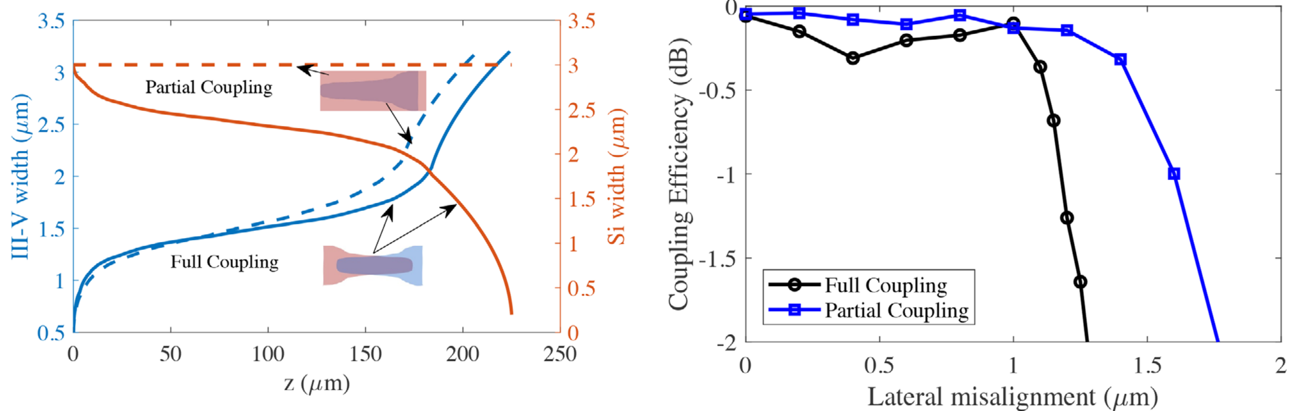

Figure 5. (Left) The III-V and Si adiabatic taper width variation along its length. The blue line and the left vertical axis represents the III-V adiabatic taper shape for the partial and full coupling designs. The red line and the right vertical axis represents the Si adiabatic taper shape and Si waveguide width in the case of full coupling and partial coupling, respectively; (Right) The simulated coupling efficiency of the adiabatic taper structures for the partial and full coupling designs versus the lateral misalignment.

power coupling between the Si and III-V waveguides is simulated at 1.55 μm wavelength. The coupling efficiency for both designs remain high (>−0.3 dB) until 1 μm misalignment, shown in Figure 5 (right). It drops to −2 dB at 1.24 μm misalignment and 1.76 μm misalignment for the full coupling design and partial coupling design, respectively. Moreover, the coupling efficiency of the partial coupling design is higher in the flat region because of the lower value of ϵ (0.01) chosen to calculate the geometry. Simulations indicate that 0.35 degree angular misalignment results in 1 dB excess coupling loss.

5. SOA Processing on the III-V Source Wafer

The SOAs are fabricated on an InP wafer. The epitaxial layer structure grown by metal-organic vapour-phase epitaxy (MOVPE) is shown in Table 1. The detailed process flow for the fabrication of the SOA is depicted in **Figure 6**. It starts by removing the 100 nm InP sacrificial layer with pure HCl (Figure 6b). A PECVD hard mask of 10 nm SiO_2 and 320 nm SiN at 270° is then deposited (Figure 6c). The hard mask is then patterned using i-line UV lithography to define the SOA mesa and III-V adiabatic taper structures. ICP etching is used to etch the InGaAs and p-InP cladding layer. The dry etch process stops when the active region is exposed. Subsequently, p-InP is anisotropically etched in 1:1 HCl:H_2O for less than a minute. This creates an angled side-wall of p-cladding when the mesa is oriented along the [01 − 1] direction (Figure 6d). Surface oxides on the active region are removed by dipping in the 1:1:20 H_2SO_4:H_2O_2:H_2O and 1:10 BHF:H_2O. Next, a layer of 200 nm SiNx at 270° is deposited to protect the side-walls of the SOA mesa. The SiNx layer also acts as a hard mask for the patterning of the AlGaInAs QWs. The QWs are partially etched using ICP and partially in 1:1:20 H_3PO_4:H_2O_2:H_2O (Figure 6e) to stop on the n-InP. After the QW etching, Ni/Ge/Au contacts are formed on the n-InP through a lift-off process (Figure 6f). The sample is again passivated with first SiNx and then planarized with DVS-BCB. In the following step DVS-BCB and SiNx are etched to expose the p-InGaAs contact layer for Ti/Au metal deposition (Figure 6h). The coupon boundaries are then formed by etching back the DVS-BCB and InP using a dry-etching process (Figure 6i). The exposed release layer is then patterned using 1:1:20 H_3PO_4:H_2O_2:H_2O etchant (Figure 6j). The etching stops at the InP substrate. Afterward, ICP is used to etch into the substrate so that tethers anchor to the substrate. At this moment, the sample is also dipped in 1:1 HCl:H_2O for few seconds to have a cleaner surface and better adhesion of the tethers to the InP substrate. A thick photoresist of 3.5 μm is spin-coated on the sample and patterned to encapsulate the device and to form tethers that will hold the device after the under-etching of the release layer. An aqueous $FeCl_3$ solution at 7° is used to under-etch the AlInAs release layer. It takes 2 h to etch a 45 μm wide coupon. The coupons at this point stand on the resist anchors (tethers). These coupons are fabricated in a dense array with a vertical pitch of 90 μm on the InP substrate, the top view of patterned and released coupons is illustrated in **Figure 7a**. The SOA coupons discussed herein are 45 μm wide and 1.4 mm in length.

6. Micro-Transfer-Printing of SOAs

A PDMS stamp with a post of 1400 × 60 μm^2 in size is used for printing 45 × 1400 μm^2 SOA coupons using an X-Celeprint μTP-100 tool. Although a single post stamp was used in this experiment, a multiple post array stamp can print multiple devices at the same time. This is more useful for high throughput integration on wafer-scale. The SOA coupons are printed on a passive Si photonic waveguide circuit. It has a 400 nm thick Si device layer and the waveguides are etched 180 nm deep. The BOX layer is 2 μm.

The target sample (Si photonic waveguide circuit) is spin-coated with a DVS-BCB:mesitylene 1:4 solution at 3000 rpm, followed by a soft bake at 150° and cooling down to the room temperature. After the prepartion of the target sample, both the SOA coupons source sample and the SOI target sample are loaded into the micro-transfer-printing tool. The source and the target samples are aligned. A good angular alignment is critical for the long SOA devices. The printing process is shown in Figure 6. It

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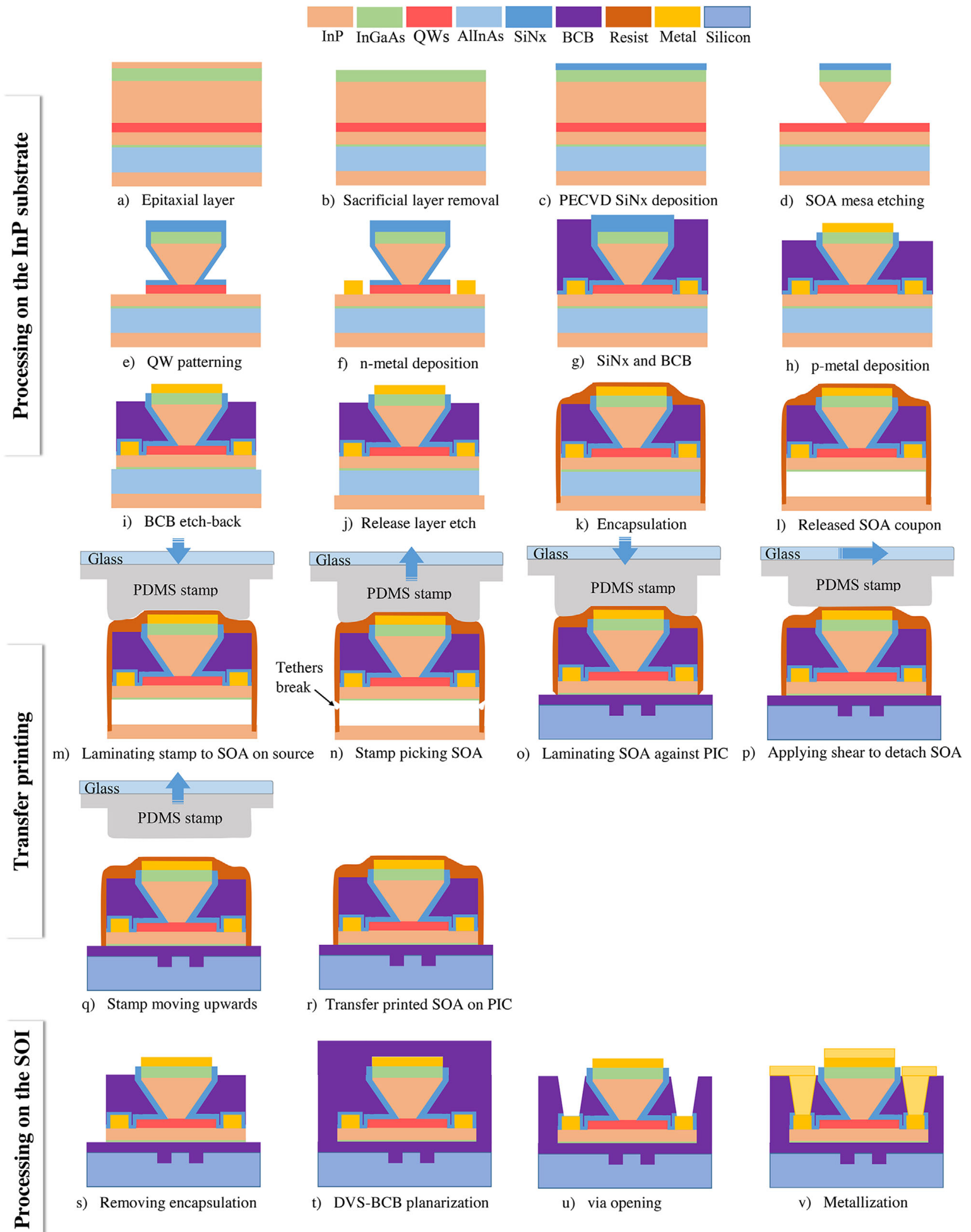

Figure 6. The complete process flow of SOA device fabrication which includes patterning on the source InP substrate, micro-transfer-printing, and final processing steps on the SOI substrate.

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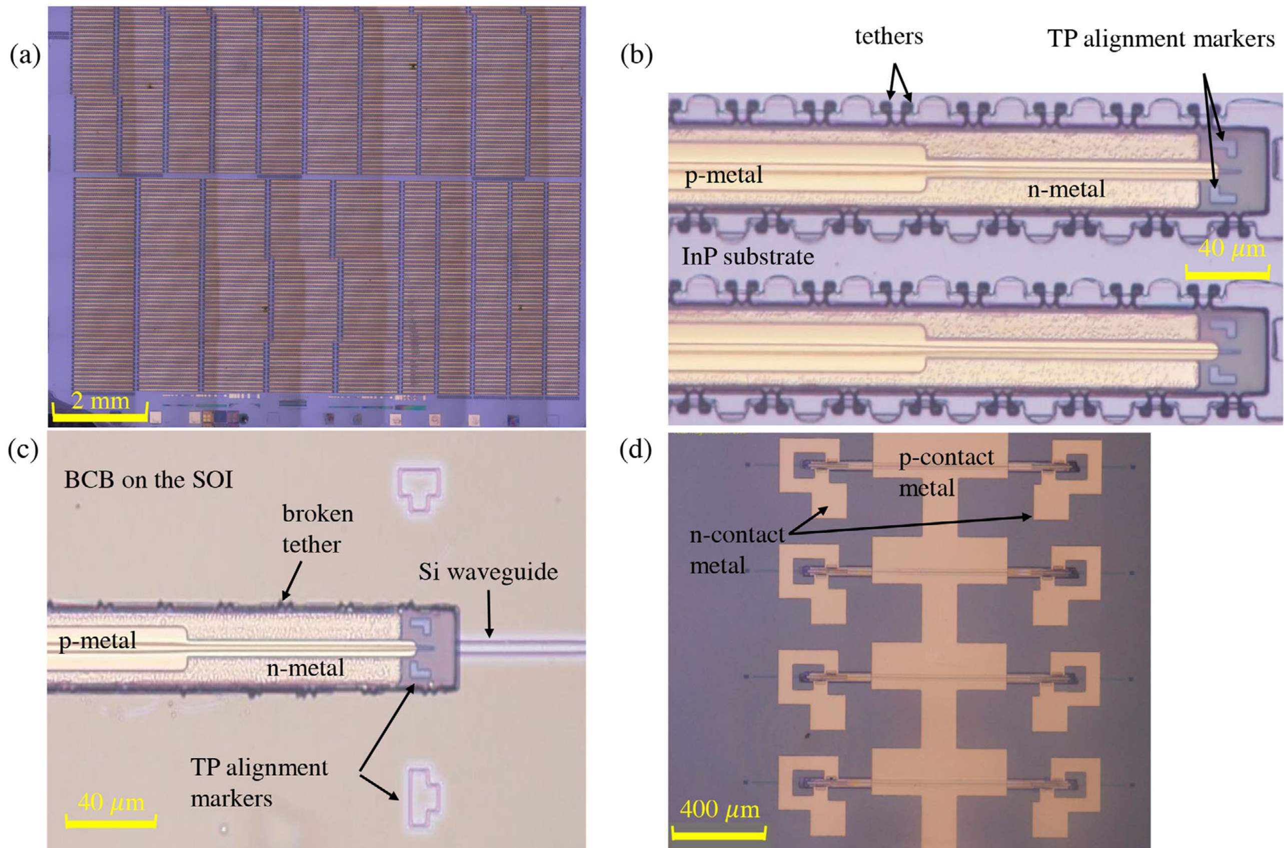

Figure 7. a) microscope top image of an array of SOA devices patterned and released on the native InP substrate, b) Zoomed-in top image of two SOA coupons, c) The SOA coupon after printing on the SOI waveguide, d) The microscope top image of several SOA coupons (devices) after the final metallization step on the target substrate.

starts with laminating the stamp to the released SOA coupon. The stamp then accelerates away from the coupon breaking the tethers at the narrowest point on the top of the previously present AlInAs release layer. After the pickup, the COGNEX VisionPro software[21] is used to auto-align the coupon doing pattern recognition on the alignment markers both on the SOA coupon and the target circuit, shown in Figure 7c. After the auto-alignment, the stamp is laminated to the target SOI and when in contact, a shear force is applied to the stamp in the x- and y-directions to detach the SOA coupon from the stamp. The stamp then slowly moves up leaving the SOA coupon on the target site.

7. Post-Processing of the III-V/SOI Structures

In order to avoid having to process III-V semiconductor devices on the SOI target wafer, all SOA processing steps were carried out on the III-V source. The post-processing steps are limited to the removal of the encapsulation, planarization and electrical contacting.The processing steps are shown in Figure 6. The first step is to remove the encapsulation resist using a dry etch process. After the complete removal, the DVS-BCB bonding layer is fully-cured by ramping the temperature from room temperature to 270° and later it is cooled down slowly to the room temperature. The coupons are then passivated with a thick layer of DVS-BCB and fully-cured. This is followed by etching the DVS-BCB and SiN (in case of n-metal) to expose the p-contact metal and n-contact metal. Finally, with a lift-off process a thick layer of Ti/Au is deposited to make electrical contacts to the SOA devices.

8. Device Characterization

The III-V-on-Si PIC is placed on a temperature-controlled stage at 20° for the measurements. The PIC is optically probed with cleaved standard single mode fibers using a fiber stage. Grating couplers are used to interface with the optical fibers. The grating couplers that couple light into the PIC have a wavelength dependent transmission response. Therefore, it is necessary to characterize grating couplers as a function of wavelength to measure the on-chip gain of the amplifiers accurately. In order to do this, reference passive Si waveguides are also fabricated along with amplifiers on the same chip and they undergo the same processing steps as the grating couplers used for interfacing with the SOAs. The wavelength-dependent transmission response of the grating coupler is measured using a tunable laser (Santec TSL-510) and an optical spectrum analyzer (OSA, Advantest Q8381A). The angle of the fiber holders is optimized to align the maximum transmission wavelength of the grating couplers with the gain peak of the two discussed SOAs. At this angle and at a wavelength of

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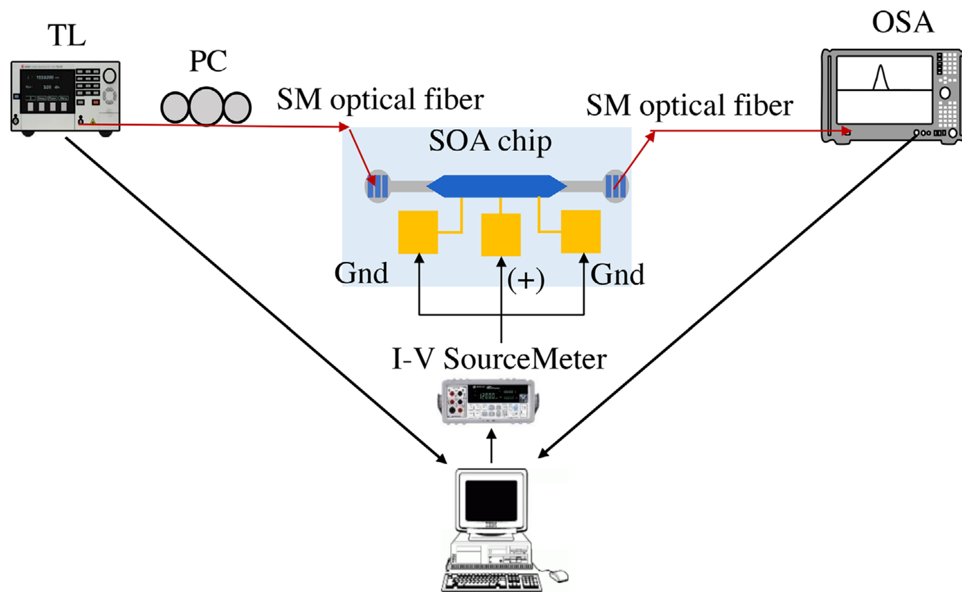

Figure 8. The measurement setup used to characterize the SOAs which includes a tunable laser (TL), polarization controller (PC), optical spectrum analyzer (OSA), and current–voltage sourcemeter. The computer is used to control the instruments and to process the measured data.

1560 nm, the coupling loss per grating coupler is 12 dB. Since the III-V SOAs printed on both SOI designs are nominally the same, the differential resistance is also nominally the same, 10.0 Ω at 80 mA bias current or 1.8 kA cm^{-2} current density. The measurement setup shown in **Figure 8** is used for characterization. The CW input signal generated by a tunable laser is polarization-controlled and coupled into the SOA chip through the grating couplers. The SOA was designed for TE polarized input signal. At the other end of the SOA, the ouput power is coupled from the grating coupler to a single mode optical fiber connected to the OSA (Advantest Q8381A), used to measure the spectrum with 1 nm resolution. The sourcemeter (Keithley 2400) controls the input bias current and probe needles are used to electrically contact the SOA.

In the first experiment, the bias current of the amplifiers is varied and the output power is measured for different wavelength. The output and input power are then normalized with the loss of the reference waveguide and the SOA gain is calculated. This measurement is performed for two values of on-chip input powers, a low one of −24 dBm, and a high one of 0 dBm(or 1 mW), where the SOAs are saturated. Net on-chip gain is observed above 44 and 58 mA for the full-coupling and the partial coupling SOA at 1548 and 1565 nm, respectively. The 1548 nm wavelength corresponds to the maximum gain wavelength for the partial coupling SOA at 160 mA bias current. The full-coupling SOA exhibits parasitic lasing at higher bias currents (>104 mA). It is deduced from the free spectral range of the lasing modes that the lasing is due to the reflections between the two grating couplers. Therefore, for the full coupling SOA all the measurements are performed at lower bias currents and at 1565 nm, slightly off the gain peak of 1557 nm, where parasitic lasing occurs. The full-coupling SOA was only biased till 140 mA (3.17 kA cm^{-2}) as no improvement is seen in the gain beyond 140 mA. However, the partial coupling SOA could be biased until 180 mA due to better heat conduction through the Si waveguide. It can be

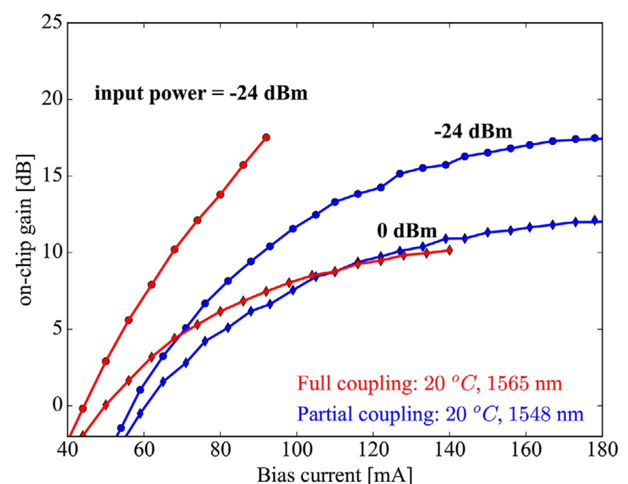

Figure 9. The variation of on-chip gain with the bias current at lower on-chip input power of −24 dBm and higher on-chip input power of 0 dBm for both the full coupling (in red) and partial coupling (in blue) SOA design.

seen in **Figure 9** that at the high input power of 0 dBm the gain saturates to 10 dB at 140 mA and 12 dB at 180 mA for the full coupling and partial coupling SOA, respectively. Moreover, in the unsaturated regime, when the input power is −24 dBm, the full coupling SOA exhibits higher gain for a particular bias current.

To measure the variation of on-chip gain for both SOAs with on-chip input power, the tunable laser's optical power is varied and the SOA output power at the pump wavelength is recorded using the OSA and gain is calculated, as shown in **Figure 10**. The maximum output power at 140 mA is 10.8 dBm at 1565 nm and at 160 mA is 11.3 dBm at 1548 nm for full coupling and partial coupling SOA, respectively. The measurement is repeated for several bias currents. The on-chip gain of the SOA doesn't increase

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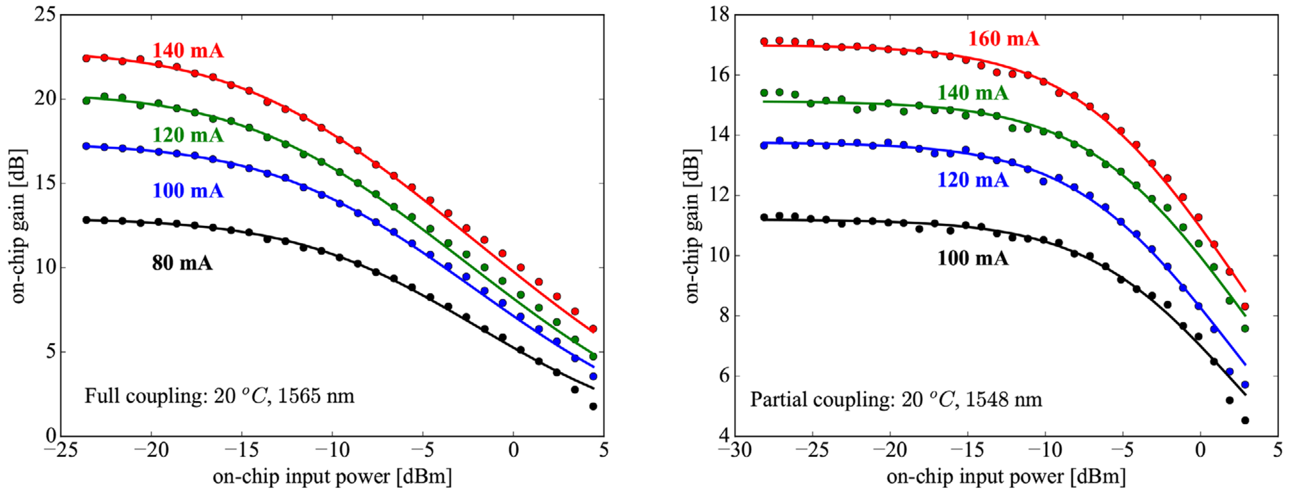

Figure 10. Variation of the on-chip gain with the on-chip input power for various bias currents, (left) for the full coupling design at 1565 nm, (right) for the partial coupling design at 1548 nm. Data points represent the measured values and the solid lines are fitting with Equation (4).

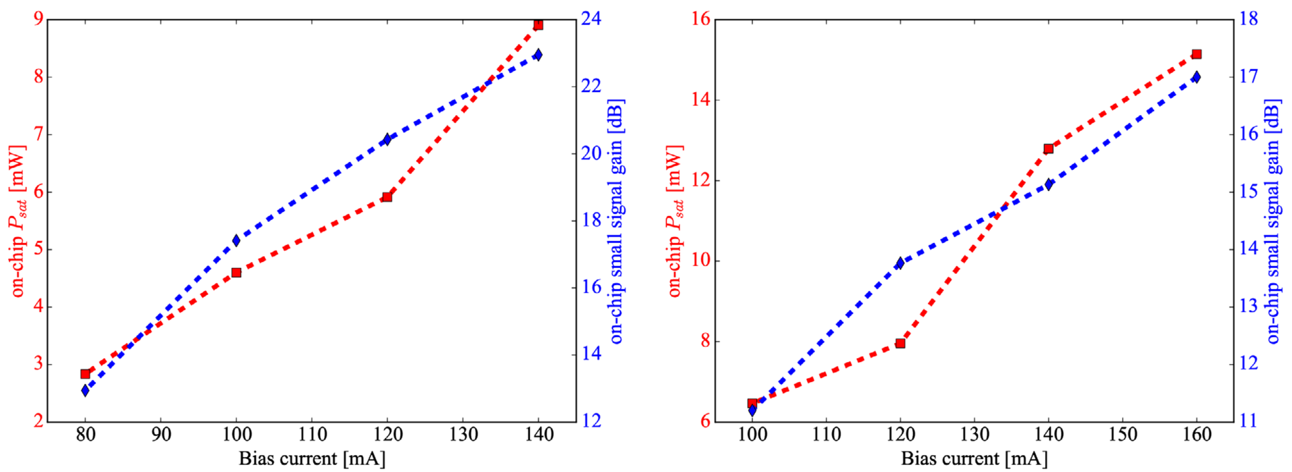

Figure 11. The markers represent the fitted values for power saturation P_{sat} and for the small signal gain G_0 (left) for the full coupling design at 1565 nm and (right) for the partial coupling design at 1548 nm. The dotted lines are guide to the eyes.

beyond 140 mA in the case of full-coupling at 1565 nm wavelength and 160 mA at 1548 nm wavelength for the partial coupling SOA. The measured data are then fitted with an expression that relates the gain G to the input power P_{in} to estimate gain saturation power P_{sat} and small signal gain G_0:[22,23]

$$G(P_{\text{in}}) = G_0 \frac{1 + \frac{P_{\text{in}}}{P_{\text{sat}}}}{1 + G_0 \frac{P_{\text{in}}}{P_{\text{sat}}}} \tag{4}$$

The result of the fitting is shown with solid lines in Figure 10.

The values of P_{sat} and G_0 extracted from the fitting procedure are then plotted against the bias current as shown in **Figure 11**. P_{sat} increases with the bias current and is described by ref. [23]:

$$P_{\text{sat}} = \frac{hc}{\Gamma} \frac{\sigma_{xy}}{a \tau \lambda} \tag{5}$$

where σ_{xy} is the quantum well cross sectional area, λ is the wavelength, a is the differential gain, Γ is the confinement factor in the pumped region of the quantum wells, h is Planck's constant, τ is the carrier lifetime and c is the speed of light in vacuum. When operating the SOA at high bias current, a and τ reduces, which increases P_{sat}.[23] At 140 mA P_{sat} is 12.8 mW and 9.0 mW for the partial and full coupling SOA, respectively. The partial coupling SOA (lower confinement in the QWs) has a maximum P_{sat} of 15 mW at 160 mA bias current (417 mW power dissipation) and small signal gain of 17 dB. In comparison, the full coupling SOA (higher confinement factor in the QWs) has a maximum P_{sat} of 9.2 mW at 140 mA bias current (336 mW power dissipation) and a small signal gain of 23 dB. Hence, the SOA with higher optical confinement factor can provide more gain, but however, has lower saturation power and vice versa.

In order to measure the wavelength dependent small-signal gain of the SOA and the bandwidth, the wavelength of the input light is swept while the on-chip input power is kept at −24 dBm

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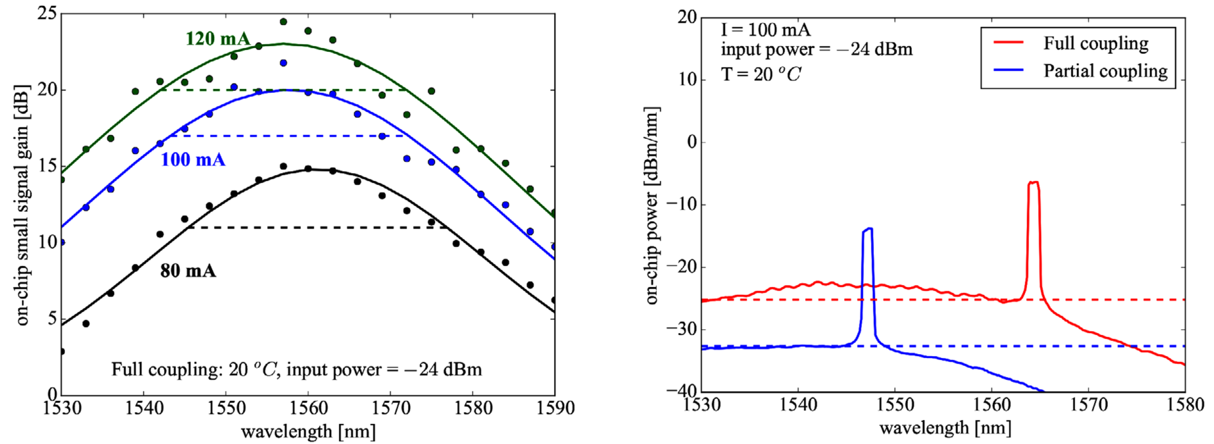

Figure 12. On-chip gain measured as a function of pump wavelength and fitted with Equation (6) for (left) full coupling SOA measured and (b) SOA output spectrum measured with a 0 dBm input power at 100 mA. The red and blue dotted lines indicates the ASE level involved in the computation of noise figure.

and the spectrum is observed on the OSA. The output power at the input wavelength is recorded and normalized with the transmission spectrum of the grating coupler to calculate the on-chip gain, shown in **Figure 12** for the case of full coupling SOA. The measurements were recorded for three different bias currents. The dot markers represent the measured values, the solid line represents the curves obtained by fitting the formula:[24]

$$G(\lambda) = G_p \exp[-A(\lambda - \lambda_p)^2] \tag{6}$$

Where $G_p \equiv exp[g_{net}(\lambda_p)L]$ is the peak value of the gain, λ_p is the wavelength at which the maximum gain occurs and A is related to the gain bandwidth. The 3-dB gain bandwidth of the SOA increases with the bias current and it is 30 nm at 120 mA (2.71 kA/cm^2). Similar gain bandwidth is obtained for the partial coupling device.

Finally, the on-chip noise figure (NF) which determines the degradation of the signal to noise ratio as a signal propagates through the SOA, is estimated. There are two main noise contributors: the shot noise and the excess noise $F_{sig-ASE}$ produced by the beating of the signal and the ASE.[24] The shot noise is given by $1/G$, where G is the gain and the excess noise can be written as:[24]

$$F_{sig-ASE} = \frac{2\lambda^3}{Gc^2h} \frac{P_{ASE}}{\delta\lambda} \tag{7}$$

where λ is the pump wavelength G is the on-chip gain. The on-chip P_{ASE} is measured in a wavelength range of $\delta\lambda$ for a given input power using the OSA. We calculate the $F_{sig-ASE}$ for higher on-chip input powers (>0 dBm) and lower on-chip input powers (<−15 dBm) for the full coupling SOA and partial coupling SOA. At 100 mA and 1565 nm, $F_{sig-ASE} \approx 8.6$ dB for on-chip input power of −24 dBm and $F_{sig-ASE} \approx 9.54$ dB at 0 dBm an on-chip input power. Similarly, at 1548 nm the partial coupling SOA has $F_{sig-ASE} \approx 7.0$ dB at −24 dBm on-chip input power and $F_{sig-ASE} \approx 8.6$ dB at 0 dBm on-chip input power. Figure 12 shows the spectrum used in the calculation of noise figure at −24 dBm on-chip input power. The noise figure values are comparable to the values previously reported in the literature for III-V-on-Si SOA.[22,25]

9. Conclusion

In this paper, we demonstrate the micro-transfer-printing of prefabricated C-band SOAs on Si photonic integrated circuit consisting of a waveguide and grating couplers. Two designs are presented, with a trade-off in small signal gain and output saturation power. An alignment tolerant taper structure is designed that can cope with 1.0–1.5 µm lateral misalignment, which is a typical alignment accuracy that can be obtained when printing large arrays of III-V devices. This showcases the potential of the micro-transfer-printing technique for the scalable integration of III-V semiconductor optical amplifiers and other waveguide-coupled III-V devices (such as laser diodes, modulators, photodetectors) on a Si photonic wafer. While the current demonstration is carried out on a passive Si photonic wafer, comprising only Si passive waveguide structures, the same integration approach can be used on full platform Si PICs comprising high-speed Si/Ge photonic components, by locally opening the back-end and micro-transfer-printing the III-V components in the formed recess. Such an integration would complete the toolkit for advanced photonic systems-on-a-chip based on a silicon photonics platform.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

heterogenous integration, SOA, transfer printing

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