THE PROLIFERATION OF HETEROGENEOUS INTEGRATION APPROACHES IN SILICON (NITRIDE) INTEGRATED PHOTONICS

Roel Baets

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GHENT UNIVERSITY

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ACKNOWLEDGEMENTS

Photonics Research Group

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G. Roelkens, N. Le Thomas, **D. Van Thourhout**

many postdocs and PhD's

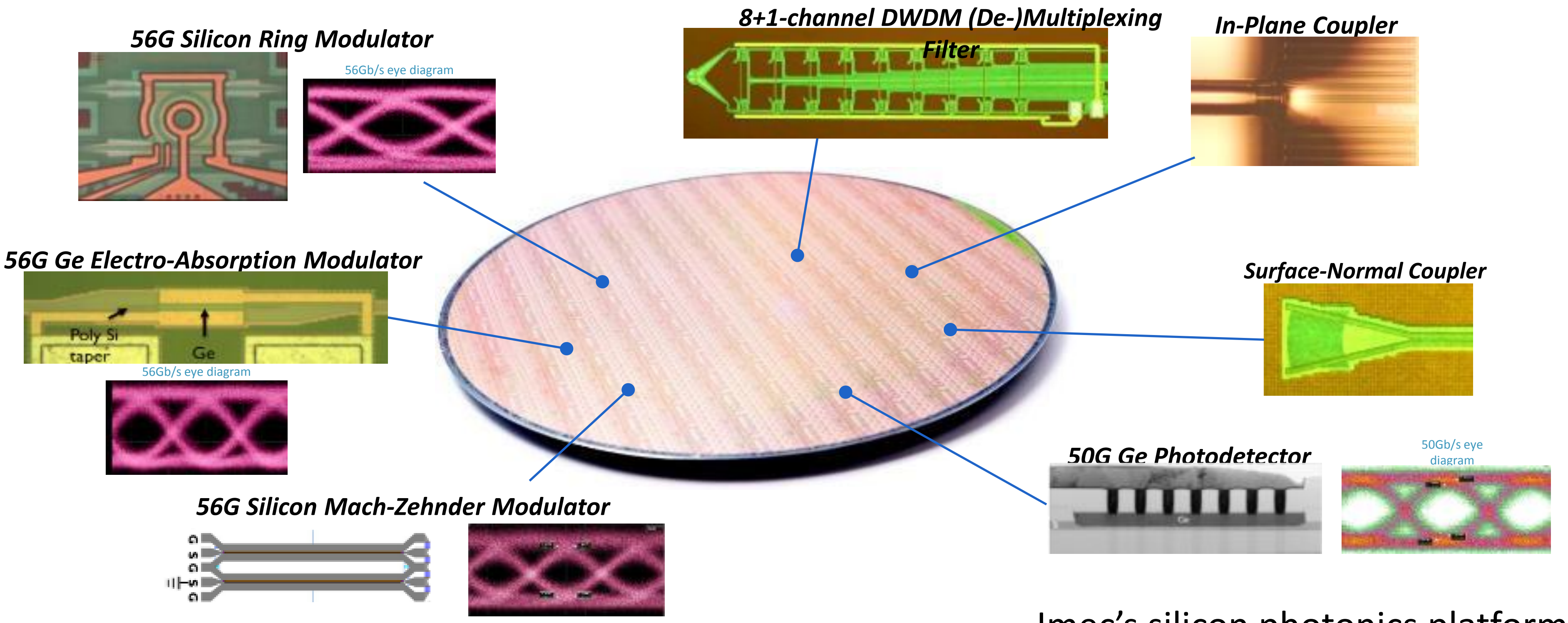
IMEC CMOS process line

and ePIXfab www.epixfab.eu

Funding and collaborations through national and EU research projects

SILICON PHOTONICS PLATFORMS TODAY

Today's mature silicon photonics manufacturing platforms are <u>"homogeneous" or "monolithic"</u>: they build on materials and processes that are well established in CMOS environments.



56G Silicon Ring Modulator

8+1-channel DWDM (De-)Multiplexing Filter

In-Plane Coupler

56G Ge Electro-Absorption Modulator

Surface-Normal Coupler

50G Ge Photodetector

56G Silicon Mach-Zehnder Modulator

Imec's silicon photonics platform

OUTLINE

- ➡ The need for heterogeneous integration
- Diversity in heterogeneous integration
- Moving to wafer-scale heterogeneous process flows
- The case of III-V on silicon

LIMITATIONS OF CURRENT SOI AND SIN (OPEN ACCESS) PIC PLATFORMS

Feature/function	SOI	SiN
Light source integration	Not established	Not established
Phase modulation (electronic)	Spurious AM Bandwidth limitations	Not established
Phase modulation (thermal)	Power hungry	Very power hungry
Linear waveguide loss	Good, not superb	Superb
Nonlinear waveguide loss	Problematic at high power	Superb
Integrated detectors	Good	Not established
Integration with electronics	Limited options	Not established

WHAT IS HETEROGENEOUS INTEGRATION

Generic:

Heterogeneous Integration refers to the **integration** of separately manufactured components into a higher level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics

In silicon photonics:

Heterogeneous Integration refers to the **wafer-level integration of separately manufactured components or CMOS-uncommon materials onto silicon photonics wafers** that, in the aggregate, provides enhanced functionality and improved operating characteristics

FUTURE SOI AND SIN (OPEN ACCESS) HETEROGENEOUS PIC PLATFORMS

Feature/function	SOI	SiN
Light source integration	Superb	Superb
Phase modulation (electronic)	Superb	Superb
Phase modulation (thermal)	Superb	Superb
Linear waveguide loss	Superb	Superb
Nonlinear waveguide loss	Less problematic	Superb
Integrated detectors	Superb	Superb
Integration with electronics	Superb	Superb

OUTLINE

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HETEROGENEOUS INTEGRATION: A STORY OF MANY MATERIALS

III-V on silicon

Colloidal quantum dots on silicon

Liquid crystals on silicon

Electro-optic materials on silicon ($LiNbO_3$, BTO, PZT, polymers, …)

2D-materials (graphene, WSe_2, WS_2, MoS_2…)

Etc.

FIGURES OF MERIT FOR A PHASE MODULATOR

Modulation efficiency $V_{\pi}L_{\pi}$

Voltage swing

Modulation bandwidth

Optical bandwidth

Size

Optical insertion losses

Spurious intensity modulation

Power dissipation

CMOS compatibility

SOI carrier depletion/injection modulators are good enough for many applications but fail to serve others

Exploration of many alternatives, based on heterogeneous integration of electro-optic materials with SOI or SiN

Organic materials

Lithium Niobate

BTO (Barium Titanate)

PZT (Lead Zirconate Titanate)

Emergence of waveguide-MEMS based approaches

HETEROGENEOUS MODULATOR TECHNOLOGIES

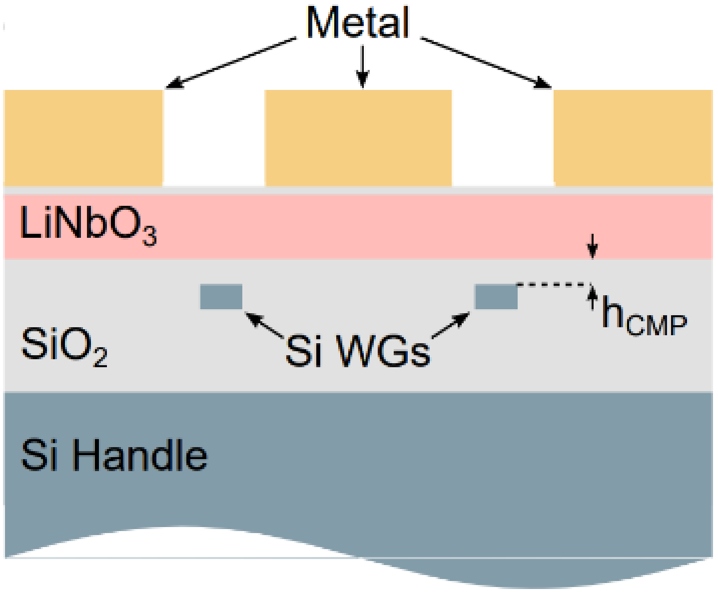
Phase modulators:

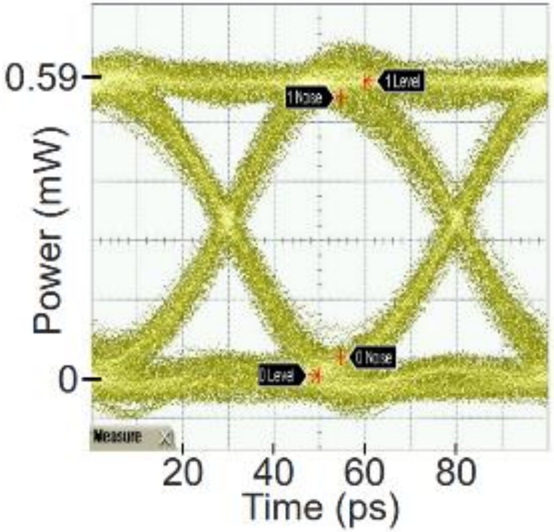
- $LiNbO_3$: thin films bonded on silicon (nitride) circuitry (Harvard, Stanford, Sun Yat-sen University, UCSD, Sandia, UCSB…)
- BTO (Barium Titanate): epitaxially grown on silicon with STO buffer layer (IBM, Yale, imec, …)
- PZT: sol-gel deposition on any substrate (Ghent University)
- EO-polymers: (KIT, ETHZ…)

Amplitude/phase modulators:

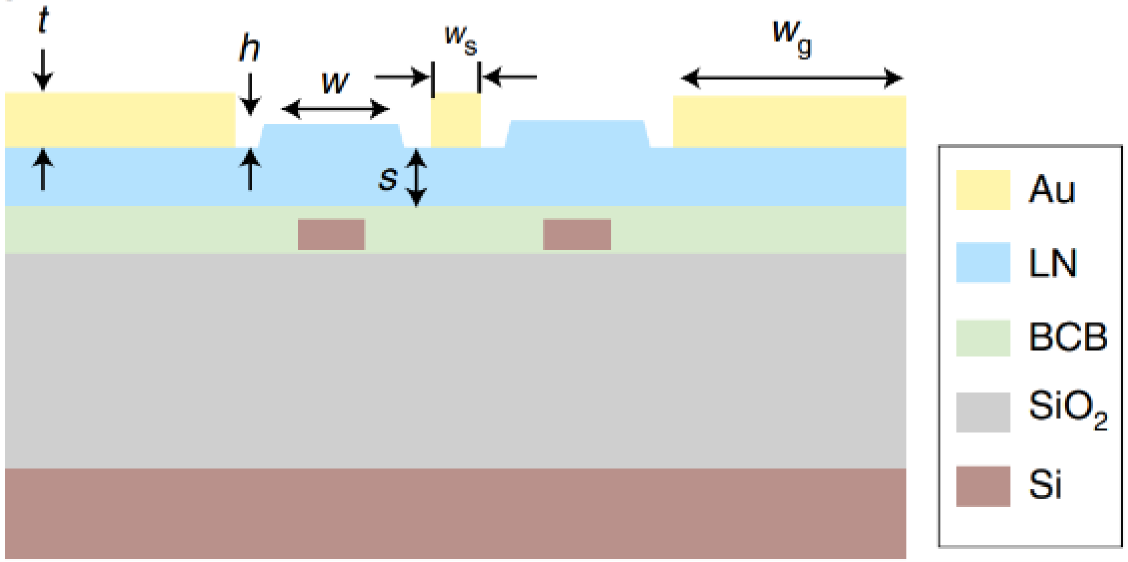
- Graphene: layer transfer (Berkeley, CNIT, imec …)
- 2D TMDCs (Columbia University, George Washington University…)

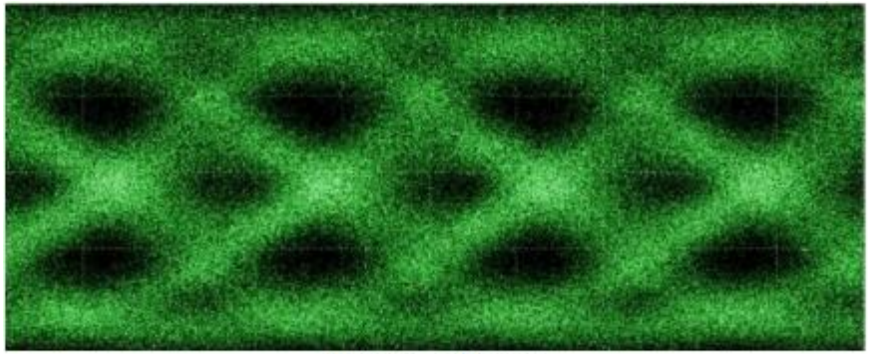
LITHIUM NIOBATE ON SI HETEROGENEOUS INTEGRATION





P. O. Weigel, *et. al.*, “Bonded thin film lithium niobate modulator on a silicon photonics platform exceeding 100 GHz 3-dB electrical modulation bandwidth,” Opt. Express **26**(18), 23728–23739 (2018).



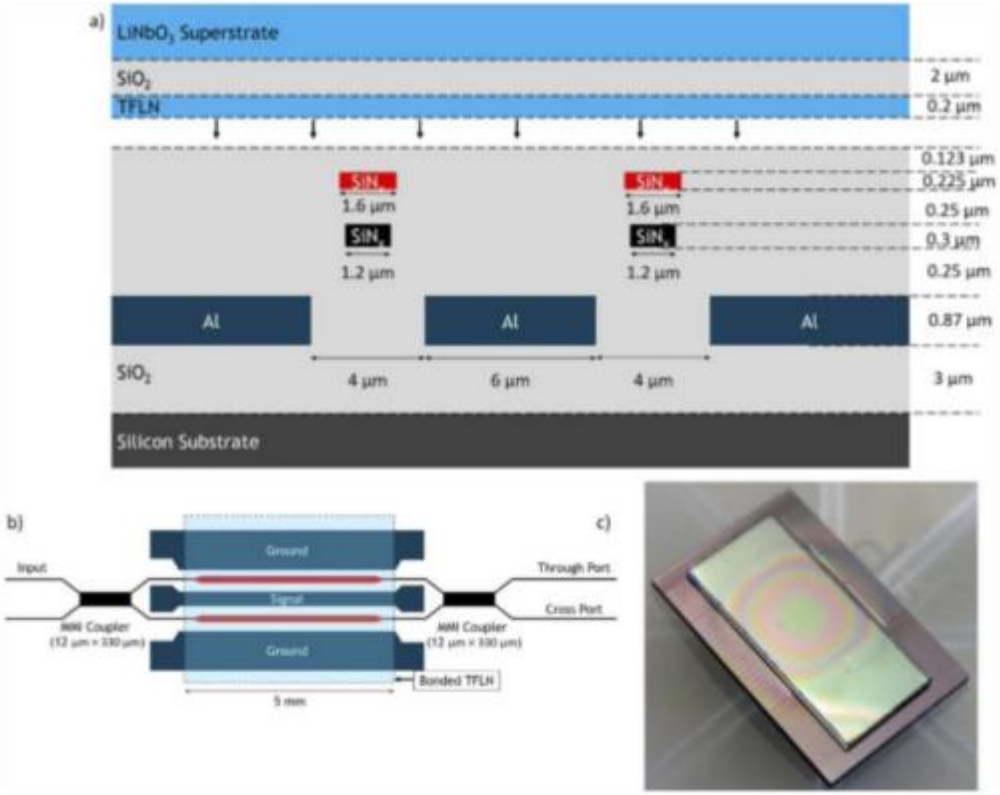


100 Gb s^{-1} OOK

He, M., *et. al.*, “High-performance hybrid silicon and lithium niobate Mach-Zehnder modulators for 100 Gbit s^{-1} and beyond,” Nat. Photonics **13**, 359–364 (2019). https://doi.org/10.1038/s41566-019-0378-6

LITHIUM NIOBATE ON SIN HETEROGENEOUS INTEGRATION

L. Chang, *et. al.*, "Heterogeneous integration of lithium niobate and silicon nitride waveguides for wafer-scale photonic integrated circuits on silicon," Opt. Lett. 42, 803-806 (2017).

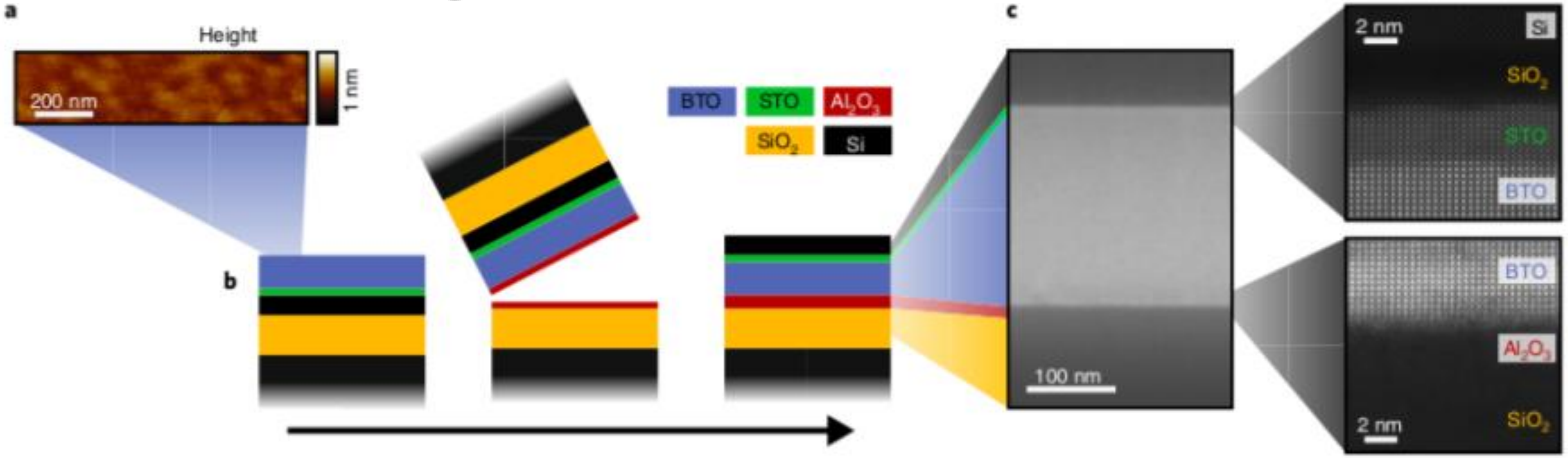


N. Boynton, *et. al.*, "A heterogeneously integrated silicon photonic/lithium niobate travelling wave electro-optic modulator," Opt. Express 28, 1868-1884 (2020).

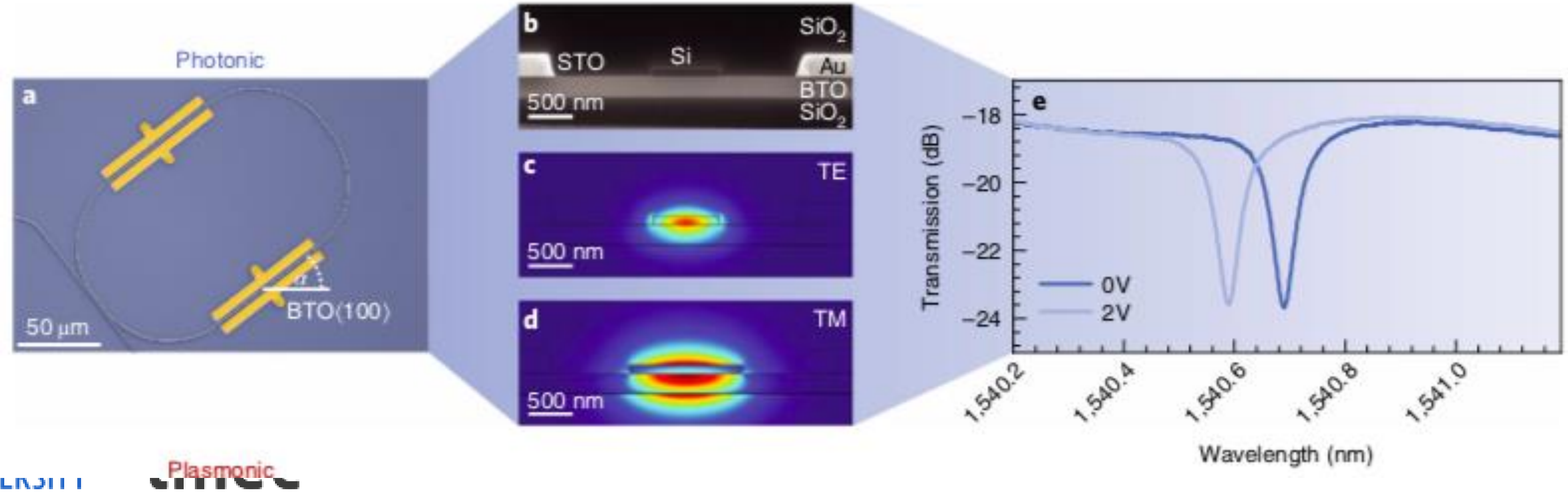

ARTICLES
https://doi.org/10.1038/s41563-018-0208-0
nature materials

Large Pockels effect in micro- and nanostructured barium titanate integrated on silicon

Stefan Abel, et al, *Nature Materials* (2019)



Epitaxy on Silicon wafer
Bonding on SiO2
a-Si waveguides

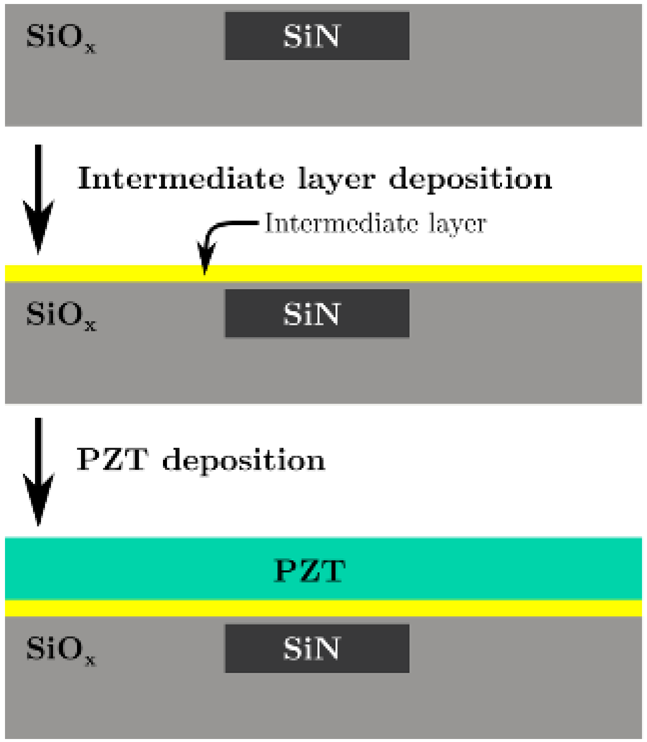


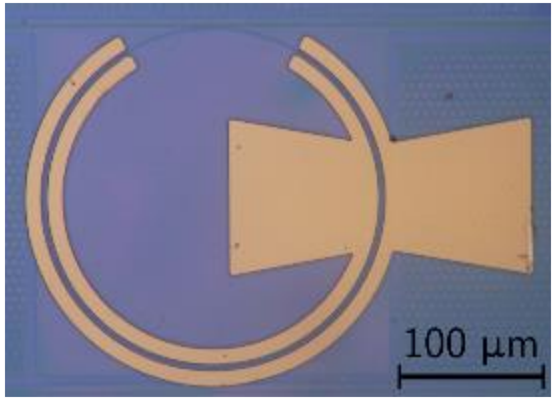
V_π.L=0.45V.cm
50GBit/s in plasmon slot waveguide

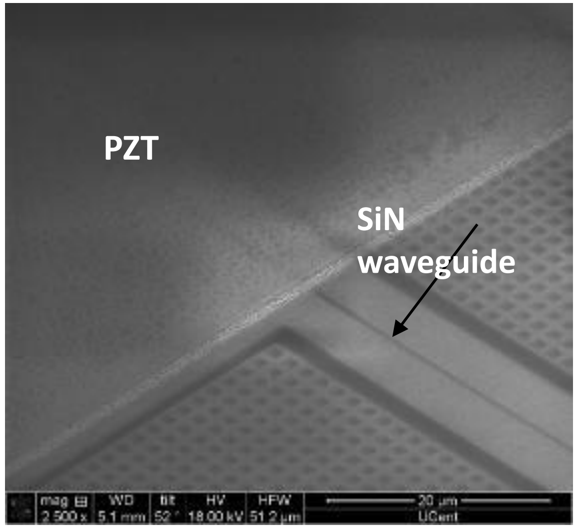
Koen Alexander et al,
Nature Communications (2018)

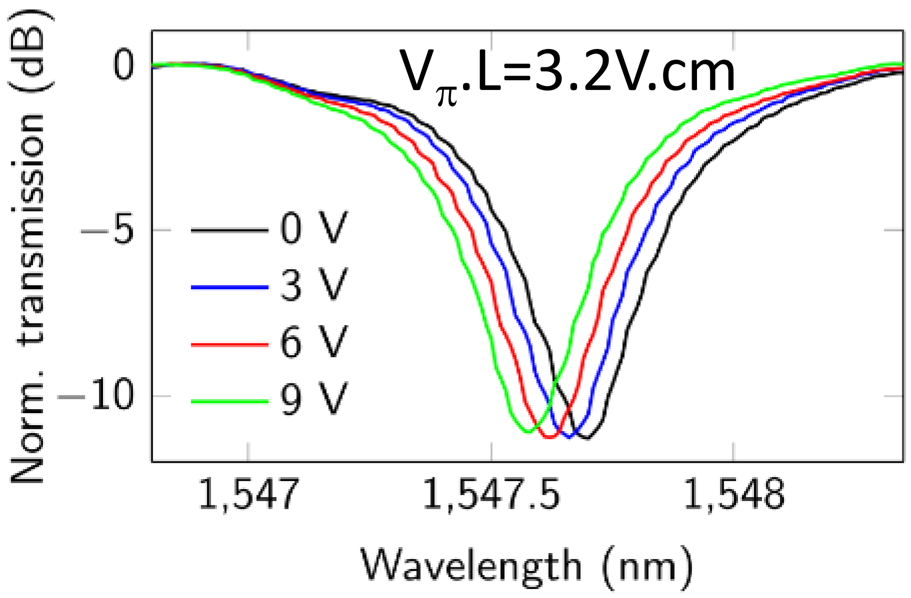
DOI: 10.1038/s41467-018-05846-6 OPEN

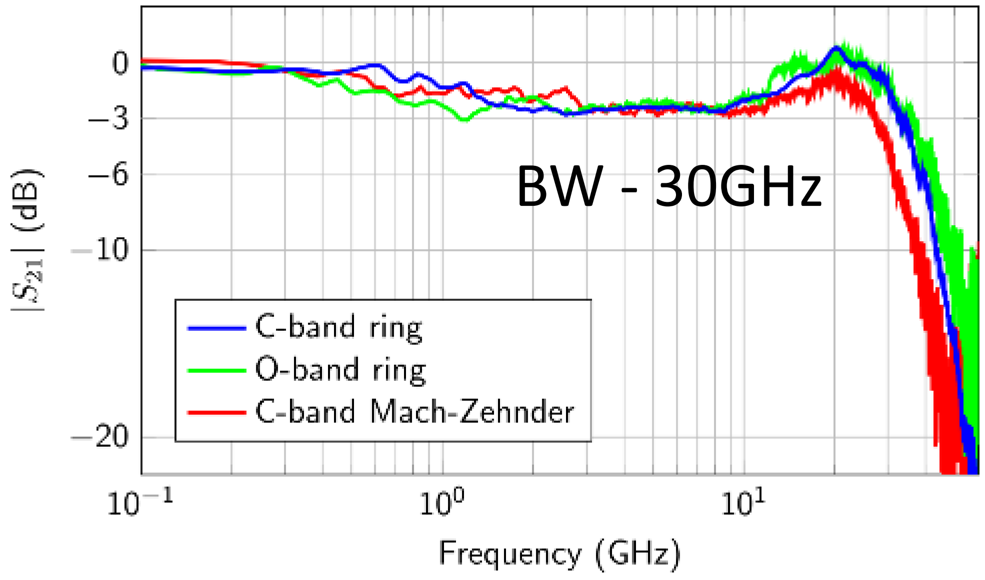
Nanophotonic Pockels modulators on a silicon nitride platform









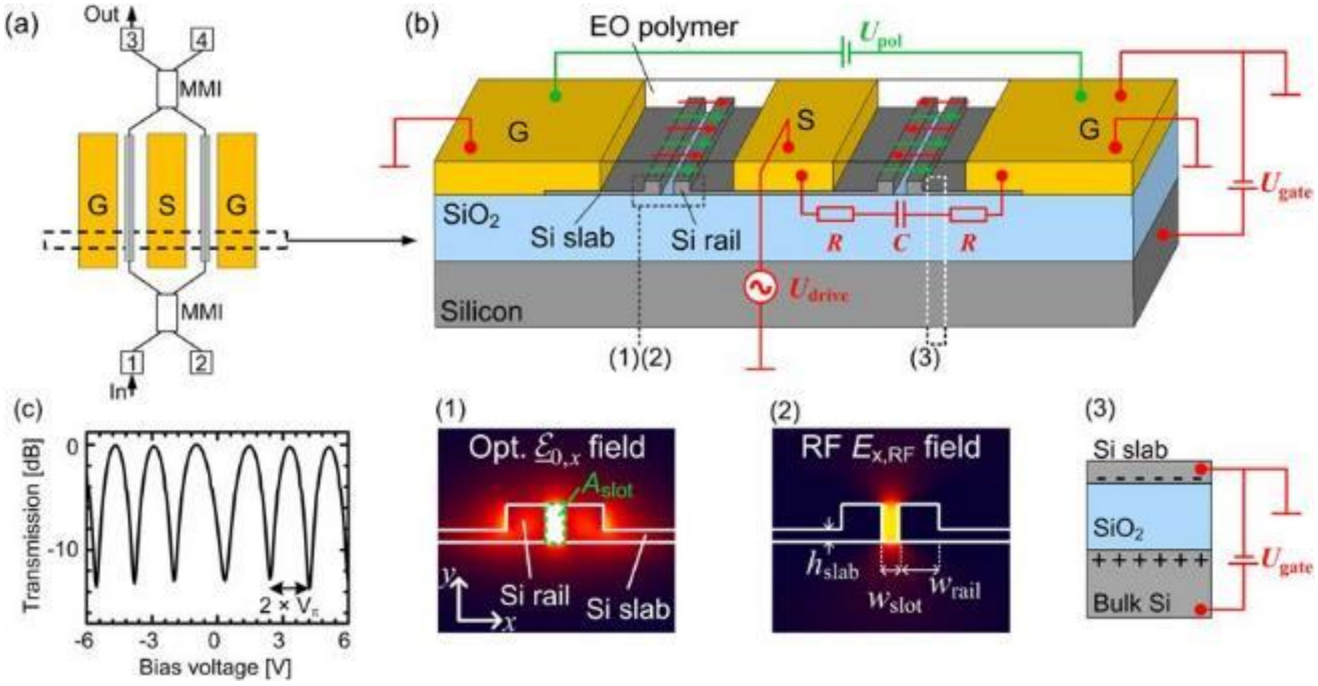


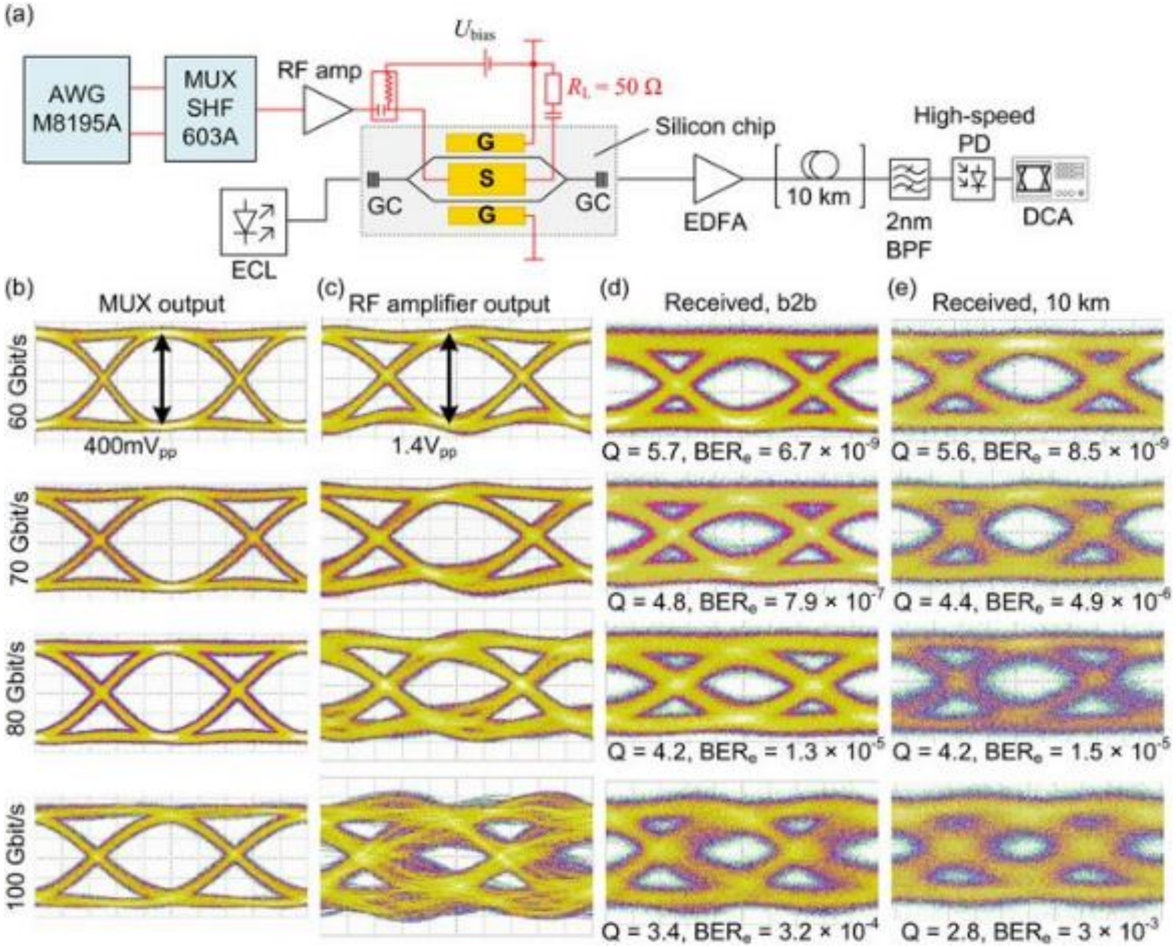
SCIENTIFIC REPORTS

Article | OPEN | Published: 03 April 2018

Silicon-Organic Hybrid (SOH) Mach-Zehnder Modulators for 100 Gbit/s on-off Keying

$V_\pi L$=0.09 V.cm, allows very high speed modulators with low drive voltage





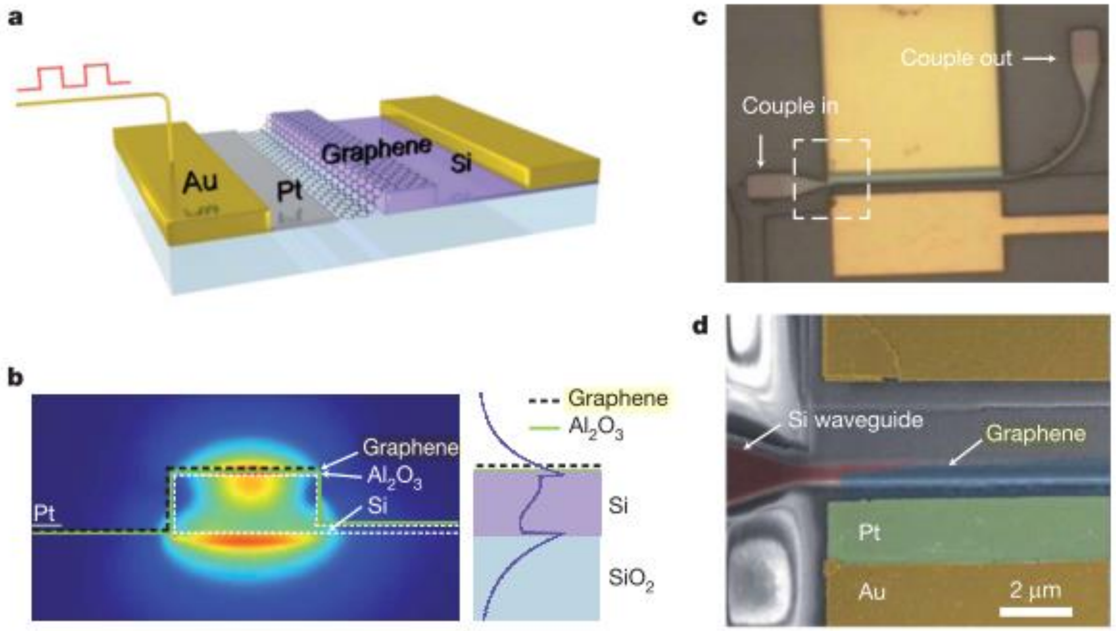
Stefan Wolf et al, *Scientific Reports* (2018)

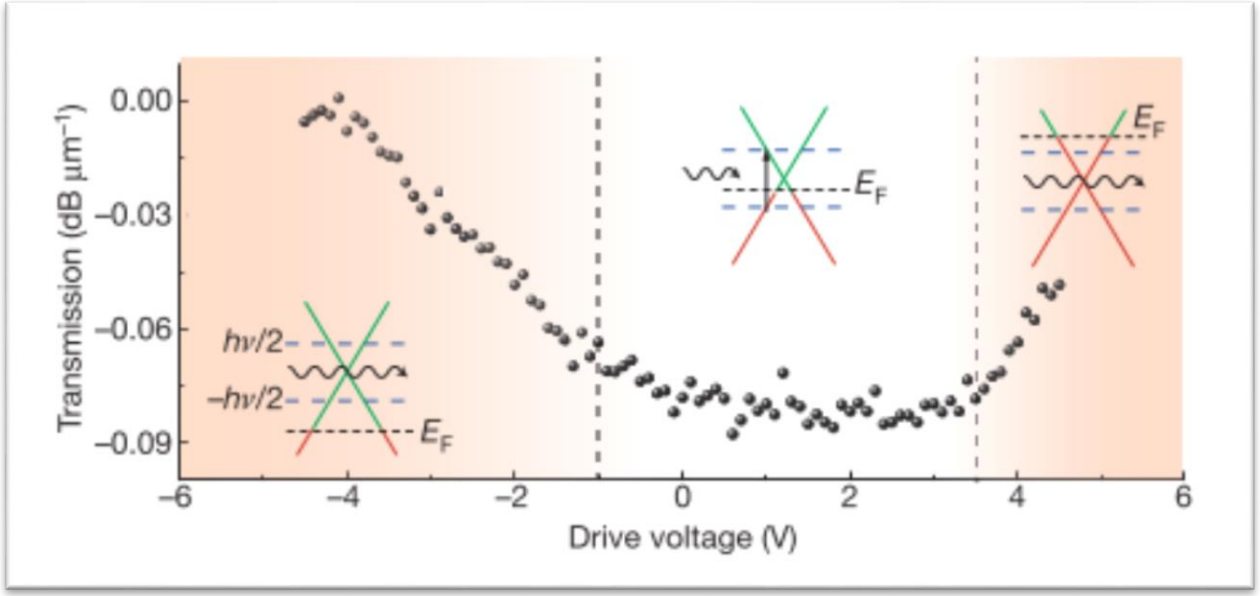
LETTER

doi:10.1038/nature10067

A graphene-based broadband optical modulator

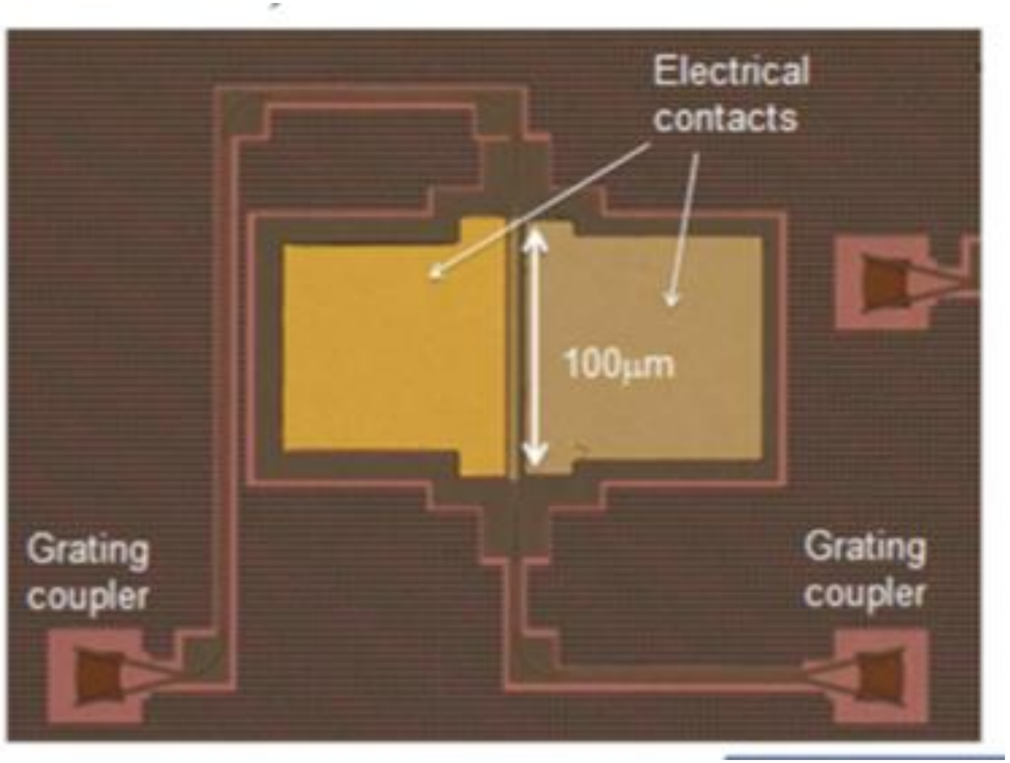
Ming Liu[1]*, Xiaobo Yin[1]*, Erick Ulin-Avila[1], Baisong Geng[2], Thomas Zentgraf[1], Long Ju[2], Feng Wang[2,3] & Xiang Zhang[1,3]

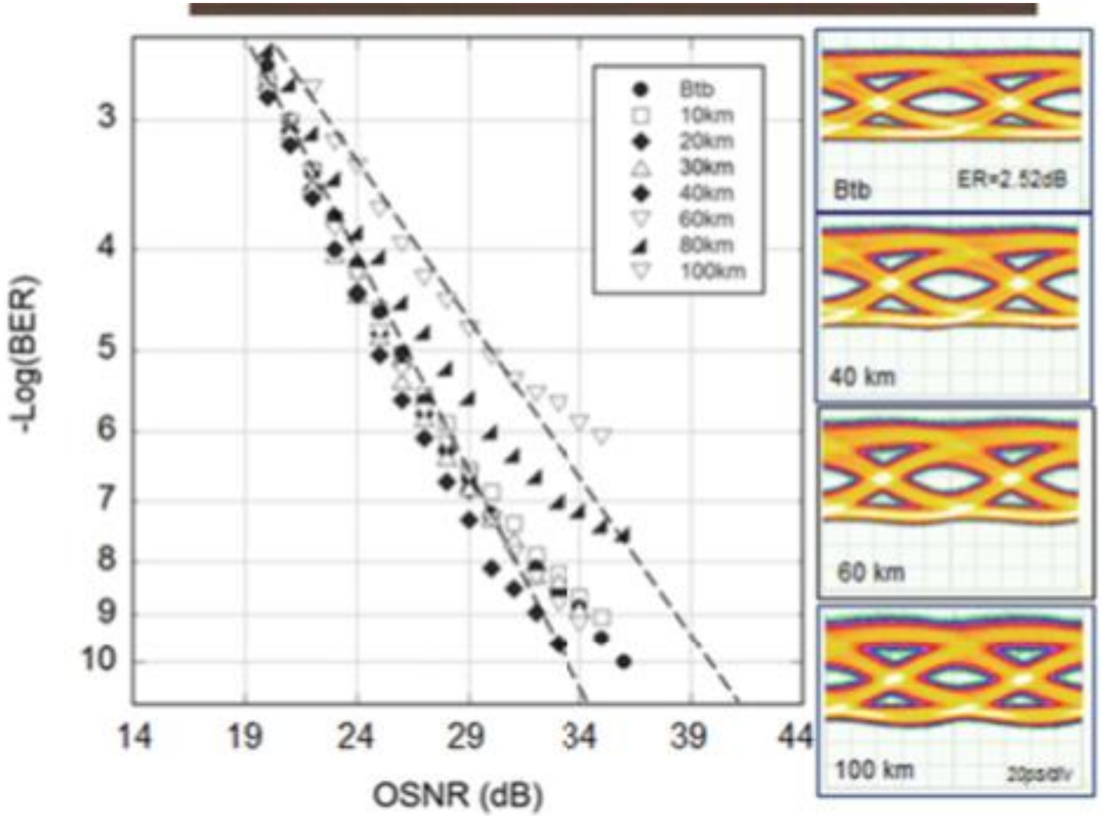




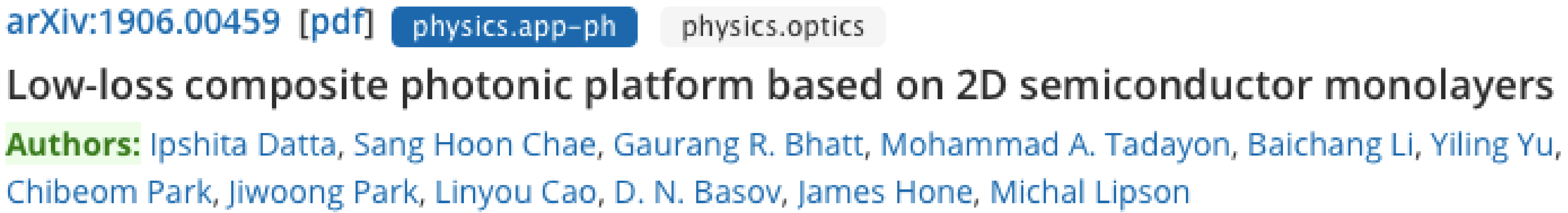
Current demonstrations up to 50GBit/s (eye diagrams), by CNIT & IMEC

GRAPHENE MODULATORS





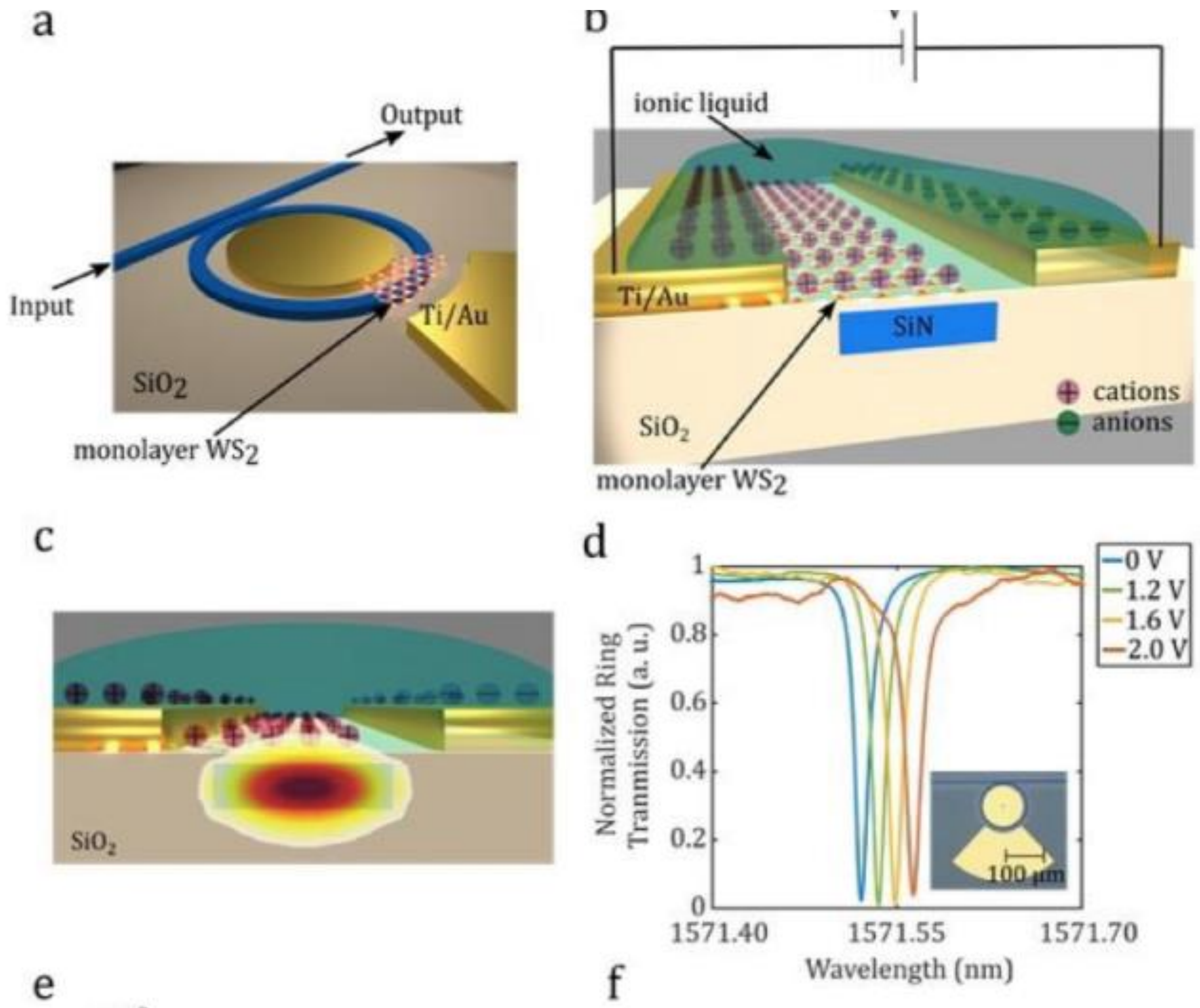
First Demonstration 50GBit/s modulation with graphene modulators (CNIT)



arXiv:1906.00459 [pdf] physics.app-ph physics.optics

Low-loss composite photonic platform based on 2D semiconductor monolayers

Authors: Ipshita Datta, Sang Hoon Chae, Gaurang R. Bhatt, Mohammad A. Tadayon, Baichang Li, Yiling Yu, Chibeom Park, Jiwoong Park, Linyou Cao, D. N. Basov, James Hone, Michal Lipson



- Strong phase-modulation observed in several 2D-materials
- Very low amplitude modulation
- Based on carrier injection: speed ?

See also Sorger-group (several arxiv papers)

OUTLINE

The need for heterogeneous integration

Diversity in heterogeneous integration

➡ Moving to wafer-scale heterogeneous process flows

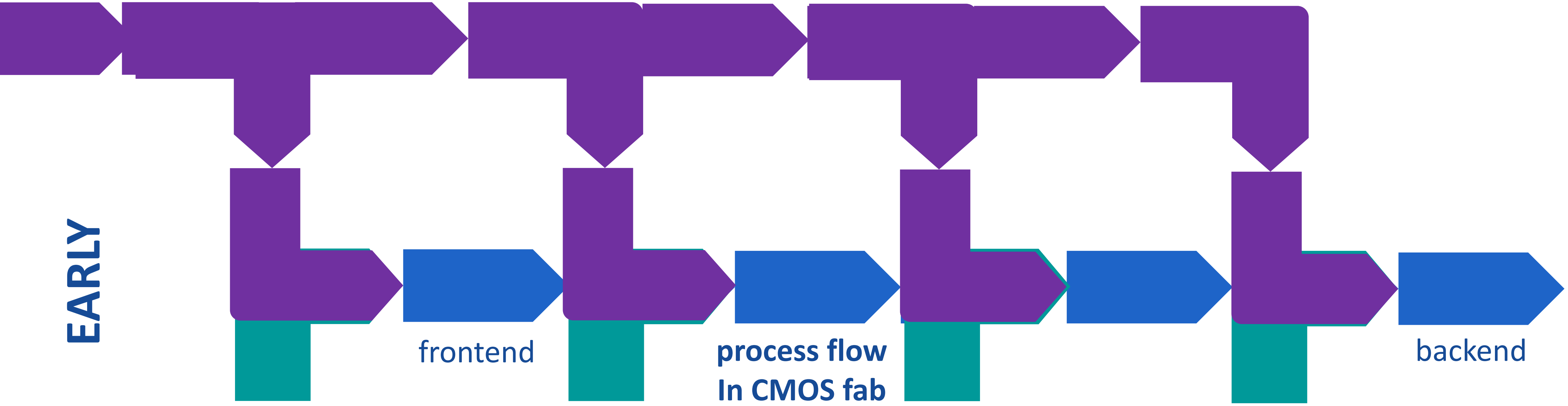
The case of III-V on silicon

MOVING TO WAFER-SCALE HETEROGENEOUS PROCESS FLOWS

Challenges:

- Thermal budget
  - Annealing steps for heterogeneous material may damage earlier processing
  - Annealing steps needed in later processing may damage heterogeneous material
- Contamination
  - Heterogeneous material may contaminate process tools (eg gold)

DIVERSITY IN HETEROGENEOUS PROCESS FLOWS



1) process wafer or chiplets
2) Integrate on Si wafer

1) process wafer or chiplets
2) Integrate on Si wafer

1) process wafer or chiplets
2) Integrate on Si wafer

1) process wafer or chiplets
2) Integrate on Si wafer

EARLY

frontend

process flow
In CMOS fab

backend

LATE

deposit material

deposit material

deposit material

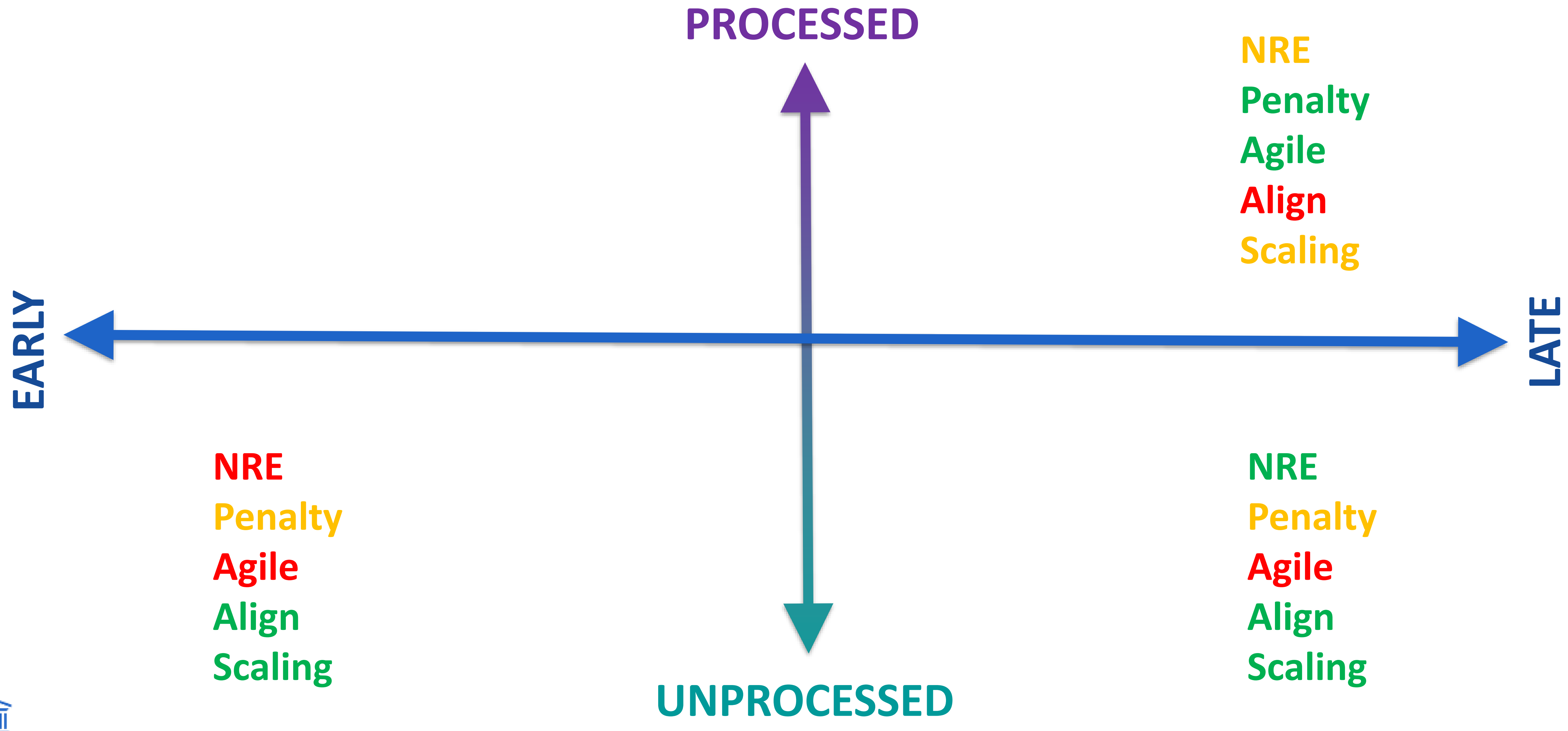
deposit material

UNPROCESSED

DECISION FACTORS

Non-recurrent engineering and tool investment cost	NRE
Heterogeneous integration leads to penalties in performance	Penalty
Technology serves many heterogeneous integration cases and enables fast routes to market	Agile
Heterogeneous integration requires precise alignment	Align
Scaling to high volume manufacturing with low cost	Scaling

SWOT OF HETEROGENEOUS PROCESS FLOWS



PROCESSED

EARLY

LATE

UNPROCESSED

NRE
Penalty
Agile
Align
Scaling

NRE
Penalty
Agile
Align
Scaling

NRE
Penalty
Agile
Align
Scaling

OUTLINE

The need for heterogeneous integration

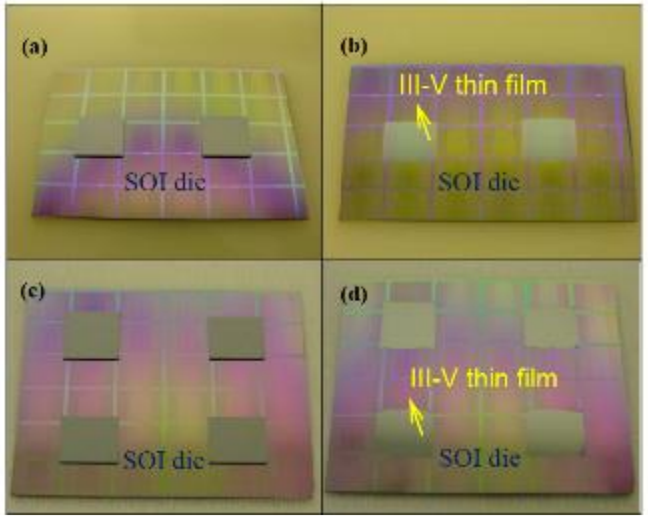
Diversity in heterogeneous integration

Moving to wafer-scale heterogeneous process flows

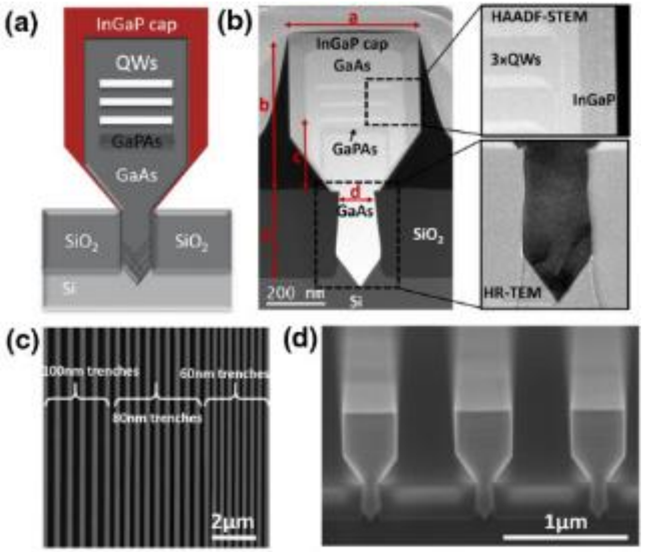
➡ The case of III-V on silicon

WAFER-LEVEL APPROACHES FOR III-V INTEGRATION ON SI PICS

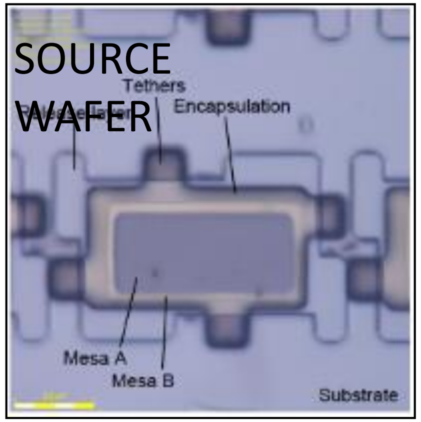
die-to-wafer bonding



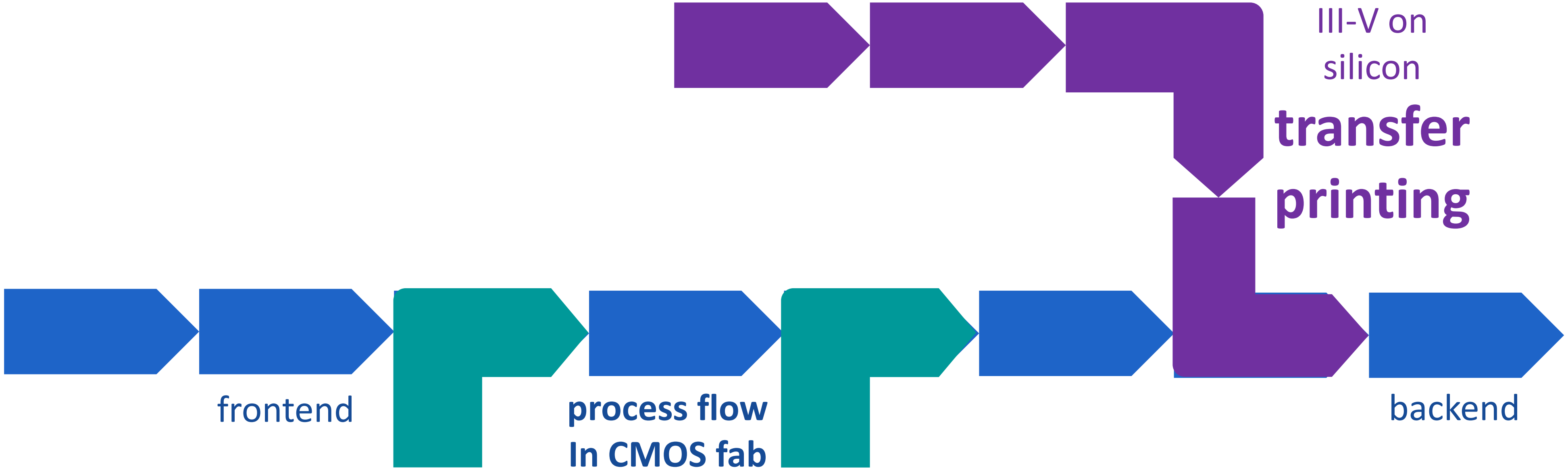
III-V epitaxy on silicon



micro transfer printing



III-V ON SILICON TECHNOLOGIES



III-V on
silicon
transfer
printing

frontend

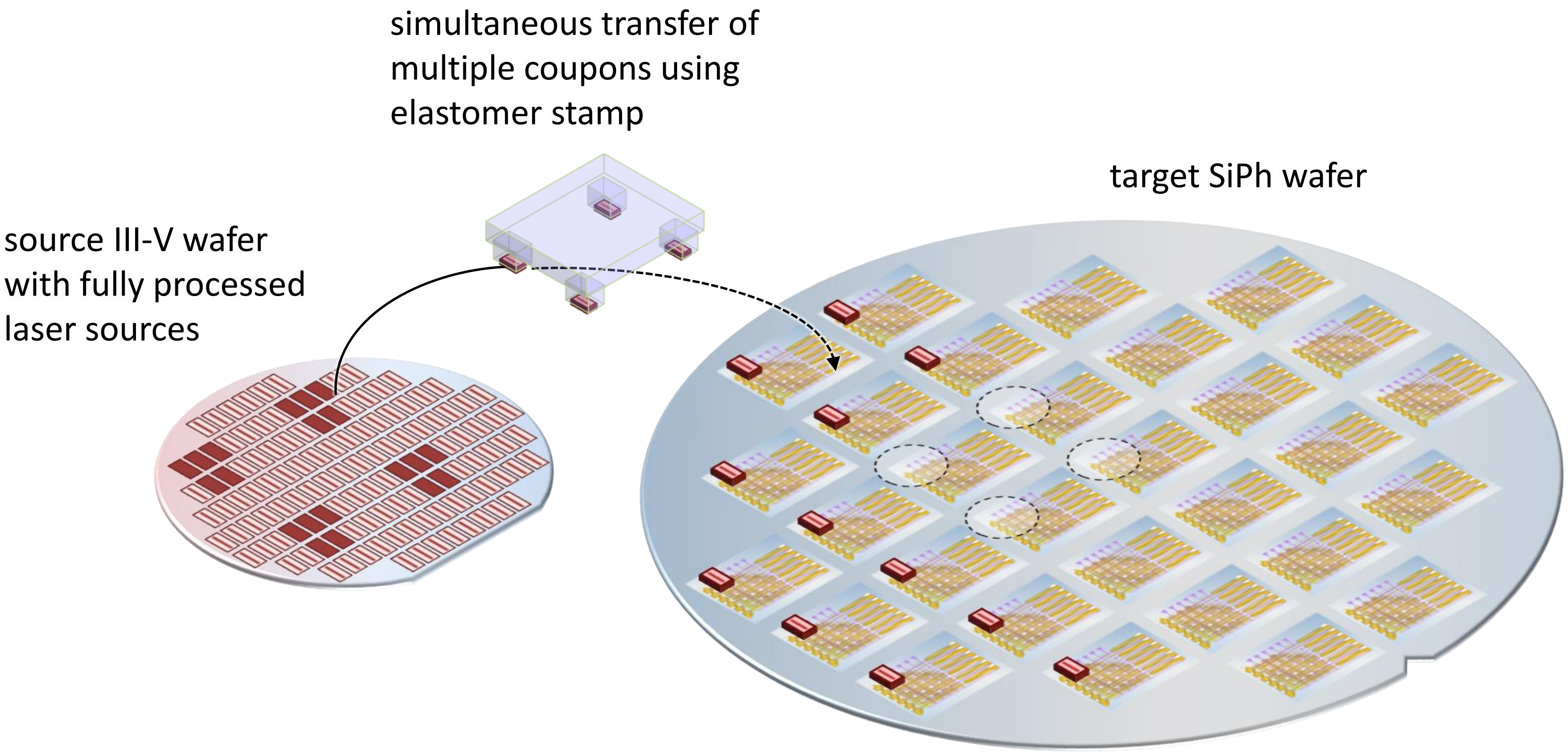
process flow
In CMOS fab

backend

III-V on
silicon
epi

III-V on
silicon
bonding

MICRO-TRANSFER-PRINTING (μTP)



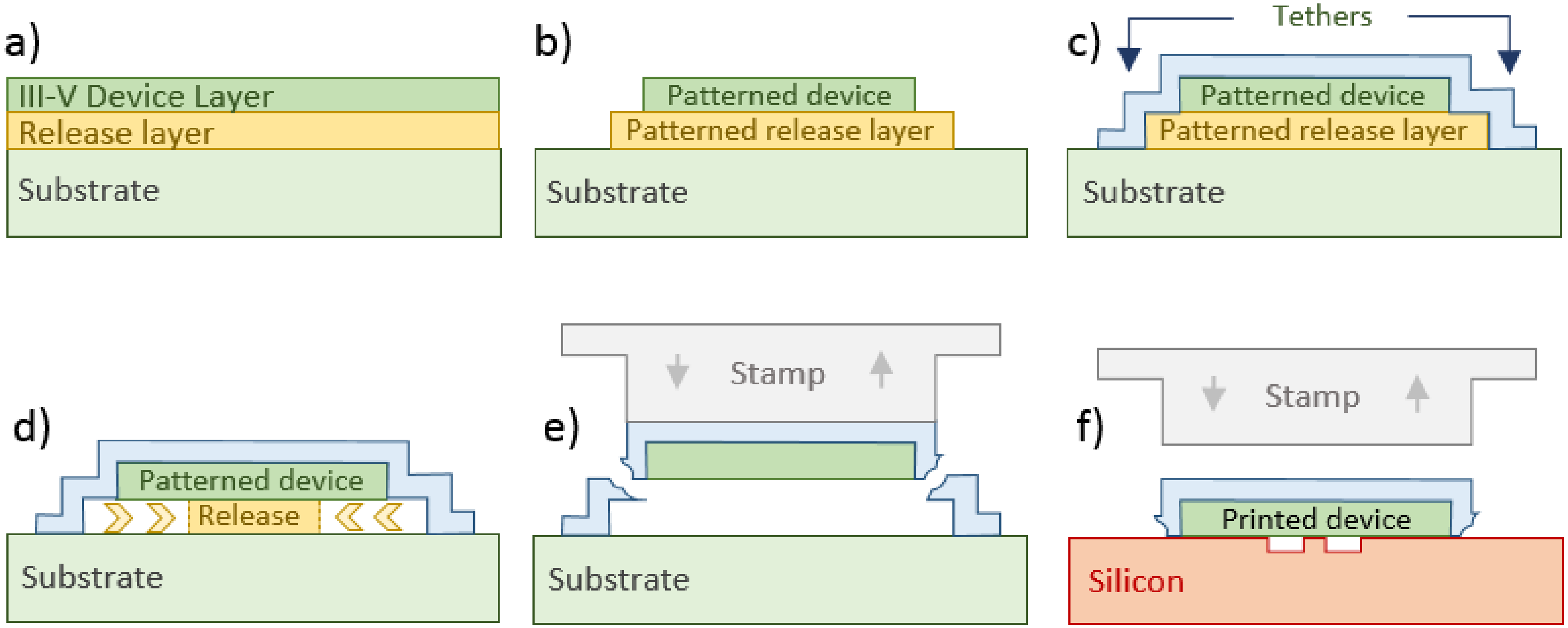
simultaneous transfer of
multiple coupons using
elastomer stamp

source III-V wafer
with fully processed
laser sources

target SiPh wafer

μ-TP combines advantages of flip-chip and die-to-wafer bonding

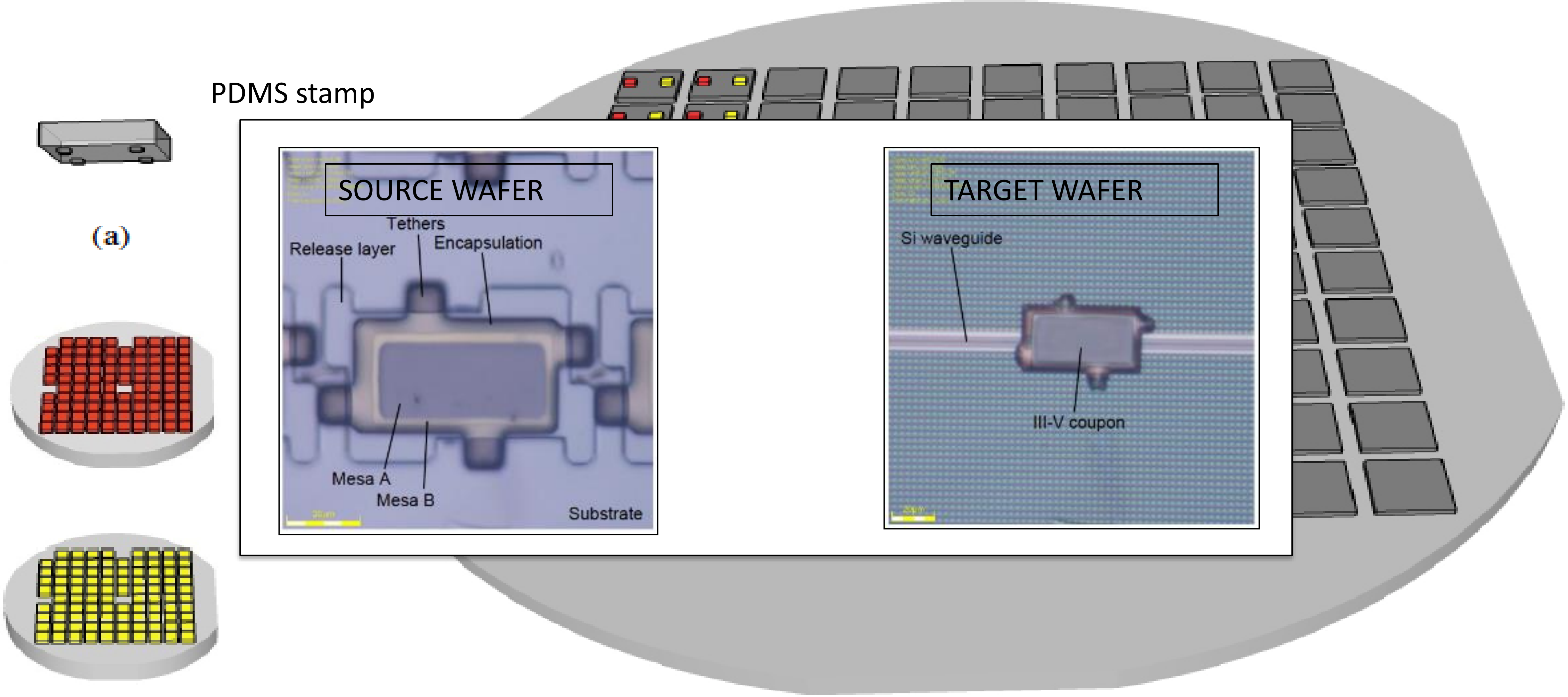
TRANSFER PRINTING



Transfer of <u>micro-scale </u>III-V coupons/devices to a Si target wafer

InP, GaAs, SOI, 2D materials, 0D materials

TRANSFER PRINTING OF III-V SEMICONDUCTORS



PDMS stamp

III-V source wafers

SOI target wafer

μTP COMBINES ADVANTAGES OF FLIP-CHIP AND DIE-TO-WAFER BONDING

Massively parallel

- >10,000 devices (LEDs) transferred per 45s cycle demonstrated
- *Flip chip transfers individual devices.*

Position tolerance of ±1.5μm at 3σ in large arrays

- ±0.5μm and better when printed in small arrays
- Pattern recognition based

The highest quality source materials used

- Can be pre-processed

Different types of devices or materials can be printed close to each other

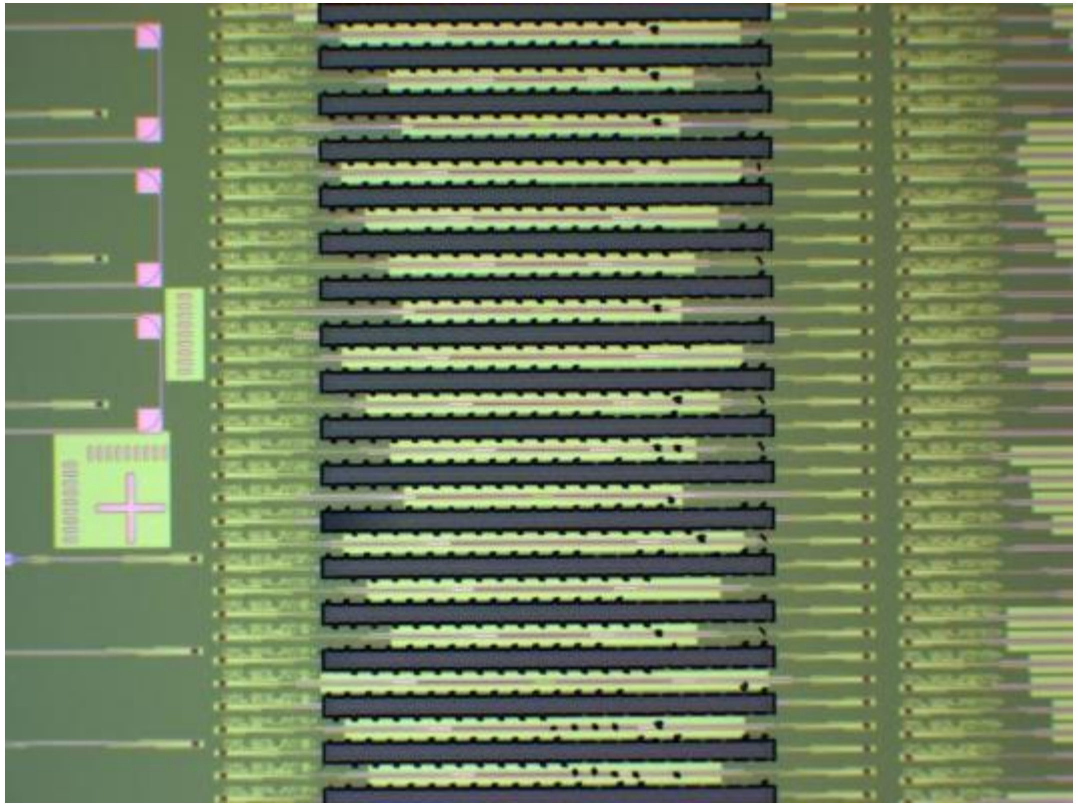
Efficient use of expensive materials

- Width of devices << conventional for higher packing
- Substrate can potentially be recovered

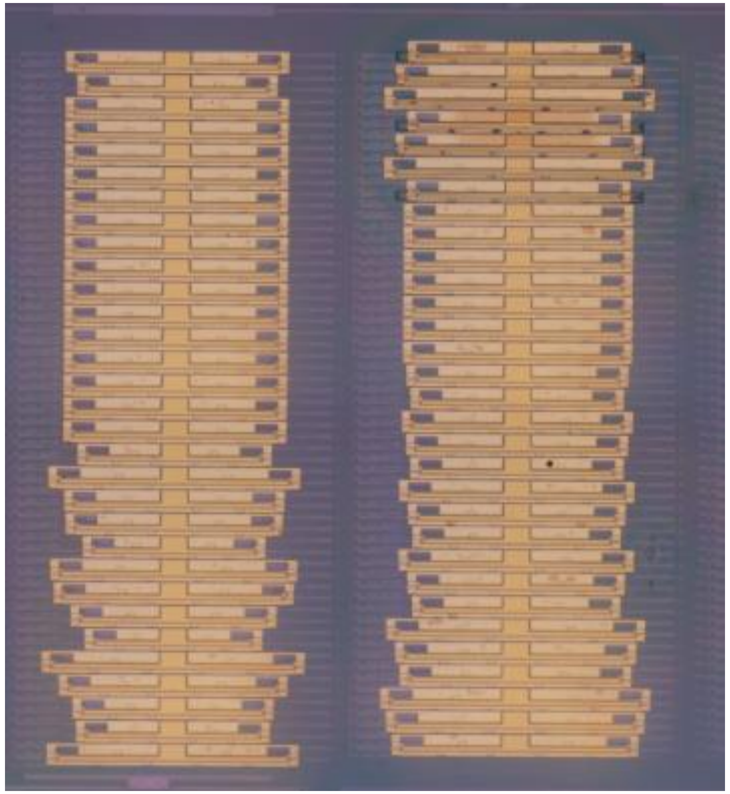
Independent of source substrate diameter

- InP wafers 50-100mm; Si wafers 200-300mm diameter

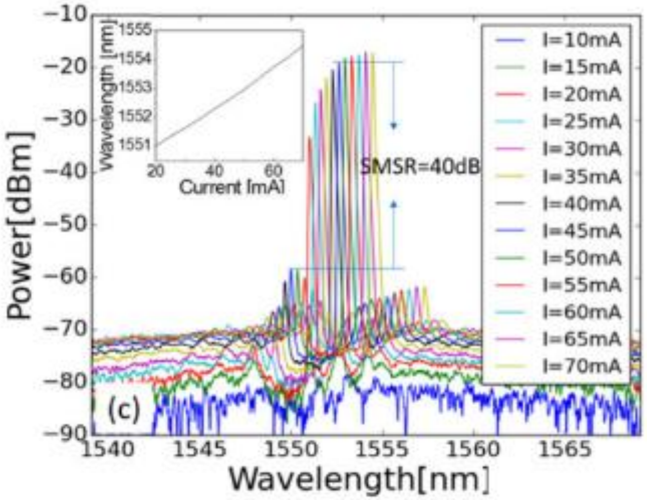
FIRST III-V-ON-SILICON µTP DFB LASERS



After transfer printing of coupons

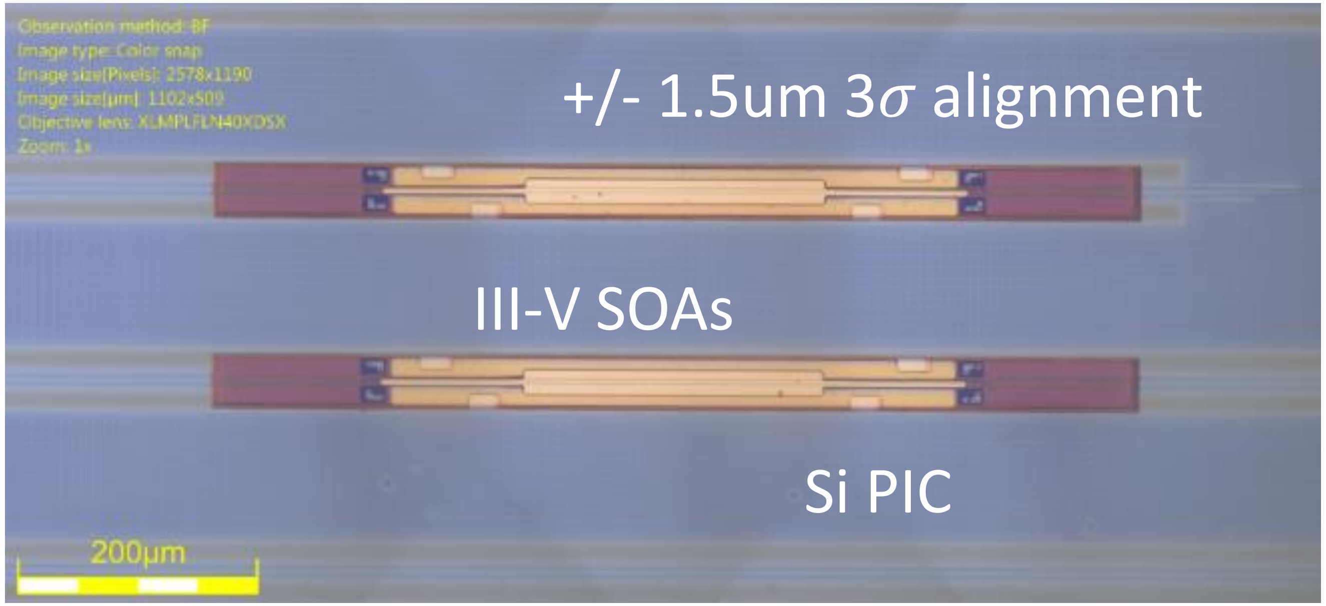


Lasers after post-processing



[J. Zhang et al, Optics Express 2018]

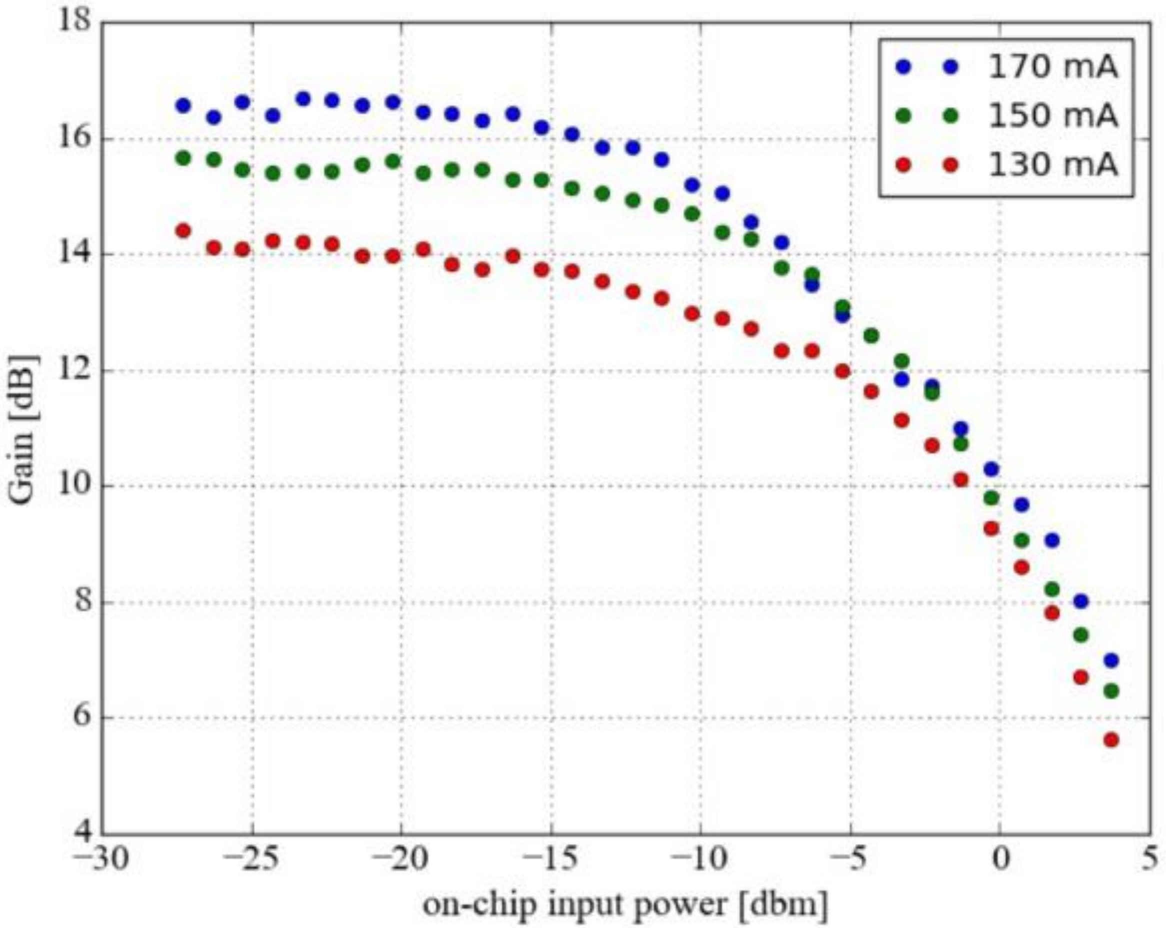
TRANSFER PRINTED C-BAND SOAS



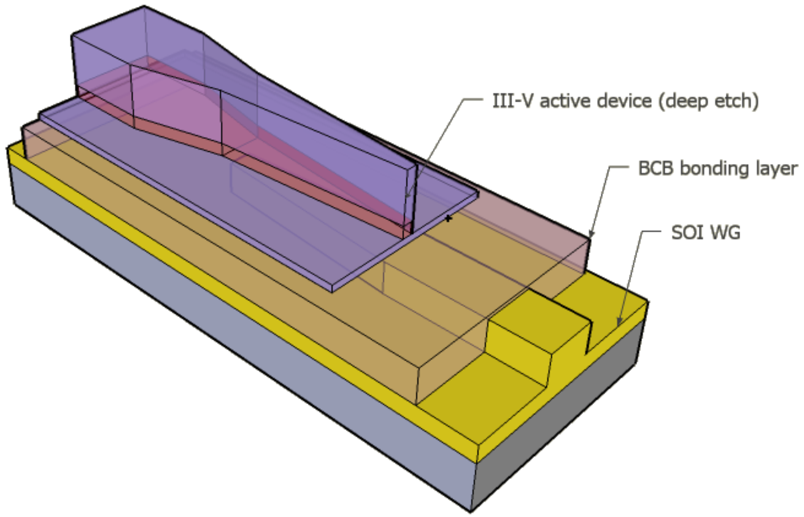
+/- 1.5um 3σ alignment

III-V SOAs

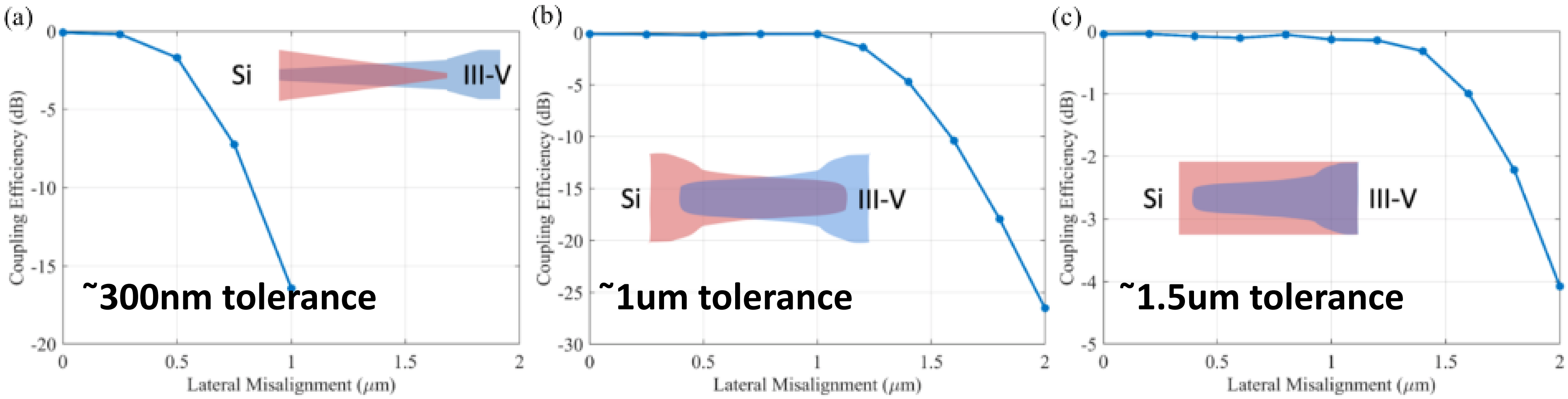
Si PIC



ALIGNMENT TOLERANT OPTICAL INTERFACE



~250um taper length – transfer printing compatible



~300nm tolerance

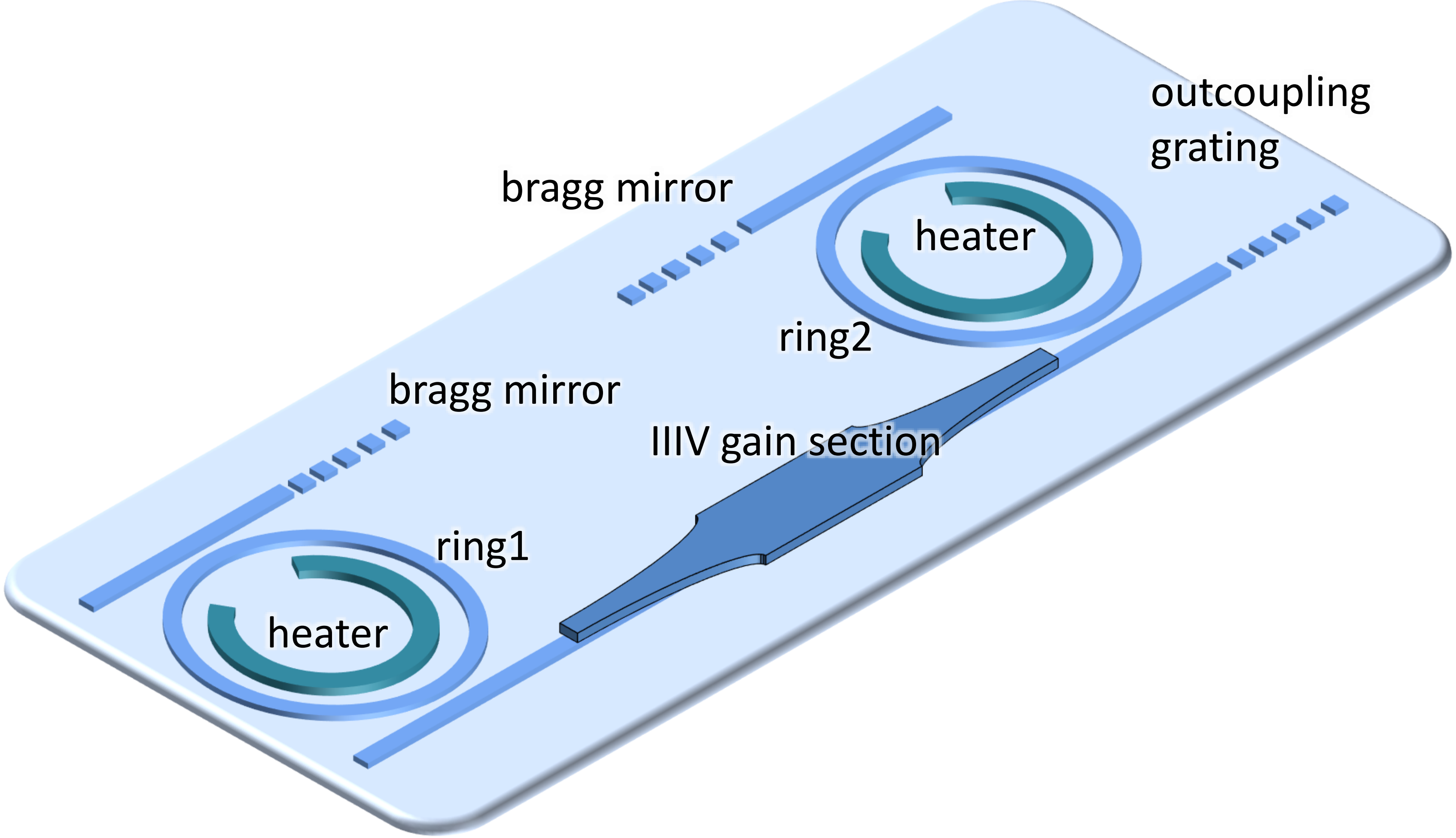
~1um tolerance

~1.5um tolerance

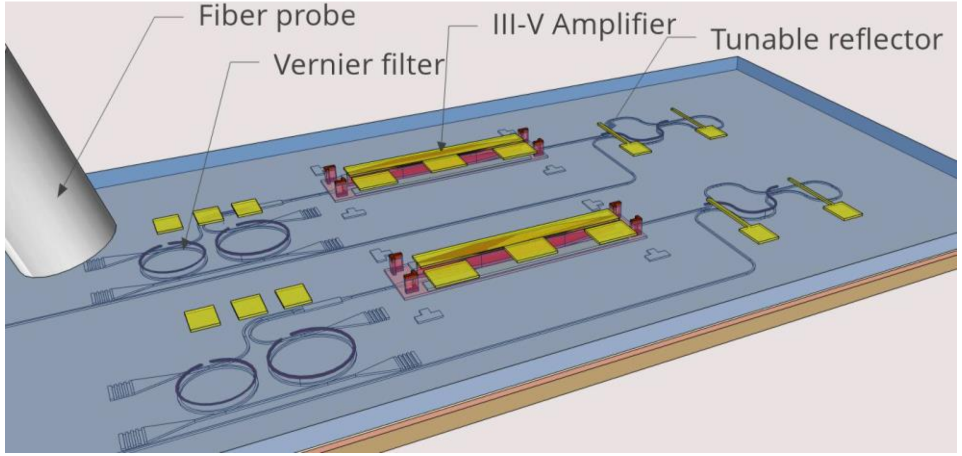
Very short tapers

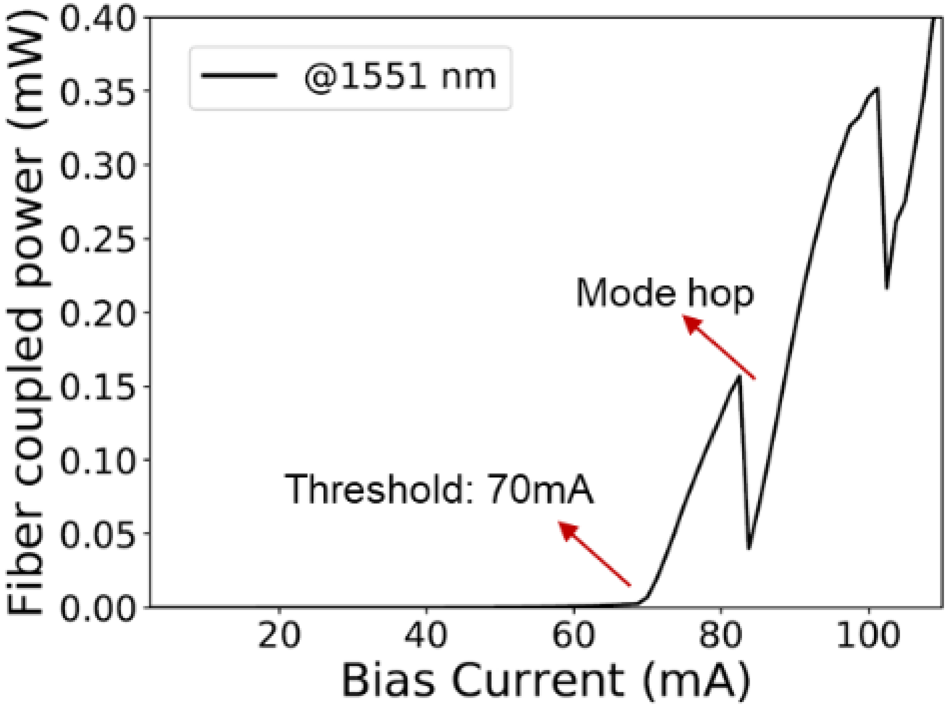
Longer tapers

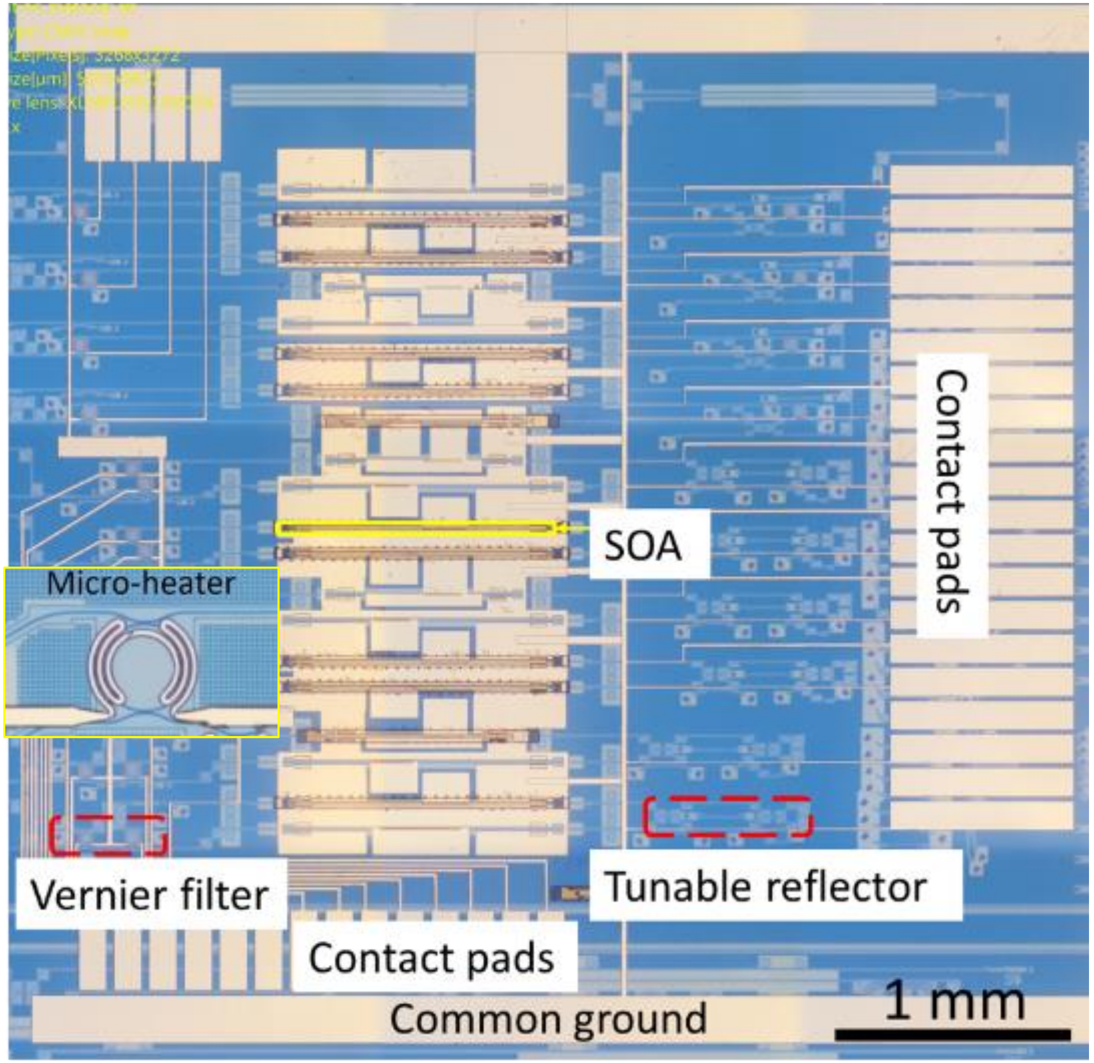
III-V-ON-SI INTEGRATED WIDELY TUNABLE LASER



III-V-ON-SI INTEGRATED WIDELY TUNABLE LASER

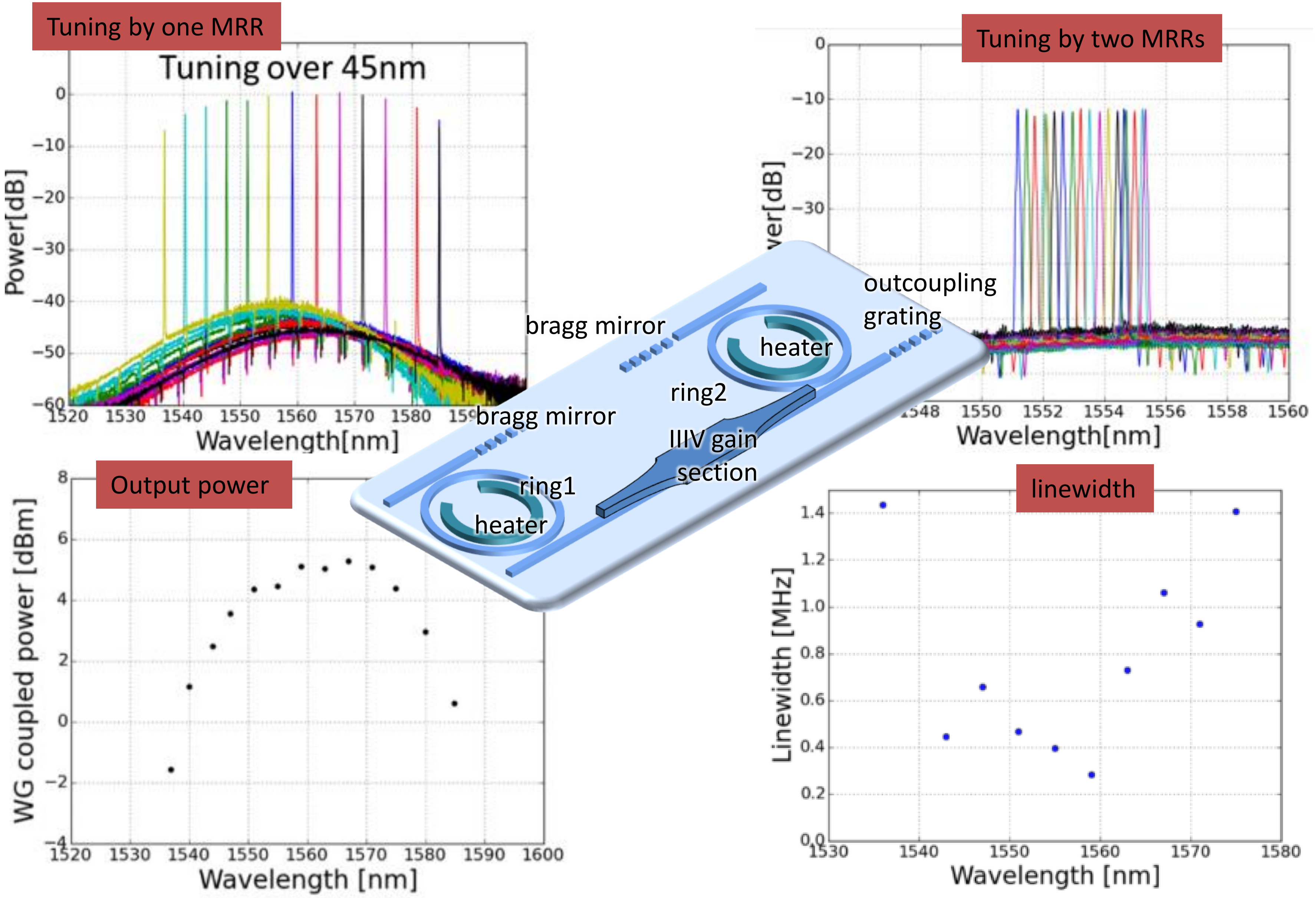






[J. Zhang et al., IEEE ECOC, 2019]

III-V-ON-SI INTEGRATED WIDELY TUNABLE LASER



Tuning by one MRR

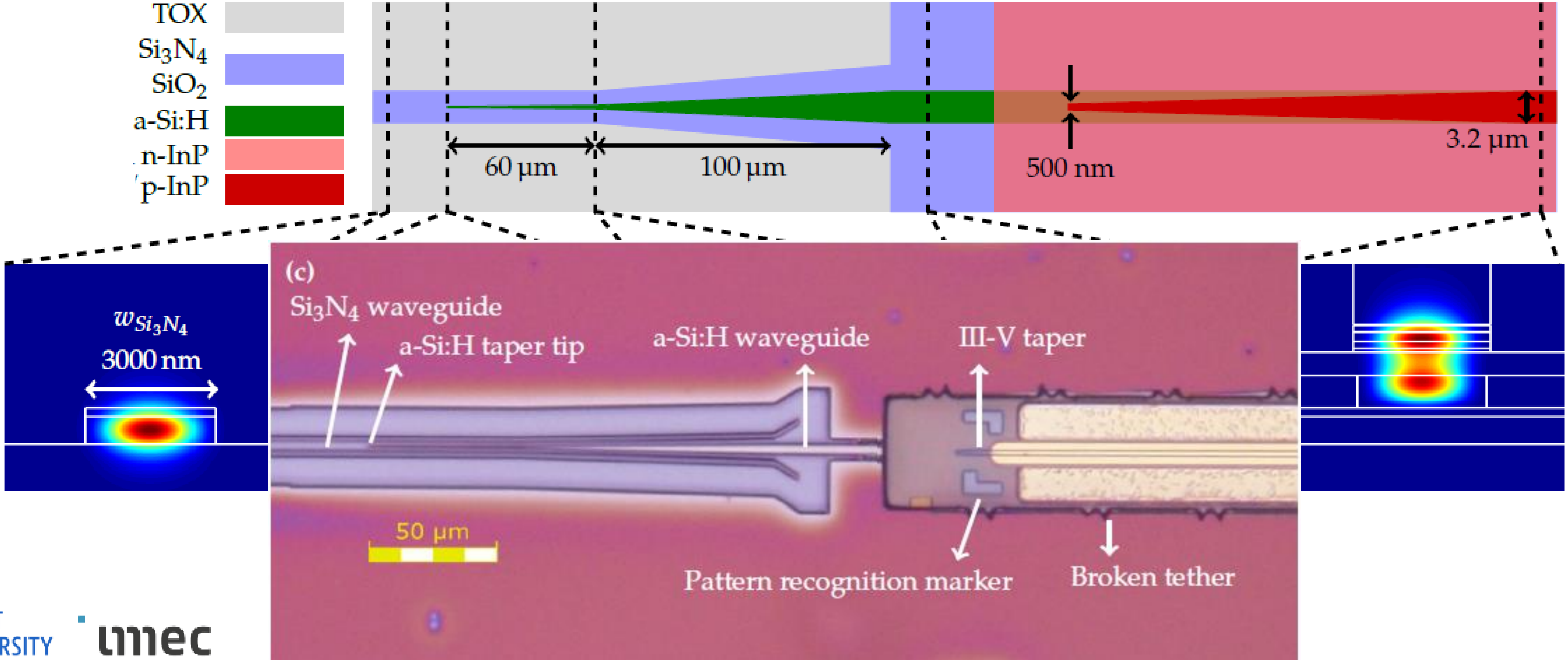
Tuning by two MRRs

Output power

linewidth

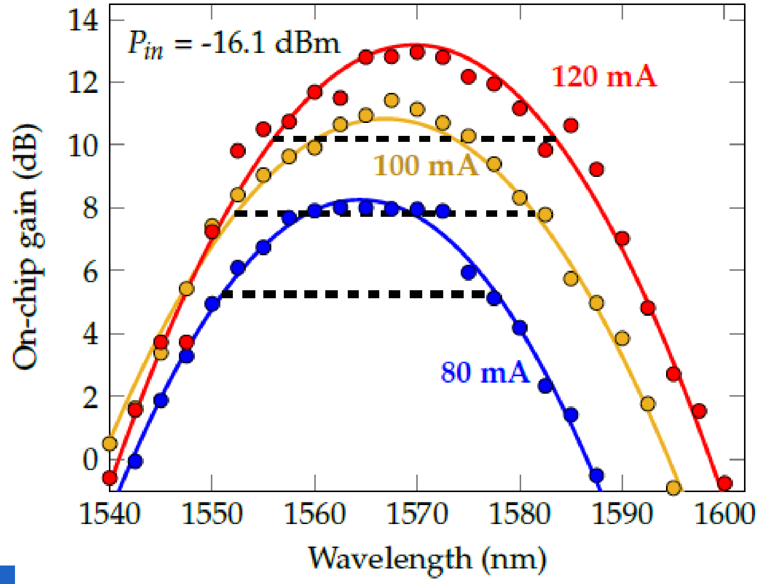
INTEGRATION OF AMPLIFIERS AND LASERS ON SILICON NITRIDE

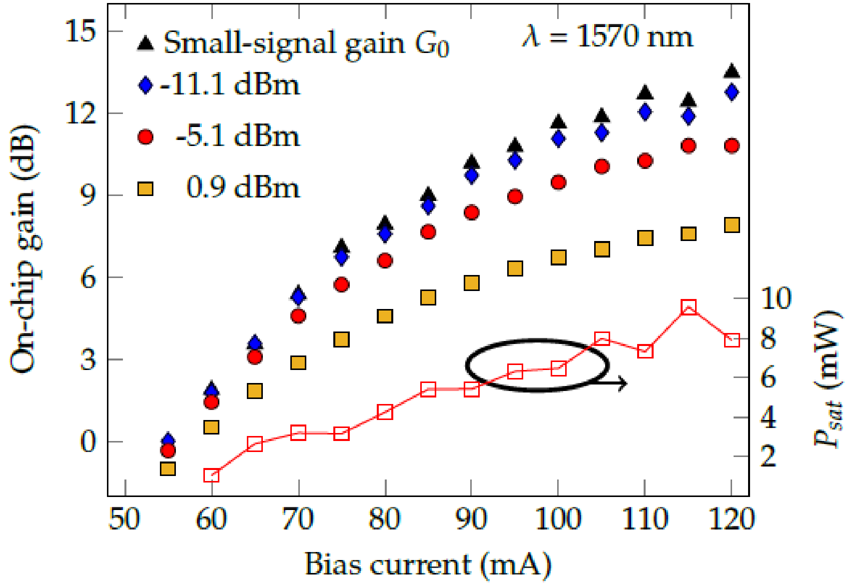
- Why: low loss, broader wavelength range
- Non-trivial given large index mismatch between InP and SiN
- Solution: intermediate amorphous silicon layer layer



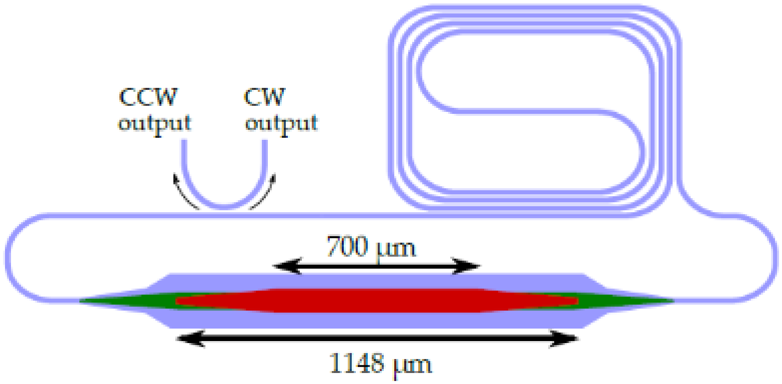
INTEGRATION OF AMPLIFIERS AND LASERS ON SILICON NITRIDE

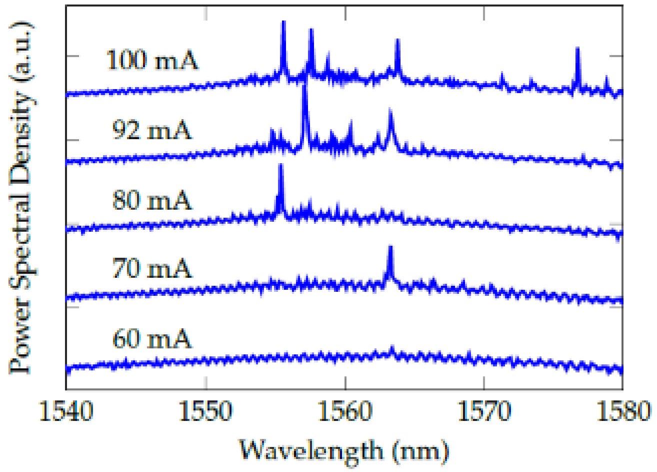
On-chip Gain

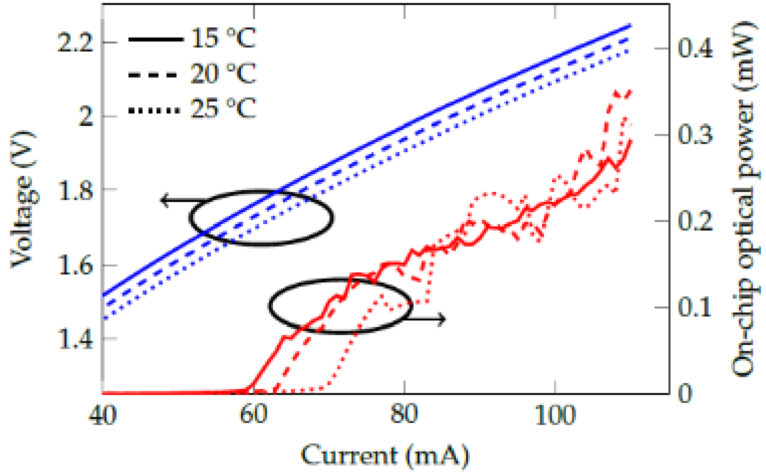




Ring-Laser

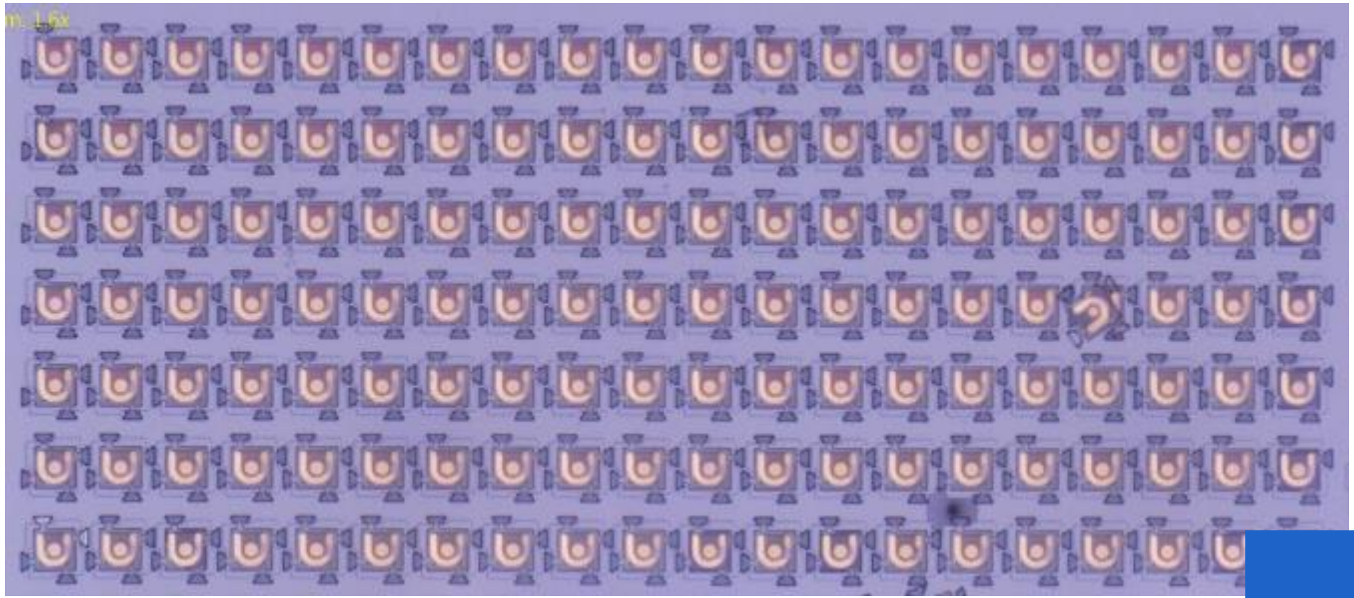


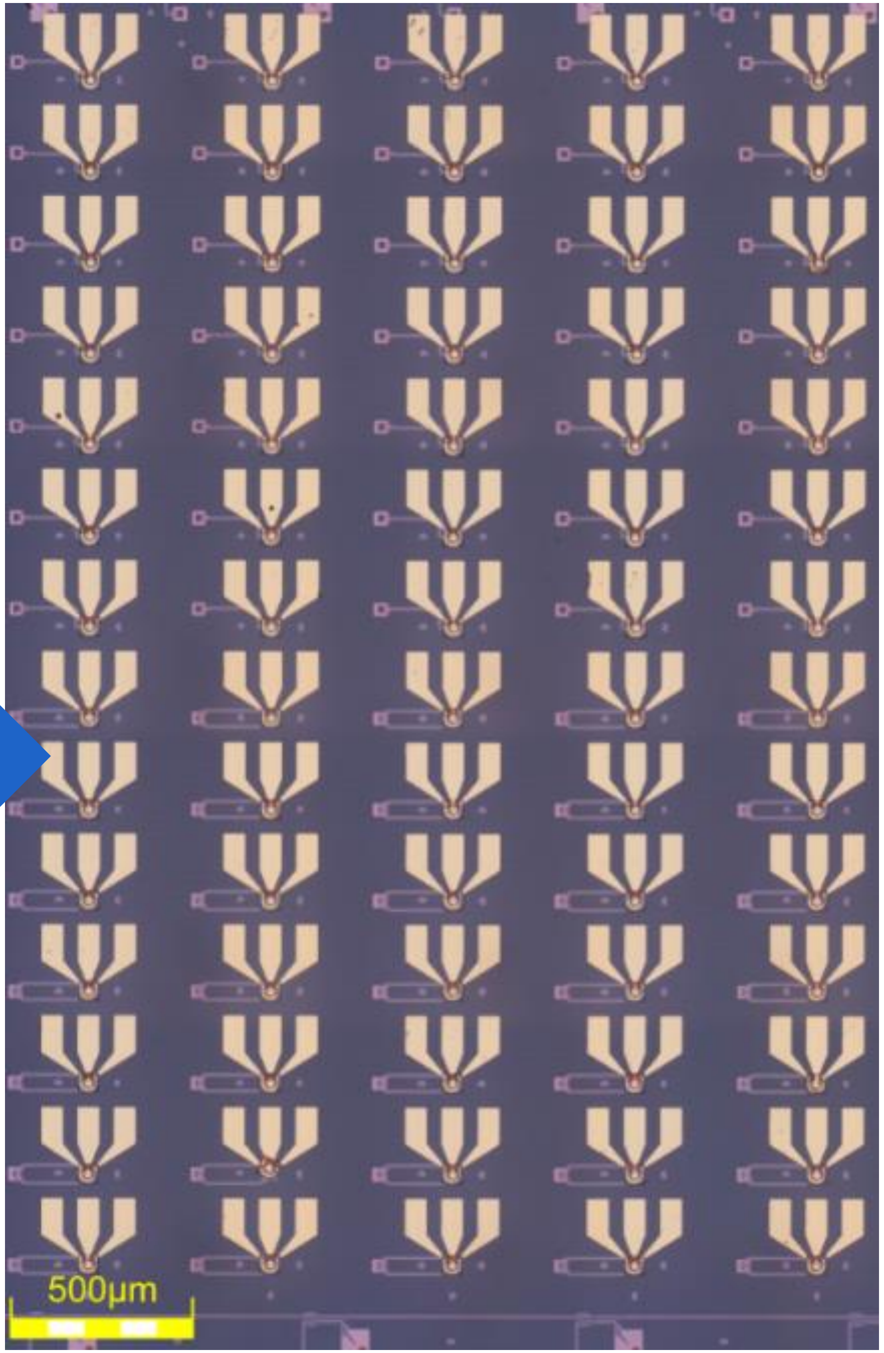




C. Op de Beeck, accepted for Optica

Printing Arrays of C-band PDs

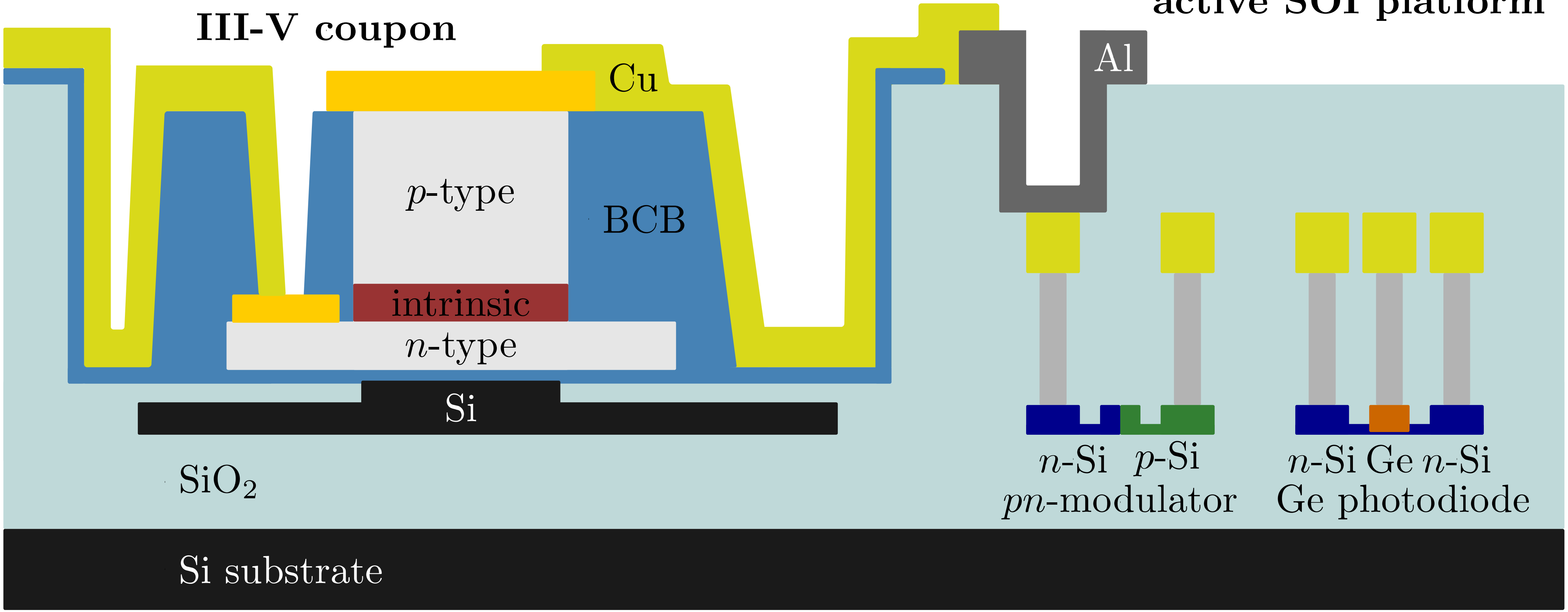




83/84 successful prints

Good device uniformity

CALADAN: INTEGRATION ON FULL PLATFORM



SUMMARY

Heterogeneous integration is key to enabling new functionalities in silicon photonics

Broad diversity of heterogeneous material combinations and technologies in research

Adding heterogeneous integration to a complete process flow is non-trivial

Micro-transfer-printing has high potential in view of its agility and combination of “best-in-class” technologies

5th ePIXfab Silicon Photonic Summer School
Ghent University (Belgium)

DATE : 15 – 19 June 2020

KEY FEATURES

- Learn all about silicon photonics: from technology to applications
- Geared towards industrial and academic participants
- A perfect blend of learning and networking

MORE INFO:

e-mail: info@ePIXfab.eu
web: https://epixfab.eu/trainings/upcoming-trainings

4th ePIXfab Silicon Photonic Design Course

DATE : 8 – 12 June 2020

KEY FEATURES

- 5 days hands-on silicon photonics design
- Layout, circuit simulation, design rules,
- Have your design fabricated and measured

: Promoting silicon photonics science, technology, and applications

PHOTONICS RESEARCH GROUP

Roel Baets

E roel.baets@ugent.be

T +32 496 559975

@PhotonicsUGent

www.photonics.intec.ugent.be

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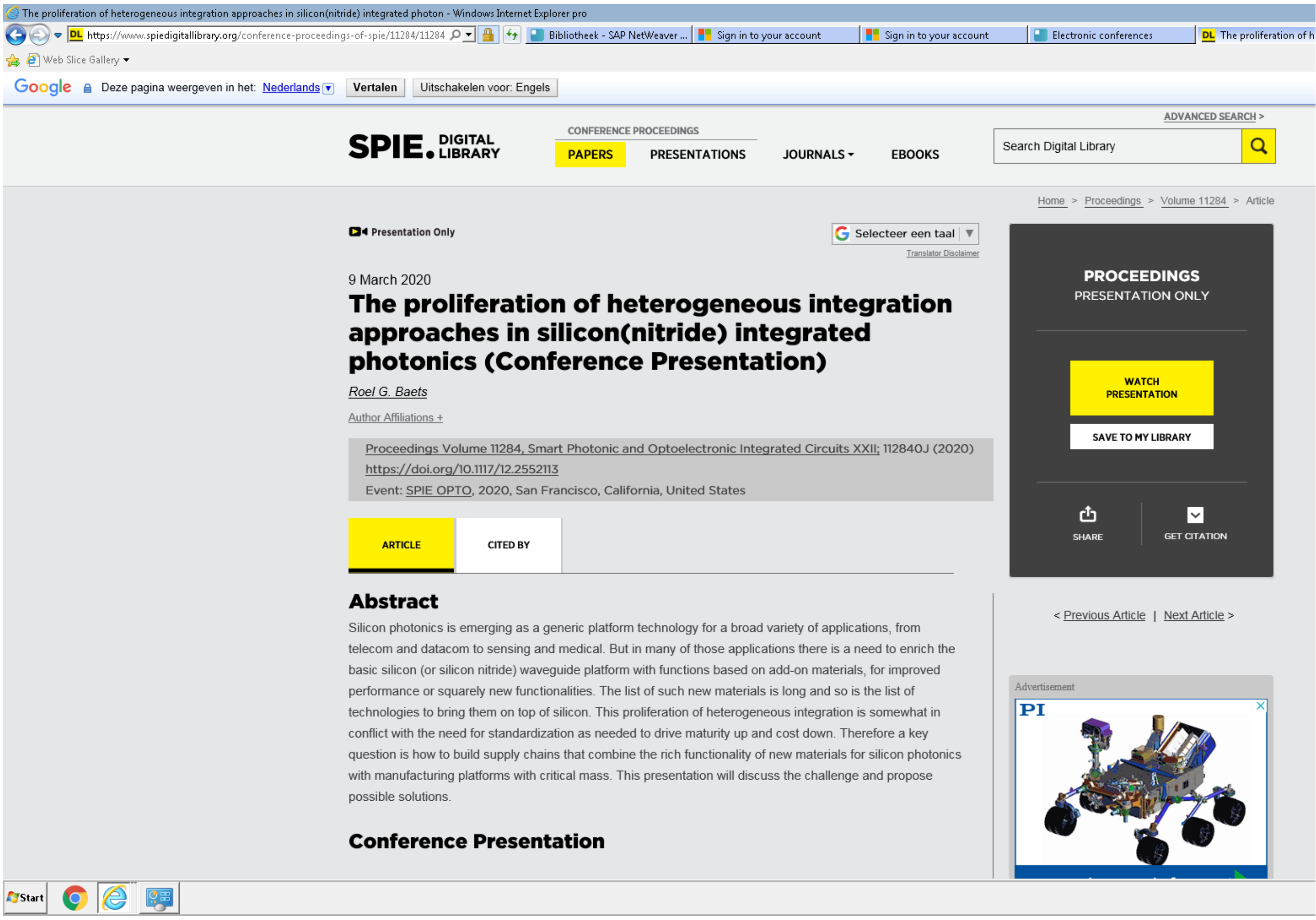

9 March 2020

The proliferation of heterogeneous integration approaches in silicon(nitride) integrated photonics (Conference Presentation)

Roel G. Baets

Author Affiliations +

Proceedings Volume 11284, Smart Photonic and Optoelectronic Integrated Circuits XXII; 112840J (2020)
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Abstract

Silicon photonics is emerging as a generic platform technology for a broad variety of applications, from telecom and datacom to sensing and medical. But in many of those applications there is a need to enrich the basic silicon (or silicon nitride) waveguide platform with functions based on add-on materials, for improved performance or squarely new functionalities. The list of such new materials is long and so is the list of technologies to bring them on top of silicon. This proliferation of heterogeneous integration is somewhat in conflict with the need for standardization as needed to drive maturity up and cost down. Therefore a key question is how to build supply chains that combine the rich functionality of new materials for silicon photonics with manufacturing platforms with critical mass. This presentation will discuss the challenge and propose possible solutions.

Conference Presentation