

# A Hybrid Integration Strategy for Compact, Broadband, and Highly Efficient Millimeter-Wave On-Chip Antennas

Quinten Van den Brande<sup>1</sup>, Student Member, IEEE, Sam Lemey<sup>2</sup>, Member, IEEE, Stijn Cuyvers, Stijn Poelman, Lars De Brabander, Olivier Caytan<sup>3</sup>, Member, IEEE, Laurens Bogaert, Igor Lima De Paula, Steven Verstuyft, Ad C. F. Reniers<sup>4</sup>, Bart Smolders<sup>4</sup>, Senior Member, IEEE, Bart Kuyken, Dries Vande Ginste<sup>5</sup>, Senior Member, IEEE, and Hendrik Rogier<sup>6</sup>, Senior Member, IEEE

**Abstract**—A novel hybrid integration strategy for compact, broadband, and highly efficient millimeter-wave (mmWave) on-chip antennas is demonstrated by realizing a hybrid on-chip antenna, operating in the [27.5–29.5] GHz band. A cavity-backed stacked patch antenna is implemented on a 600  $\mu\text{m}$  thick silicon substrate by using air-filled substrate-integrated-waveguide technology. A hybrid on-chip approach is adopted in which the antenna feed and an air-filled cavity are integrated on-chip, and the stacked patch configuration is implemented on a high-frequency printed circuit board (PCB) laminate that supports the chip. A prototype of the hybrid on-chip antenna is validated, demonstrating an impedance bandwidth of 3.7 GHz. In free-space conditions, a bore-sight gain of 7.3 dBi and a front-to-back ratio of 20.3 dB at 28.5 GHz are achieved. Moreover, the antenna is fabricated using standard silicon fabrication techniques and features a total antenna efficiency above 90% in the targeted frequency band of operation. The high performance, in combination with the compact antenna footprint of  $0.49 \lambda_{\text{min}} \times 0.49 \lambda_{\text{min}}$ , makes it an ideal building block to construct broadband antenna arrays with a broad steering range.

**Index Terms**—Air-filled substrate integrated waveguide (AFSIW), broadband, high efficiency, millimeter-wave (mmWave), on-chip antenna.

## I. INTRODUCTION

AS WE embark on the road to the fifth generation of network technology (5G), countless challenges and opportunities

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Q. Van den Brande, S. Lemey, L. De Brabander, O. Caytan, I. Lima de Paula, D. Vande Ginste, and H. Rogier are with Electromagnetics Group, Department of INTEC IDLab, Ghent University, IMEC, 9052 Gent, Belgium (e-mail: quinten.vandenbrande@ugent.be; sam.lemey@ugent.be; lars.debrabander@ugent.be; Olivier.Caytan@ugent.be; igor.limadepaula@ugent.be; Dries.VandeGinste@UGent.be; hendrik.rogier@ugent.be).

S. Cuyvers, S. Poelman, L. Bogaert, S. Verstuyft, and B. Kuyken are with Photonic Research Group, Department of INTEC, Ghent University, IMEC, 9052 Gent, Belgium (e-mail: stijn.cuyvers@ugent.be; Stijn.Poelman@UGent.be; Laurens.Bogaert@ugent.be; steven.verstuyft@ugent.be; bart.kuyken@ugent.be).

A. C. F. Reniers and B. Smolders are with the Electromagnetics Group, Department of Electrical Engineering, Eindhoven University of Technology, TU Eindhoven, Eindhoven 5612 AZ, Netherlands (e-mail: a.reniers@tue.nl; a.b.smolders@tue.nl).

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emerge. To address the prime objectives of 5G, radical improvements are needed in the cellular network architecture [1]. Given that the cellular bands below 6 GHz cannot support the exponentially increasing demands, a key enabler to realize 5G is millimeter-wave (mmWave) communication. As such, 5G is likely to utilize much higher frequencies, up to mmWave and beyond [2]. On the one hand, one of the major challenges in implementing mmWave communication is overcoming the unfavorable propagation characteristics [3]. To conquer this hurdle, multiantenna systems with adaptive beamforming will be indispensable [4], [5]. On the other hand, the exploitation of mmWave frequencies gives rise to smaller antenna footprints. This facilitates highly integrated radio units containing both the RF front end and the antenna, thereby improving reliability and mitigating large interconnect losses [6]–[13]. In the literature, two main strategies can be identified to realize these highly integrated RF solutions: antenna-on-chip (AoC) and antenna-in-package (AiP). Although both strategies are very promising, several critical issues remain. On the one hand, AoC solutions typically suffer from unfavorable electromagnetic material properties of bulk silicon substrates, resulting in poor antenna performance and substantial surface wave excitation [9]. On the other hand, AiP integration strategies face increased interconnect losses. These become more pronounced as the frequency of operation increases [9] and may be reduced by using a flip-chip technology [11]. However, the inductive nature of the interconnects may lead to narrowband performance [13]. Furthermore, in both integration strategies, utmost care should be taken to prevent electromagnetic interference (EMI) issues, due to inadequate shielding of the RF front end [9].

In this letter, a novel hybrid integration strategy for compact, broadband, and highly efficient mmWave on-chip antennas is demonstrated by realizing a highly efficient hybrid on-chip antenna, operating in the [27.5–29.5] GHz band. A cavity-backed stacked patch antenna topology is selected and implemented in air-filled substrate-integrated-waveguide (AFSIW) technology. In order to achieve unprecedented overall AoC/AiP performance, a hybrid on-chip approach is adopted by implementing the antenna feed and a metallized air-filled cavity on-chip and the stacked patch configuration on a Rogers RO4350B laminate supporting the chip. The fabricated hybrid on-chip antenna exhibits a measured  $-10$  dB bandwidth of 3.7 GHz, a maximal gain of 7.3 dBi at 28.5 GHz and a total antenna efficiency larger than 90% in the complete [27.5–29.5] GHz frequency

band. Moreover, by leveraging a stacked-patch configuration, an antenna footprint of only  $5.0 \text{ mm} \times 5.0 \text{ mm}$  is obtained. Furthermore, a high isolation between the antenna and both the RF front end and neighboring antennas is achieved by metallizing the air-filled cavity, thereby reducing EMI issues [9] and detrimental mutual coupling effects in antenna arrays [13], [14].

Many attempts to increase antenna efficiency have been described in the literature, both for AoC [15]–[25] and AiP strategies [11], [13], [19]. Considering AoC strategies, micromachined patch antennas have been a popular antenna topology [8], [16], [17], [20]–[22], [26], achieving antenna efficiencies up to 95%. However, these techniques usually result in an enlarged antenna footprint. Furthermore, high levels of mutual coupling [17] and/or susceptibility to EMI issues [15] were present due to lack of metallization of the micromachined cavities. Other micromachined topologies have been reported as well [15], [18], [19], achieving equivalent radiation performance. Yet, the aforementioned issues remain. Another common radiation enhancement technique is superstrate focusing [23]–[25], enabling easy integration with  $0.13 \text{ }\mu\text{m}$  SiGe or CMOS RF front ends. However, the highest reported antenna efficiency is limited to 50%. In conclusion, the AoC strategy typically leads to a constant tradeoff between antenna efficiency, bandwidth, and antenna footprint. In this respect, the AiP strategy allows achieving high antenna efficiencies within a small antenna footprint [11], [13], [19]. However, interconnects still remain an obstacle for AiP strategies [9] and, as such, hybrid integration strategies have been proposed to combine the best of both integration strategies, yielding high-performance integrated antennas [10], [12]. Compared to [10] and [12], our hybrid integration strategy reconciles the conflicting demands of high radiation efficiency, large bandwidth, small footprint, and low interconnect losses by implementing the antenna feed and a metallized air-filled cavity on-chip and exploiting the RF printed circuit board (PCB) laminate that supports the chip for the implementation of a stacked-patch configuration. Furthermore, the use of AFSIW technology strongly reduces EMI issues, commonly encountered in AoC and AiP designs. The proposed hybrid integration strategy is validated by realizing a novel on-chip antenna. Its measured performance is compared with the current state of the art in Table I, proving its excellent performance in terms of bandwidth, antenna efficiency, and antenna footprint.

The remainder of this letter is organized as follows. In Section II, the hybrid on-chip antenna topology is proposed and the design evolution is discussed. Section III elaborates on the fabrication process and the relevant manufacturing tolerances. Simulation and measurement results are discussed in Section IV.

## II. COMPACT AND HIGHLY EFFICIENT HYBRID ON-CHIP STACKED PATCH ANTENNA

A linearly polarized, highly integrated antenna on silicon is designed for operation in the  $[27.5\text{--}29.5]$  GHz band, targeting an antenna footprint smaller than  $5.450 \text{ mm} \times 5.450 \text{ mm}$  ( $0.54 \lambda_{\text{min}} \times 0.54 \lambda_{\text{min}}$ , with  $\lambda_{\text{min}}$  the free-space wavelength at  $29.5 \text{ GHz}$ ) for grating-lobe-free beam steering up to  $\theta = \pm 60^\circ$ . Moreover, an antenna efficiency over 90% is imposed in the complete bandwidth. Finally, a fabrication procedure that guarantees compatibility with CMOS and microelectromechanical systems (MEMS) processes and, thus, allows mass production and scalability to even higher frequencies

TABLE I  
COMPARISON OF CURRENT WORK TO THE STATE OF THE ART

	Technique	f [GHz]	BW [%]	$\eta$ [%]	A [ $\lambda \times \lambda$ ]
[17]	$\mu$ Machining	135.0	8.90	80.0	$0.81 \times 0.81$
[18]	$\mu$ Machining	60.0	11.80	90.0	$0.61 \times 0.95$
[19]	$\mu$ Machining	143.0	13.90	76.0	$0.95 \times 0.95$
[22]	$\mu$ Machining	34.5	4.00	95.0	$1.15 \times 1.15$
[24]	Superstrate	93.0	8.50	50.0	$0.70 \times 0.50$
[19]	AiP	143.0	6.90	89.0	$0.38 \times 0.38$
[11]	AiP	60.0	8.80	85.0	$2.60 \times 2.60$
[13]	AiP	29.0	5.00	N.A.	$0.23 \times 0.23$
[10]	Hybrid	60.0	12.60	73.0	$0.33 \times 0.16$
[12]	Hybrid	68.0	5.70	96.7	$0.16 \times 0.28$
<b>This</b>	<b>Hybrid</b>	<b>28.5</b>	<b>13.00</b>	<b>90.9</b>	<b><math>0.49 \times 0.49</math></b>

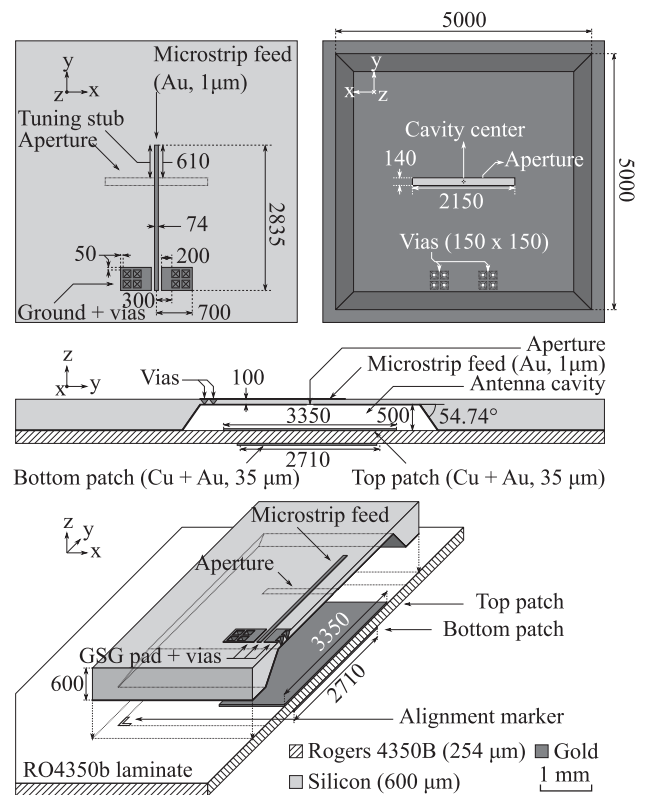


Fig. 1. Structure of the hybrid on-chip antenna (dimensions in micrometer). Top left: top view; top right: bottom view; middle: cross-sectional view; bottom: 3-D cross-sectional view. The rectangular top and bottom patch have dimensions  $3350 \text{ }\mu\text{m} \times 1800 \text{ }\mu\text{m}$  and  $2710 \text{ }\mu\text{m} \times 3080 \text{ }\mu\text{m}$ , respectively.

is strived for to remain competitive with current state-of-the-art solutions. To fulfill these stringent design requirements, a cavity-backed stacked patch antenna topology is adopted, as shown in Fig. 1. The backing cavity guarantees both a high antenna-to-integration platform isolation and reduces mutual coupling in arrays [14], while the stacked-patch configuration enables to satisfy the radiation and bandwidth requirements. To achieve the imposed total antenna efficiency, the antenna is implemented in AFSIW technology [27]–[29]. By removing the

silicon substrate underneath the stacked patches and plating the newly exposed silicon surface, an AFSIW cavity is created. As a result, the electromagnetic fields of the stacked patch antenna reside in an air substrate for the most part and, hence, a low-loss antenna performance is achieved over a large bandwidth and surface wave excitation is strongly suppressed. Furthermore, by exploiting mode bifurcation [29] in the stacked patch configuration, the antenna footprint of  $5.0 \text{ mm} \times 5.0 \text{ mm}$  remains below  $0.54 \lambda_{\text{min}} \times 0.54 \lambda_{\text{min}}$ , despite the use of AFSIW technology. As can be seen in Fig. 1, a hybrid on-chip antenna strategy is adopted. The antenna is constructed partially on-chip and partially on a high-frequency PCB laminate, where the parts that need the highest accuracy are developed in silicon, making use of micro- and nanoscale fabrication technologies. The antenna cavity and feed structure are created in and on a  $610 \mu\text{m}$  thick silicon wafer ( $\epsilon_r = 11.9$ ,  $\tan \delta = 0.0013$ ), respectively, whereas the patches are implemented on a  $254 \mu\text{m}$  thick Rogers RO4350B laminate ( $\epsilon_r = 3.66$ ,  $\tan \delta = 0.0031$ ), subsequently bonded to the silicon wafer with a nonconductive glue. On the one hand, the antenna feed structure is fabricated on-chip, making it compatible with standard silicon fabrication processes and, thus, the implementation of the RF front end can be both fully electrical [6], [7] or an opto-electrical hybrid [30], [31]. On the other hand, suspending the stacked-patch configuration on a Rogers RO4350B laminate allows a radiation performance equivalent to AiP antennas, without frequency-dependent interconnect losses. As such, our hybrid on-chip antenna approach minimizes interconnect losses and alleviates the tradeoff between bandwidth, efficiency, and antenna footprint.

A  $200 \mu\text{m}$  pitch ground-signal-ground (GSG) pad is used to enable antenna characterization with a probe, via a microstrip feed that excites the antenna by means of aperture coupling. Tuning the antenna feed dimensions, being the rectangular aperture and the tuning stub (see Fig. 1), allows for an optimization of the front-to-back ratio while still maintaining sufficient bandwidth. Moreover, leveraging aperture coupling provides adequate shielding between the antenna and feeding network, significantly mitigates parasitic radiation, and benefits radiation pattern purity. Note that the metallic traces on silicon are composed of gold and have a thickness of  $1 \mu\text{m}$ , whereas the patches on the Rogers RO4350B laminate are gold-plated copper traces and have a thickness of  $35 \mu\text{m}$ . Both patches and the aperture in the cavity are centered around the cavity center. Furthermore, as the antenna cavity and vias are created with a low-cost potassium hydroxide (KOH) wet etch process, they exhibit sloped edges with a fixed angle of  $54.74^\circ$ , as discussed in more detail in Section III. This is due to the (100) crystalline orientation of the silicon wafer. The proposed antenna is designed using the frequency domain solver of CST Microwave Studio. Its final dimensions are shown in Fig. 1.

### III. FABRICATION PROCESS

The antenna is fabricated in the clean room facility of Ghent University. It is fully compatible with standard silicon fabrication processes, making it low-cost and suitable for mass production. A high-resistivity (100) silicon substrate is used with a thickness of  $600 \mu\text{m}$  and a reported resistivity of  $40 \Omega\text{cm}$ . The substrate is undoped, double-sided polished, and contains a thin silicon oxide ( $\text{SiO}_2$ ) layer of  $400 \text{ nm}$  on both sides. Using a chemical vapor deposition process, a  $600 \text{ nm}$  thick silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer is deposited on both sides of the silicon wafer [see

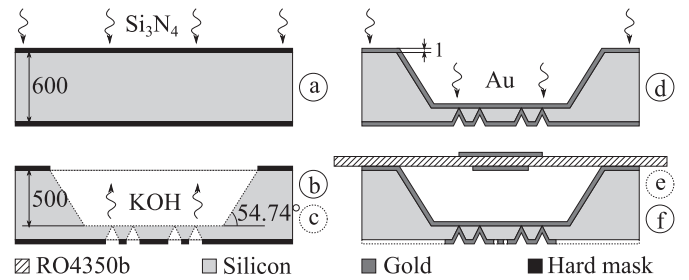


Fig. 2. An overview of the fabrication process (dimensions in  $\mu\text{m}$ ): (a) hard mask deposition, (b) hard mask patterning, (c) wet etch, (d) gold deposition, (e) gold patterning and (f) bonding.

Fig. 2(a) to realize a hard mask for the wet etch. Next, the silicon wafer is cleaved into samples of  $20 \text{ mm} \times 20 \text{ mm}$ . The remainder of the processing is divided into the following steps: etching, metallization, and bonding.

First, the antenna cavity and vias, described in Section II, are etched into the silicon samples. Thereto, a thin layer of TI prime [32] is spin-coated onto the top side of the sample to promote adhesion of the photoresist in the next step. After the proper baking procedure, a  $4 \mu\text{m}$  thick TI 35E [33] photoresist layer is spin-coated on top of the TI prime layer and baked. Next, the SUSS MicroTec MA6/BA6 aligner is used to perform the photolithography step, where the image reversal technique [33] is adopted to pattern the photoresist. The Advanced Vacuum Vision 310 RIE is then used to transfer the pattern onto the hard mask with a plasma etching procedure, using a gas mixture of  $\text{SF}_6$  and  $\text{O}_2$ . However, first, a thin TI 35E photoresist layer is coated on the back side of the sample to protect it during the plasma etching step. The cavity pattern is now transferred onto the hard mask of the silicon sample [see Fig. 2(b)]. Next, the same procedure is used to transfer the via patterns onto the hard mask on the sample backside. To ensure accurate positioning of the vias, backside alignment (with an accuracy of  $\pm 600 \text{ nm}$ ) is performed with the cavity corners as a reference. Finally, a wet etch procedure is performed using a 20% KOH solution. The etching solution is heated to  $80^\circ\text{C}$ , resulting in a silicon etch rate of about  $1.7 \mu\text{m}/\text{min}$ . The samples are submerged in the solution for 295 min, until a cavity depth of  $500 \mu\text{m}$  is reached [see Fig. 2(c)]. Due to the (100) crystalline orientation of the silicon wafer, the edges are etched at an angle of  $54.74^\circ$  and, as such, the etching process of the vias stops automatically after the tip of its pyramidal shape is reached [see Fig. 2(c)]. After completing the etching process, a small portion of the cavity is punctured by the vias on the other side of the silicon sample. Finally, the remainder of the hard mask is removed using a hydrofluoric acid (HF) solution.

In the second step, gold (Au) is deposited and patterned on both sides of the chip. First, a  $10 \text{ nm}$  layer of titanium (Ti) is pre-deposited on the sample backside by means of sputtering to act as an adhesive layer between the Si and Au. Afterward, sputtering is applied to deposit a  $1 \mu\text{m}$  thick layer of Au [see Fig. 2(d)]. Next, an  $8.8 \mu\text{m}$  thick layer of AZ9260 positive resist [34] is applied to pattern the metal on the backside of the silicon sample during the photolithography step. After developing the sample in a 1:2 AZ400K [35] water solution, the feed structure of the antenna is finished [see Fig. 2(e)]. Next, the same procedure is performed for the top side of the sample to create the metal cavity and



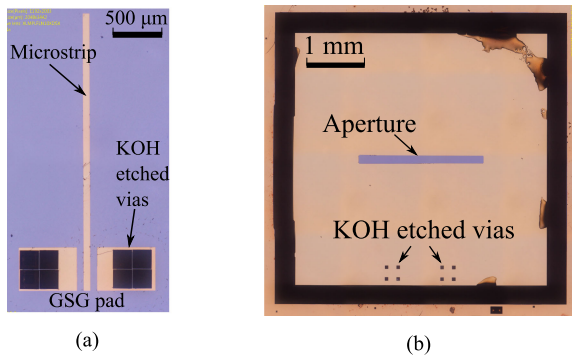


Fig. 3. (a) Feed structure with GSG pad and (b) etched cavity with aperture of the on-chip stacked patch antenna.

the feeding aperture. Backside alignment is again performed to guarantee accurate alignment of the different antenna features. A fabricated on-chip antenna prototype is shown in Fig. 3.

In the final step, the metallized silicon sample is bonded to an RO4350B laminate, supporting a stacked patch structure. To this end, a 9  $\mu\text{m}$  thick layer of Cyclotene 3022-57 [36] is spin-coated on the substrate. By using the alignment markers on the superstrate (see Fig. 1), the chip and PCB laminate are aligned by means of a Finetech Pick and Place bonder (with an accuracy of  $\pm 1 \mu\text{m}$ ). After alignment, the chip and substrate are pressed together while being heated to 150  $^{\circ}\text{C}$ . After a heating period of 20 min, the antenna is finished [see Fig. 2(f)]. A fabricated on-chip antenna prototype is shown in Fig. 3. Note that, in future array configurations, some excess silicon can be placed at the edges of the chip to provide sufficient bonding surface between the superstrate and chip.

#### IV. SIMULATION AND MEASUREMENT RESULTS

The reflection coefficient and far-field performance of the antenna prototypes are measured in the mmWave Anechoic Chamber [37] at Eindhoven University of Technology (TUE). This fully automated system, with a 1 m diameter and a 0.5 m height, is equipped with a probing setup that allows both backside and frontside probing and is operational up to 90 GHz. In this letter, backside probing is performed using a GSG-200 Picoprobe and a Keysight N5247A PNA-X Microwave Network Analyzer for both the reflection coefficient and far-field measurements. A SOLT calibration is performed to measure the scattering parameters of two prototypes, making use of a CS-5 calibration substrate [38]. For measurement purposes, the patch-supporting RO4350B laminate is sized 4 cm  $\times$  4 cm. The excess RO4350B laminate is used to install the antenna inside the anechoic chamber on top of a Rohacell ( $\epsilon_r = 1.05$ ,  $\tan \delta = 0.0034$ ) antenna mount.

The simulated and measured  $|S_{11}|$  w.r.t. 50  $\Omega$  of the hybrid on-chip antenna and the prototypes are shown in Fig. 4. Two resonance peaks are visible because of the two stacked patches, resulting in a measured and simulated bandwidth of 3.7 and 3.1 GHz, respectively. A good agreement between simulated and measured radiation patterns (co- and cross-polarization) in the  $yz$  and  $xz$  planes at 28.5 GHz can be seen in Fig. 5. A simulated boresight gain of 6.64, 7.27, and 7.38 dBi is achieved at 27.5, 28.5, and 29.5 GHz, respectively. The corresponding measured gain is 6.62, 7.08, and 7.12 dBi, respectively. This results in a

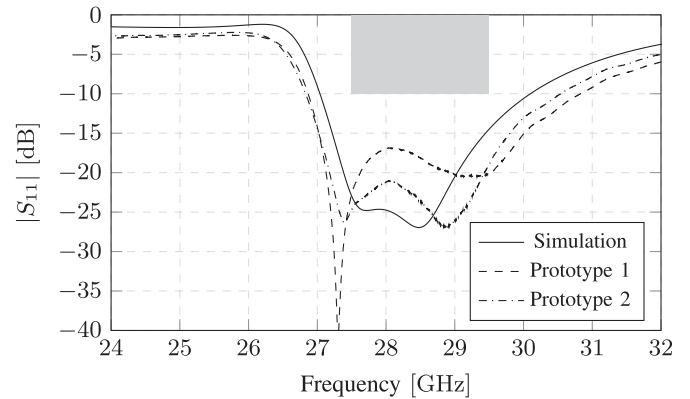


Fig. 4. Simulated and measured magnitude of the reflection coefficient ( $|S_{11}|$ ) w.r.t. 50  $\Omega$ .

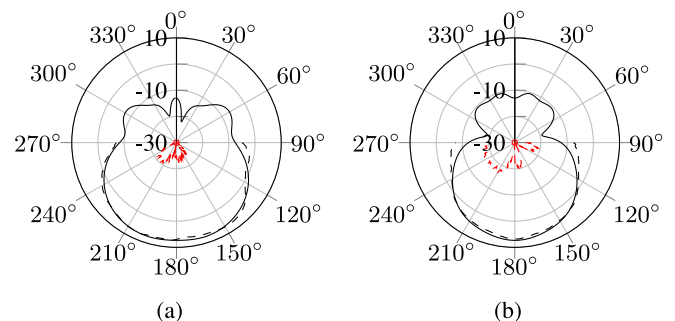


Fig. 5. Simulated (solid) and measured (dashed), copolarized (black) and cross-polarized (red) antenna gain at 28.5 GHz. (a)  $yz$  plane (E-plane), (b)  $xz$  plane (H-plane).

total antenna efficiency of 92.7%, 90.9%, and 90.4% at those frequencies. Furthermore, a front-to-back ratio of 20.3 dB is obtained at the center frequency, and an axial ratio over 20 dB within the 3 dB beamwidth of over 65 $^{\circ}$  in both planes is realized. Table I compares the proposed hybrid on-chip antenna with the state of the art in terms of fractional bandwidth (BW), antenna efficiency ( $\eta$ ), and antenna footprint ( $A$ ). The antenna footprint is expressed in a fraction of the wavelength at the highest frequency of operation. It can be seen that the presented antenna enables excellent performance with respect to the state of the art when considering the combination of bandwidth, efficiency, and antenna footprint.

#### V. CONCLUSION

A novel hybrid integration strategy for mmWave antennas is demonstrated by realizing an on-chip AFSIW cavity-backed stacked patch antenna, featuring excellent performance in terms of radiation efficiency, broadside gain, and bandwidth. Measurements report a total antenna efficiency over 90%, a minimal boresight gain of 6.6 dBi, and sufficient bandwidth to cover the [27.5–29.5] GHz band. Moreover, the compact antenna footprint (5.0 mm  $\times$  5.0 mm) in combination with the large beamwidth ( $> 65^{\circ}$ ) and high antenna-to-integration platform isolation makes the proposed antenna element an attractive building block for multiantenna systems with beam-steering capabilities.

## REFERENCES

- [1] A. Gupta and R. K. Jha, "A survey of 5G network: Architecture and emerging technologies," *IEEE Access*, vol. 3, pp. 1206–1232, 2015.
- [2] Z. Pi, J. Choi, and R. Heath, "Millimeter-wave gigabit broadband evolution toward 5G: Fixed access and backhaul," *IEEE Commun. Mag.*, vol. 54, no. 4, pp. 138–144, Apr. 2016.
- [3] T. S. Rappaport, G. R. MacCartney, M. K. Samimi, and S. Sun, "Wideband millimeter-wave propagation measurements and channel models for future wireless communication system design," *IEEE Trans. Commun.*, vol. 63, no. 9, pp. 3029–3056, Sep. 2015.
- [4] T. Cameron, "5G—The microwave perspective," *Analog Devices*, Norwood, MA, USA, Tech. Rep., 2015.
- [5] M. Y. Frankel, P. J. Matthews, and R. D. Esman, "Practical optical beamforming networks," *Opt. Quantum Electron.*, vol. 30, pp. 1033–1050, 1998.
- [6] W. Shin, B. Ku, O. Inac, Y. Ou, and G. M. Rebeiz, "A 108–114 GHz  $4 \times 4$  wafer-scale phased array transmitter with high-efficiency on-chip antennas," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2041–2055, Sep. 2013.
- [7] B. Ku, O. Inac, M. Chang, H. Yang, and G. M. Rebeiz, "A high-linearity 76–85-GHz 16-element 8-transmit/8-receive phased-array chip with high isolation and flip-chip packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2337–2356, Oct. 2014.
- [8] Y. Liu, A. Agrawal, and A. Natarajan, "Millimeter-wave IC-antenna cointegration for integrated transmitters and receivers," *IEEE Antennas Wireless Propag. Lett.*, vol. 15, pp. 1848–1852, 2016.
- [9] Y. P. Zhang and D. Liu, "Antenna-on-chip and antenna-in-package solutions to highly integrated millimeter-wave devices for wireless communications," *IEEE Trans. Antennas Propag.*, vol. 57, no. 10, pp. 2830–2841, Oct. 2009.
- [10] J. A. Z. Luna, L. Dussopt, and A. Siligaris, "Hybrid on-chip/in-package integrated antennas for millimeter-wave short-range communications," *IEEE Trans. Antennas Propag.*, vol. 61, no. 11, pp. 5377–5384, Nov. 2013.
- [11] Y. P. Zhang, M. Sun, D. Liu, and Y. Lu, "Dual grid array antennas in a thin-profile package for flip-chip interconnection to highly integrated 60-GHz radios," *IEEE Trans. Antennas Propag.*, vol. 59, no. 4, pp. 1191–1199, Apr. 2011.
- [12] Y. Song *et al.*, "A hybrid integrated high-gain antenna with an on-chip radiator backed by off-chip ground for system-on-chip applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 1, pp. 114–122, Jan. 2017.
- [13] H. Kim *et al.*, "A 28-GHz CMOS direct conversion transceiver with packaged  $2 \times 4$  antenna array for 5G cellular system," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, May 2018.
- [14] Y. Li and K. Luk, "60-GHz substrate integrated waveguide fed cavity-backed aperture-coupled microstrip patch antenna arrays," *IEEE Trans. Antennas Propag.*, vol. 63, no. 3, pp. 1075–1085, Mar. 2015.
- [15] E. Ojefors, H. Kratz, K. Grenier, R. Plana, and A. Rydberg, "Micromachined loop antennas on low resistivity silicon substrates," *IEEE Trans. Antennas Propag.*, vol. 54, no. 12, pp. 3593–3601, Dec. 2006.
- [16] G. P. Gauthier, J. Raskin, L. P. B. Katehi, and G. M. Rebeiz, "A 94-GHz aperture-coupled micromachined microstrip antenna," *IEEE Trans. Antennas Propag.*, vol. 47, no. 12, pp. 1761–1766, Dec. 1999.
- [17] H. Chu, Y. Guo, T. Lim, Y. M. Khoo, and X. Shi, "135-GHz micromachined on-chip antenna and antenna array," *IEEE Trans. Antennas Propag.*, vol. 60, no. 10, pp. 4582–4588, Oct. 2012.
- [18] P. Liu, L. Chang, Y. Li, Z. Zhang, S. Wang, and Z. Feng, "A millimeter-wave micromachined air-filled slot antenna fed by patch," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 10, pp. 1683–1690, Oct. 2017.
- [19] W. T. Khan *et al.*, "A D-band micromachined end-fire antenna in 130-nm SiGe BiCMOS technology," *IEEE Trans. Antennas Propag.*, vol. 63, no. 6, pp. 2449–2459, Jun. 2015.
- [20] Y. Koga *et al.*, "Cavity-backed MEMS patch antennas on double-layer silicon wafers," in *Proc. IEEE Antennas Propag. Soc. Int. Symp.*, Jul. 2006, pp. 3935–3938.
- [21] I. Papapolymerou, R. F. Drayton, and L. P. B. Katehi, "Micromachined patch antennas," *IEEE Trans. Antennas Propag.*, vol. 46, no. 2, pp. 275–283, Feb. 1998.
- [22] V. K. Singh, "Ka-band micromachined microstrip patch antenna," *Microw. Antennas Propag.*, vol. 4, pp. 316–323, Mar. 2010.
- [23] Y. Ou and G. M. Rebeiz, "On-chip slot-ring and high-gain horn antennas for millimeter-wave wafer-scale silicon systems," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 1963–1972, Aug. 2011.
- [24] Y. Ou and G. M. Rebeiz, "Differential microstrip and slot-ring antennas for millimeter-wave silicon systems," *IEEE Trans. Antennas Propag.*, vol. 60, no. 6, pp. 2611–2619, Jun. 2012.
- [25] J. M. Edwards and G. M. Rebeiz, "High-efficiency elliptical slot antennas with quartz superstrates for silicon RFICs," *IEEE Trans. Antennas Propag.*, vol. 60, no. 11, pp. 5010–5020, Nov. 2012.
- [26] M. Komulainen *et al.*, "Embedded air cavity backed microstrip antenna on an LTCC substrate," *J. Eur. Ceramic Soc.*, vol. 27, no. 8, pp. 2881–2885, 2007.
- [27] A. Ghiotto, F. Parment, T. P. Vuong, and K. Wu, "Millimeter-wave air-filled SIW antipodal linearly tapered slot antenna," *IEEE Antennas Wireless Propag. Lett.*, vol. 16, pp. 768–771, 2017.
- [28] F. Parment, A. Ghiotto, T. P. Vuong, J. M. Duchamp, and K. Wu, "Millimetre-wave air-filled substrate integrated waveguide slot array antenna," *Electron. Lett.*, vol. 53, no. 11, pp. 704–706, 2017.
- [29] Q. Van den Brande, S. Lemey, J. Vanfleteren, and H. Rogier, "Highly-efficient impulse-radio ultra-wideband cavity-backed slot antenna in stacked air-filled substrate-integrated-waveguide technology," *IEEE Trans. Antennas Propag.*, vol. 66, no. 5, pp. 2199–2209, May 2018.
- [30] A. O. Boryszenko, J. Liao, J. Zeng, S. Deng, V. M. Joyner, and Z. R. Huang, "Radio-optical dual-mode communication modules integrated with planar antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 2, pp. 403–410, Feb. 2010.
- [31] O. Caytan *et al.*, "Passive opto-antenna as downlink remote antenna unit for radio frequency over fiber," *J. Lightw. Technol.*, vol. 36, no. 19, pp. 4445–4459, Oct. 2018.
- [32] MicroChemicals GmbH, *TI PRIME adhesion promotor*, Technical datasheet, Ulm, Germany, Aug. 2002.
- [33] MicroChemicals GmbH, *TI 35E image reversal resist*, Technical datasheet, Ulm, Germany, Aug. 2016.
- [34] MicroChemicals GmbH, *AZ9200 Photoresist, High-Resolution Thick Resist*, Technical datasheet, Ulm, Germany, 1997.
- [35] MicroChemicals GmbH, *AZ400K*, Technical datasheet, Ulm, Germany, 2005.
- [36] DOW, *CYCLOTENE 3000 Series Advanced Electronic Resins*, Technical datasheet, Midland, MI, USA, Feb. 2005.
- [37] A. C. F. Reniers, Q. Liu, M. H. A. J. Herben, and A. B. Smolders, "Review of the accuracy and precision of mm-wave antenna simulations and measurements," in *Proc. 10th Eur. Conf. Antennas Propag.*, Apr. 2016, pp. 1–5.
- [38] Picoprobe GGB Industries, *Calibration Substrates*, Technical datasheet, Naples, FL, USA, 2002.