An enhanced architecture for silicon photonic reservoir computing

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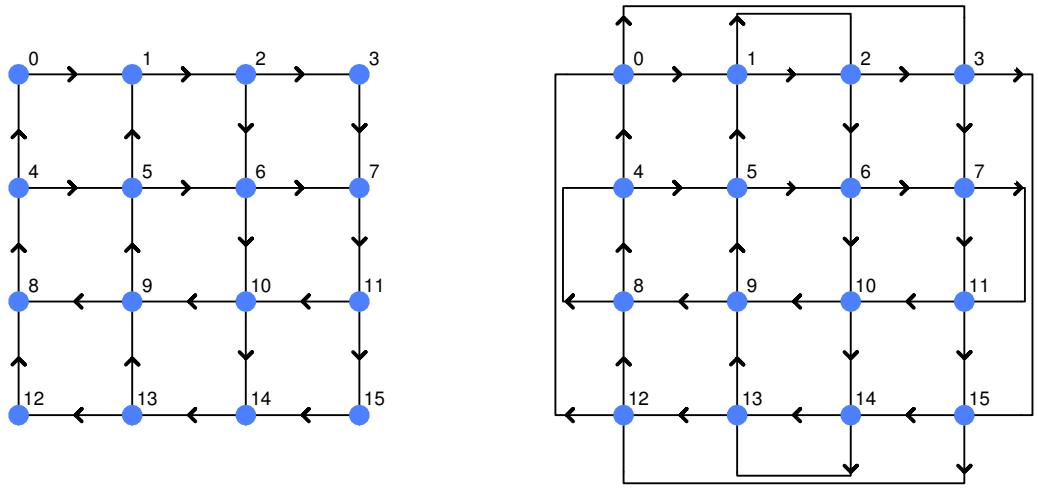
Summary. Reservoir computing is a neuromorphic computing paradigm which is well suited for hardware implementations. In this work, an enhanced reservoir architecture is introduced as to lower the losses and enhance mixing behaviour in silicon photonic reservoir computing designs.

Reservoir computing is a machine learning technique in which a nonlinear dynamical system is used for computation. it was originally implemented as an efficient way to train a neural network [1] but it has grown to a commonly used method for classification and regression tasks. The dynamical system, also called the reservoir, is held unchanged during the procedure and during training, only the weights used to linearly combine the reservoir states are optimized. Keeping the recurrent network unchanged and only training on the level of the reservoir states makes reservoir computing a computationally cheap method.

Although reservoir computing was originally invented in computer science as a software solution to bypass the computational cost of optimizing a neural network, it is perfectly suited to be implemented in various hardware platforms. These implementations do not suffer from classical digital computer bottlenecks and are by nature more convenient to operate neuromorphic computing schemes. One such hardware implementation that is especially suited for reservoir computing is silicon photonics. Silicon photonics is a CMOS-compatible platform in which waveguides, splitters and combiners are used to guide light through a silicon chip. It has the advantages of being compact, inexpensive to produce in high volumes and having a mature fabrication process. For reservoir computing, an additional advantage that comes costless is that the computation happens in the optical domain, which improves the reservoir richmess as each signal is in essence two-dimensional. Optics also supports much higher bandwidths than electronics and in principle, one can exploit many nonlinear processes in photonics.

Until now, silicon photonic reservoir computing approaches typically employ the swirl architecture [2, 3] as initially defined in [4] and illustrated in figure 1a. Even though it indeed introduces the necessary dynamics, there is still room for improvements in terms of losses and mixing. Concerning losses, the swirl architecture fundamentally suffers from modal radiation losses at each 2×1 combiner (for example node 7). These losses are inherent for non-symmetrical reciprocal splitting devices as on average there is a 50% modal mismatch between the two input channels. In terms of mixing, some nodes are partially withdrawn from the dynamics, only consisting of one input and one output (the corner nodes). In general, the most interesting behaviour in swirl reservoirs will be at the inside, by definition of the architecture, while it could be beneficial to also bring the outer layers more into play.

In this paper, we present a new architecture, the four-port architecture, which reduces the problems concerning excessive losses by avoiding 2×1 devices and employing 2×2 devices exclusively instead as illustrated in Figure 1b. It is compared with the swirl architecture in simulations in terms of loss and in terms of performance on the equalization of a nonlinearly distorted BPSK signal.



(a) Swirl architecture

(b) Four-port architecture

Figure 1: Silicon photonic reservoirs on a conceptual level.

These simulations show that the four-port architecture indeed suffers less losses and thus has a better energy-efficiency as all input power at a node is redirected to one of the two output channels instead of radiating away. Not only does this avoid undesired losses, but this strategy also contributes to a more uniform power distribution and additional mixing between states which were topologically far apart in the swirl architecture by exploiting extra output ports of the 2×2 devices in an smart way. A better power uniformity does not only increase the richness of the dynamics, it also facilitates measuring the states in an eventual chip as more nodes will be measurable above a certain threshold.

Consequently, the four-port architecture was designed which, in terms of losses and in terms of connectivity within the reservoir, finds itself superior to the swirl architecture.

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