Effect of fabrication imperfections on the performance of silicon-on-insulator arrayed waveguide gratings

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We discuss and analyze the effect of fabrication imperfections on the performance of silicon arrayed waveguide gratings, using an extensive experimental parameter sweep combined with dedicated AWG simulation tools.

Introduction

Silicon photonics has become a prominent technology for photonic integrated circuits for many applications ranging from optical communications to sensing. This success can be attributed to two main factors i.e. use of the existing *complementary metal oxide semiconductor* (CMOS) infrastructure and the high material index contrast of the *silicon-on-insulator* (SOI) material stack, which permits submicron waveguides and high integration density. However, high index contrast makes the devices very susceptible to geometry variations, which degrades device performance, and rapidly impact yield of larger circuits.

In this research, we discuss the effect of fabrication imperfections on the performance of the *arrayed waveguide gratings* (AWG) devices after providing an insight into the fabrication variability, backed up with experimental results.

Fabrication Variability

Fabrication variability is present at different levels for integrated photonics e.g. lot-to-lot, wafer-to-wafer, die-to-die and device-to-device. Different process conditions like exposure dose, plasma density, resist age and *chemical mechanical polishing* (CMP) slurry composition lead to variations in the linewidth, layer thickness, sidewall angles and doping profile variation. These variations in the geometry affect optical properties of a device such as its effective index, group index, coupling coefficients and center wavelength. Changes in optical properties of the individual devices propagate to the circuit level and increase the insertion loss, cross-talk, noise figures and power consumption. Variability can be explained with the example of the simplest photonic component: a waveguide. A silicon wire waveguide is very sensitive to change in linewidth and thickness. The effective and the group indices change as the geometry of the waveguide changes. This change in indices can lead to phase errors in an interferometric device with multiple delay lines even when waveguides are placed close together. This variability comes from different processes during the fabrication and can have different distributions over the wafer. Process variability can be environmental, temporal or spatial. Environmental and the temporal variabilities are usually reflected at the wafer-to-wafer and lot-to-lot level so not considered here. The spatial variability is the core of this research as it affects the device performance and is dependent on the distance between devices or device's location on the wafer. Often, elements closer together are more likely to have less variability than the elements further apart.

Arrayed Waveguide Gratings and Variability

An AWG consists of an input star coupler, an array of waveguides and an output star coupler. AWGs are capable of separating different wavelength channels from a broadband input so are key devices for *wavelength division multiplexing* (WDM) systems. An example SOI-based 8-channel (400 GHz channel spacing) AWG and its transmission response are shown in Figure 1(a) below. Compact AWGs with good insertion loss and extinction ratio have already been demonstrated in a compact footprint taking advantage of the high index contrast provided by the SOI technology platform [1, 2]. As discussed above, this compactness comes at the expense of sensitivity to the fabrication imperfections [3, 4]. Especially the side wall roughness and the waveguide width variations are considered to be the main contributors in introducing the phase errors in the delay lines which result into enhanced cross-talk between the output channels of the AWGs.
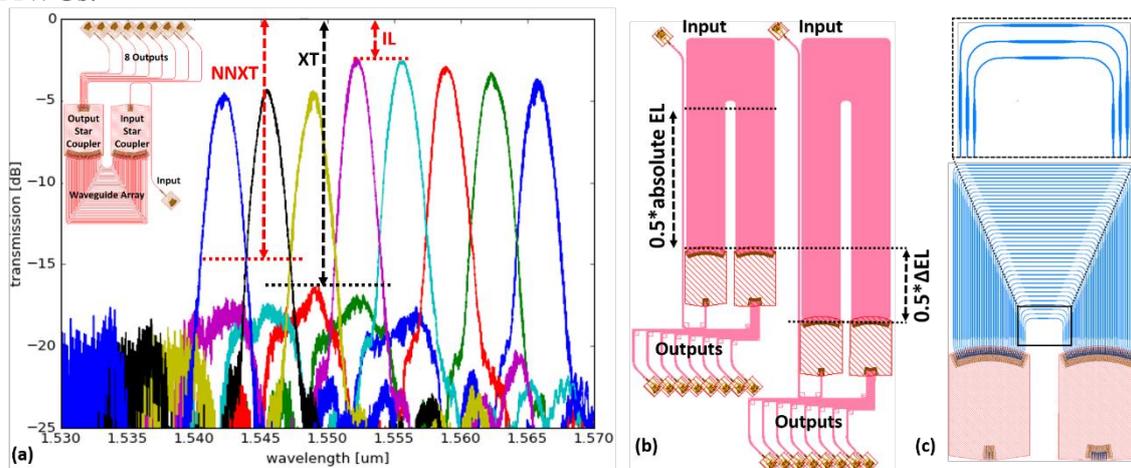
Figure 1 (a) Measured transmission response of a SOI based 8 channel 400 GHz AWG. Insertion loss (IL), cross-talk (XT) and next neighbout cross-talk (NNXT) are marked in the plot. The inset shows the layout of the device. (b) Designed 8 channel AWG devices with 800 μm and 1200 μm extra lengths. The absolute extra length for the 800μm AWG and the extra length between these two AWG devices are marked.(c) Designed 8 channel AWG with width of the waveguides increased to 1200 μm. It should be noticed that width of the waveguide around the bends is not increased to prevent mode conversions.

To analyze the effect of above mentioned fabrication imperfections we designed and fabricated variations of this 8 channel AWG with extra length in the delay lines (Figure 1(b)), as well as different waveguide widths in the delay lines (Figure 1(c)). In total, 19 variations for both length and the width of the delay lines were designed and fabricated. Design and simulation were performed with Luceda Photonics' dedicated filter toolbox algorithms, and fabrication using the IMEC iSiPP process through the Europractice *multi-project wafer* (MPW) service.

AWG devices having 7 different extra lengths ranging from 50 μm to 1200 μm were designed with width of the delay waveguides fixed at 0.45 μm to get a quantitative insight in the effect of phase errors and losses on the AWG performance. The additional length in all the arms does not affect the ideal behavior of the device, but will increase the effect of phase errors. The fabricated AWG devices with varying delay lines lengths over a wafer were measured using a tunable laser and a photodetector in a clean-room environment. The effect of the extra lengths on the *insertion loss* (IL), *cross-talk* (XT) and the *next neighbor cross-talk* (NNXT) is shown in Figure 2(a) below. It can be noticed in the graph that the extinction ratio decreases with increasing extra lengths in the delay lines. The two main factors here are the side wall roughness and the local variability.

Local variability results in varying waveguide width along the waveguides and between adjacent waveguides, causing a phase mismatch between the arms. The thickness of the waveguides is assumed to be constant for a device as thickness variation is a wafer level slowly varying phenomenon.

The widths of the delay lines were varied in total of 12 steps from 0.3 µm to 1.2 µm for AWGs having zero extra length (EL = 0 µm). The *insertion loss* (IL), *cross-talk* (XT) and the *nearest neighbor cross-talk* (NNXT) for the devices with varying width of the delay lines are shown in Figure 2(b). It can be noticed that the extinction ratio increases (cross-talk decreases) with increasing waveguide widths. The insets in Figure 2 (a) and (b) show the calculated fundamental TE modes for both 0.45 µm and 0.8 µm wide waveguides respectively. It can be noticed that less light interacts with the side walls for 0.8 µm waveguide so side wall roughness and changes in linewidth play a smaller role here. The insertion loss for AWGs with wider waveguide is reduced as scattering losses are lower for wider waveguides. So, local variabilities and the side wall roughness do not affect the performance as much and the cross-talk decrease with increasing width of the waveguide.
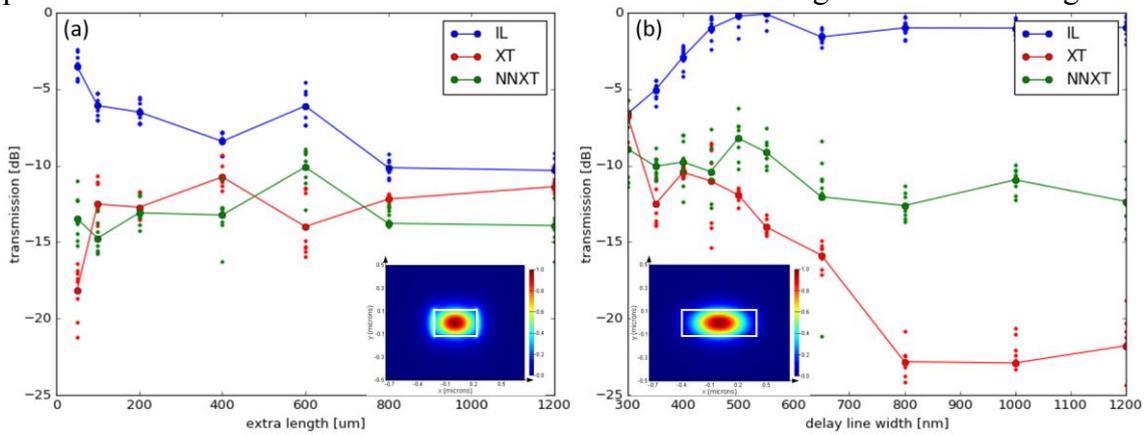
Figure 2 (a) Plot showing the change in insertio loss, cross-talk and the next neighbour cross-talks for different extra lengths of the 8 channel 400GHz AWG. The inset shows the fundamental TE mode for 0.45µm wide waveguide. (b) Plot showing the change in insertio loss, cross-talk and the next neighbour cross-talks for different delay line widths of the 8 channel 400GHz AWG. The inset shows the fundamental TE mode for 0.8µm wide waveguide.

The devices were measured over the wafer to find out the wafer level trends for the performance parameters like insertion loss, cross-talk, next neighbor cross-talk and the deviation from the designed wavelength. Wafer maps of performance parameters for devices with 50 µm extra length and 0.45 µm linewidth are shown in Figure 3 below. It can be noticed in Figure 3(a) that insertion loss is uniform over the wafer with some exceptions at the edges. Similar trends were observed for average channel cross-talks and next neighbor cross-talks which are shown in Figure 3(b) and Figure 3(c) respectively. It was found in our previous research [4] that linewidth is usually smaller while thickness is larger than the designed values at the edges of the wafer. So, it can be assumed that the linewidth change is somehow compensated by the increase in thickness. Some small islands can be observed in the cross-talk wafer map which can be attributed to the local die-level width variations as thickness is a wafer level phenomenon. The average channel wavelength deviation over the wafer is shown in Figure 3(d). It can be noticed that the deviation from the desired wavelength is minimum at the center of the wafer. The deviation increase towards the edges in an annular way. The thickness of the silicon layer also varies in a similar way due to the polishing effect, so this deviation can be largely attributed to the change in thickness of the silicon guiding layer.
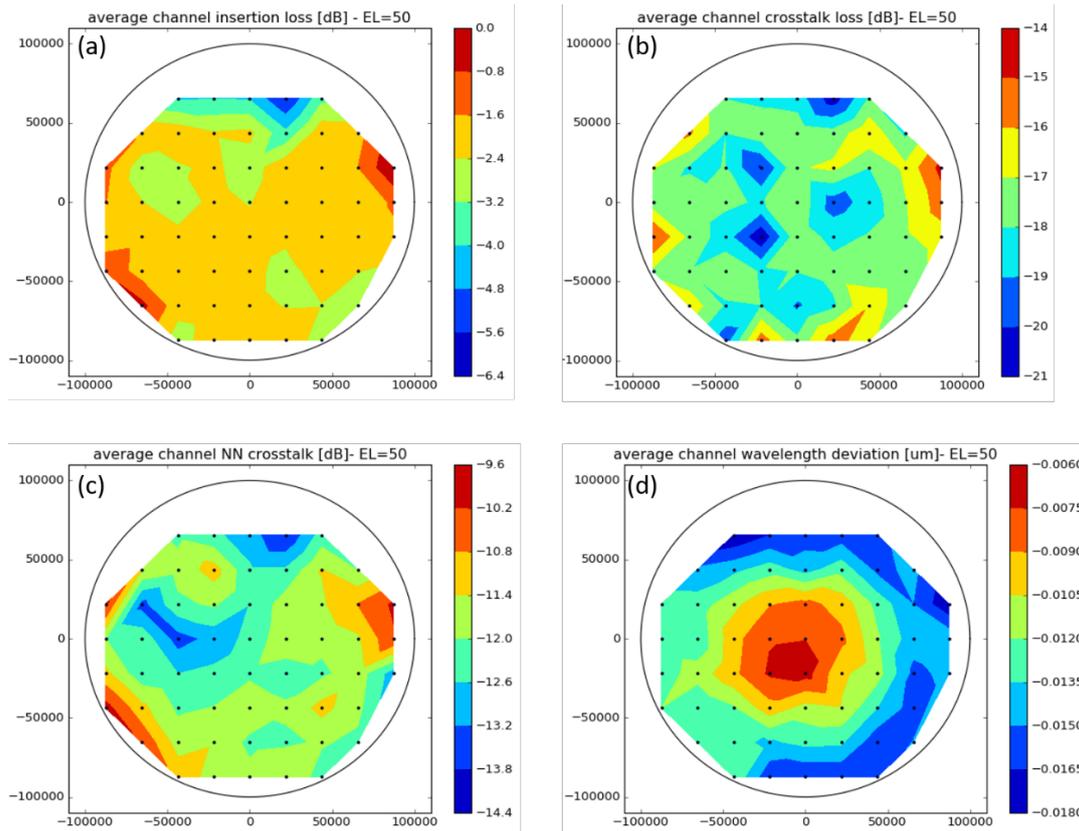
Figure 3 (a) A wafer map showing the average channel insertion loss for a 8 channel 400GHz AWG with an extra length of 50µm. (b) A wafer map showing the average channel cross-talk for a 8 channel 400GHz AWG with an extra length of 50µm. (c) A wafer map showing the average channel next neighbour cross-talk for a 8 channel 400GHz AWG with an extra length of 50µm. (d) A wafer map showing the average channel wavelength deviation from the desired value for a 8 channel 400GHz AWG with an extra length of 50µm.

Conclusions

We have collected experimental data on the behavior of silicon photonic AWGs under the influence of fabrication variation. The effect of delay line length is very pronounced, and we also see a confirmation that using wider waveguides in the delay lines is beneficial for the device performance.

Acknowledgements

References

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