From Parameter Extraction, Variability Models to Yield Prediction

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Abstract: We will discuss methods and workflow of variability analysis and yield prediction for integrated photonic circuits, describing the process from wafer-scale parameter extraction over spatial variability modelling to layout-aware yield prediction of photonic circuits.

OCIS codes: (130.3120) Integrated optics devices; (000.5490) Probability theory, stochastic processes, and statistics;(230.7370) Waveguides.

1. Introduction

Silicon photonics is maturing quickly to become more commercially viable. Its high material contrast facilitates tight light confinement and high-density integration, which enables photonic circuits with ever-increasing size, complexity and functionality. Meanwhile, high material contrast also makes silicon photonic circuit very susceptible to fabrication induced performance variations. For example, deviation from the designed waveguide geometry will severely shift the spectrum of a waveguide-based filter device. Device performance degradation propagates and accumulates to the circuit level and can rapidly decrease the yield of large circuits, i.e., the number of fabricated circuits working as intended. It will ultimately increase the cost of the delivered product and limit the capacity of a circuit. Predicting the performance variation becomes essential in a standardized design work flow to predict yield and estimate how to compensate degradation of the fabricated chip. [1] In integrated electronics, the yield can be assessed using corner analysis, which calculates best and worst cases under a fabrication variation. The definition of best or worst is often clear. Better corresponds to lower resistance, faster switching times, etc. However, it is less intuitive to define "better" for photonics building blocks using one parameter. For example, the effective index and coupling coefficients both affect the performance of wavelength filter, but they have no intrinsic good or bad values. It is the deviation from the designed value or the mismatch between values of components in the circuit that degrade the performance. [1] To predict the yield of photonics circuits, we can map variations of low-level behavior parameters (effective index, coupling coefficient) or fabricated geometry parameters (linewidth, thickness) to high-level circuit performance variations. By assigning location-aware variations that mimics the actual fabrication variation, we can derive the high-level circuit variations using Monte-Carlo simulations. This technique requires three pieces of information: an accurate collection of data on the fabricated wafer, a realistic variation model to separate systematic and random variations on different spatial levels, and a virtual fabrication wafer map based on extracted fabricated data to enable Monte-Carlo simulations. We will discuss our progress on these aspects to achieve yield prediction.

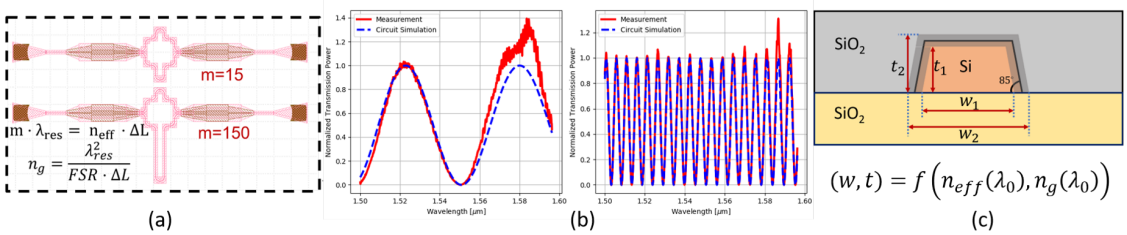

Fig. 1. (a) Two configurations of MZIs for parameter extraction. (b) Extract n_{eff} and n_g using the curve fitting method. (c) Map n_{eff} and n_g to width w and thickness t.

2. Parameter extraction using circuit models

Extracting compact model parameters of fabricated circuits is essential to get input data for performance evaluation [2] and variability analysis [3]. Extracting parameters is not trivial. For example, it is easy to calculate the effective index in a mode solver, but it is difficult to obtain it directly from the measurement. Therefore, we designed special test structures and included them in the chip design. For example, effective index and group index of the fabricated straight waveguide can be extracted using optical measurements of a *Mach-Zehnder interferometers* (MZI). To improve the extraction accuracy, we used curve fitting techniques. Also, we use two configurations of the MZI with different interference orders. The accuracy of extraction is improved particularly due to the reduced extraction bounds of effective index with the knowledge of accurate group index extracted from the higher order MZI. [4]

Extraction of the fabricated geometry is essential in mapping fabricated variations to circuit performance variations. However, metrology measurement of fabricated chip using a *scanning electron microscope* (SEM) or *atomic force microscope* (AFM) is either expensive, destructive or extremely time-consuming. The limited amount of metrology measurements offered by semiconductor fabs during process development are often not representatives for real fabricated devices. The accuracy of such measurement is not accurate enough for variability analysis. Alternatively, we use optical measurements to obtain behavior parameters from the fabricated device, then accurately map them to accurate geometry parameters. In [4] a numerically developed geometrical model linking the waveguide effective index and group index has been used to estimate waveguide geometry (width and height). The approach provides the sub-nanometer precision of geometry extraction for waveguide fabricated using a foundry process line, which helps to identify process variations and non-uniformity across the device layer.

3. Spatial variability model

To analyze the statistics of the parameters extracted from fabricated wafer and make use of it in the yield prediction, we require a variation model. The process-related parameter variation originates from sources at different spatial levels. [6] For example, wafer-level non-uniformity can come from layer thickness, photoresist spinning effects and plasma distributions, which varies slowly across the wafer and exhibits a symmetric radial pattern. Resources such as low-frequency change in layer thickness, local pattern density and error in the photomask lead to intra-die systematic variations. Besides, the model should also include random variations. Fluctuation in exposure dose and imaging focus add to the random die-to-die variation. Intrinsic randomness in layer thickness and waveguide sidewalls result in device-to-device random variation. Spatial variations from different levels have differed sources and relatively small

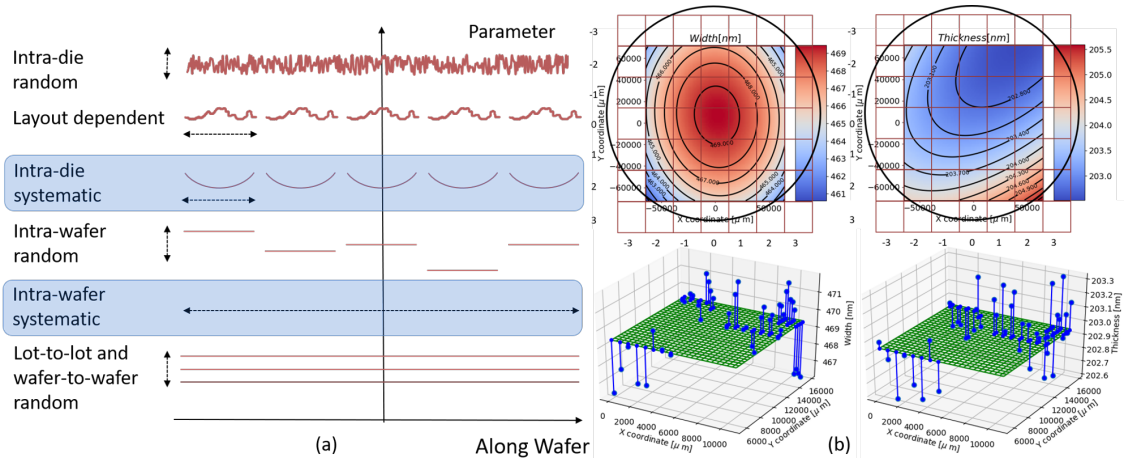

Fig. 2. (a) Illustration of decomposing spatial variability of device parameter at different levels. [6] (b) Top wafer maps of linewidth and thickness present the systematic intra-wafer variations under the process variation. Bottom wafer maps represent the systematic intra-die variations of linewidth and thickness.

interactions. So we decompose the total spatial variation into lot-to-lot, wafer-to-wafer, die-to-die and device-to-device variations with systematic and random components. We designed the workflow to obtain components of the additive hierarchical model (Fig. 2), which facilitates characterizing statistical data measured on-wafer. The waveguide thick-

ness we extracted [6] suffers significantly larger intra-wafer systematic variation (3.0 nm) than the intra-die systematic variation (0.7 nm), while linewidth has a intra-wafer systematic variation (8.5 nm) comparable with its intra-die systematic variation (5.0 nm).

4. Location-aware yield prediction

Waveguide-based filters are very sensitive to phase variations and coupling variations. Monte-Carlo simulations using simple random distributed parameters shows the sensitivity of the circuit. However, for yield prediction this is not realistic since it does not consider location-dependency of variations. For example, the intra-wafer linewidth variation with a symmetric radial pattern affects devices in the center and near the rim differently, which is not considered by the standard Monte-Carlo method. Also, devices located next to each other should be more correlated than placed further apart. To make realistic predictions, we incorporate information of the spatial variations into the Monte-Carlo method. We created a virtual fabrication map (linewidth, thickness) using the additive spatial variation model, which could be offered by the fab who can obtain it from wafer-scale optical measurements. In a circuit simulator as CAPHE, maps of global variations (e.g. linewidth and thickness deviations from the nominal value) can be 'projected' onto the actual layout of a circuit which is positioned on different wafer sites. [5] Knowing the sensitivity of parameters to geometry variations, we can propagate these variations to the circuit level and simulate the response. For example, we test the sensitivity of 4-channel demultiplexer circuit comprising 4 ring resonators. They are designed to drop a wavelength on a regular wavelength grid with 1.6 nm spacing. From Monte-Carlo circuit simulations, we found that demultiplexer shows significantly larger variation in channel spacing when the rings are placed further apart.

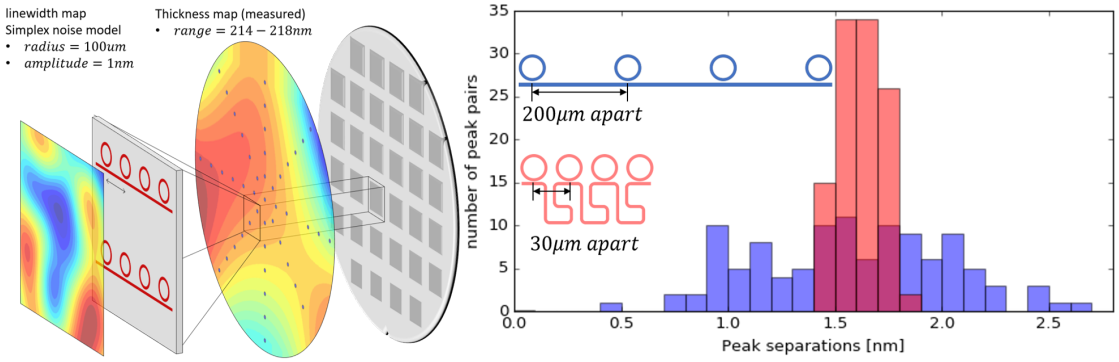

Fig. 3. (a) Generate maps of width and thickness deviation and placing ring demultiplexers over the selected points over the virtual wafer. (c) Channel spacing distribution of the demultiplexer with rings spaced 200μm apart (blue) and 30μm apart (red).

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