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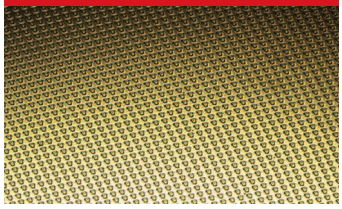
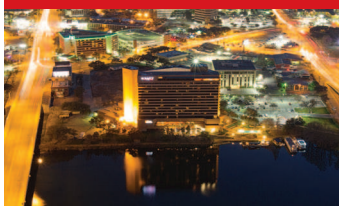


Making waves with the GaN HEMT



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AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

Viewpoint

By Dr Richard Stevenson, Editor

Lasing on the edge

WHEN RESEARCHERS develop a technology, they often do so with a product in mind. But there are times when things don't work out in the way they intended – and the technology ends up being used in a different manner.

That may well be the case for the technology that engineers at imec have developed to form high-quality III-Vs on a silicon substrate. When efforts started around a decade ago, the ultimate goal was the fabrication of compound semiconductor MOSFETs on silicon.

That effort is still underway, but more recently this III-V-on-silicon technology has also been used as a way to enable the growth of lasers on silicon. That's important, as improvements in the performance of silicon ICs are now under threat from on-chip and chip-to-chip data transfer rates, which are getting close to their limit. The solution is to switch from electrons to photons – hence the introduction of laser on silicon.

The researchers at imec are producing high-quality III-V material on silicon by a technique known as aspect ratio trapping. Defects are inevitable, due to the significant lattice-mismatch between the silicon and the III-Vs, but these imperfections are annihilated at the walls of the trench. What's more, by having a V-shape at the bottom of the trench, planes can be selected that prevent anti-phase domains – a destroyer of device performance.

By controlling the growth rates of the III-Vs on various facets, imec's engineers define the shape of the material that emerges

from the trench: it can be rectangular, triangular or hexagonal in nature (see imec's feature "Gaining an edge with nano-ridges" on p. 36 to discover the details of their craft).

imec's work on nano-ridge lasers is still in its infancy. So far, the team have produced optically pumped lasers on trenches with widths from 60 nm to 120 nm. By inserting a phase-shift grating, a single-mode emission peak is ensured.

One of the next goals will surely be the progression from optically pumped to electrically pumped lasers. Given the dimensions, success will not be easy. But imec has a great track record in innovation, so I, for one, am optimistic.

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Gaining an edge with nano-ridges

Aspect ratio trapping enables the fabrication of nano-ridge lasers on silicon substrates

BY BERNARDETTE KUNERT, ROBERT LANGER, MARIANNA PANTOUVAKI AND JORIS VAN CAMPENHOUT FROM IMEC AND DRIES VAN THOURHOUT FROM GHENT UNIVERSITY

MAINTAINING the march of Moore's law is getting more and more difficult. In recent times, it has required the introduction of novel geometries and esoteric materials, such as hafnium dioxide. And in the years that lie ahead, progress may hinge on the use of III-Vs – either as a material for adding on-chip RF-functionalities, or for providing a light source that speeds on-chip and chip-to-chip communication.

Requirements for the integration of III-V and silicon technologies are more complex than the realisation of good performance. It is essential that the process must also be cost-efficient and suitable for mass production. So, in other words, it must be scalable and compatible with existing IC technology.

The key to cost-efficient, scalable integration is the monolithic hetero-epitaxial growth of III-V layers directly on a silicon substrate. This approach is superior to that of bonding at the wafer, chip and die level. However, the challenge is to develop a technology that can accommodate the lattice-mismatch between silicon and the majority of the III-Vs. Dislocation defects will arise, due to strain, so they have to be controlled and restricted to a constrained area, to allow the active III-V device layers to be free from defects.

Nano-ridge engineering

At imec, we are trailblazing a unique approach to the integration of III-Vs with CMOS. We are pioneering

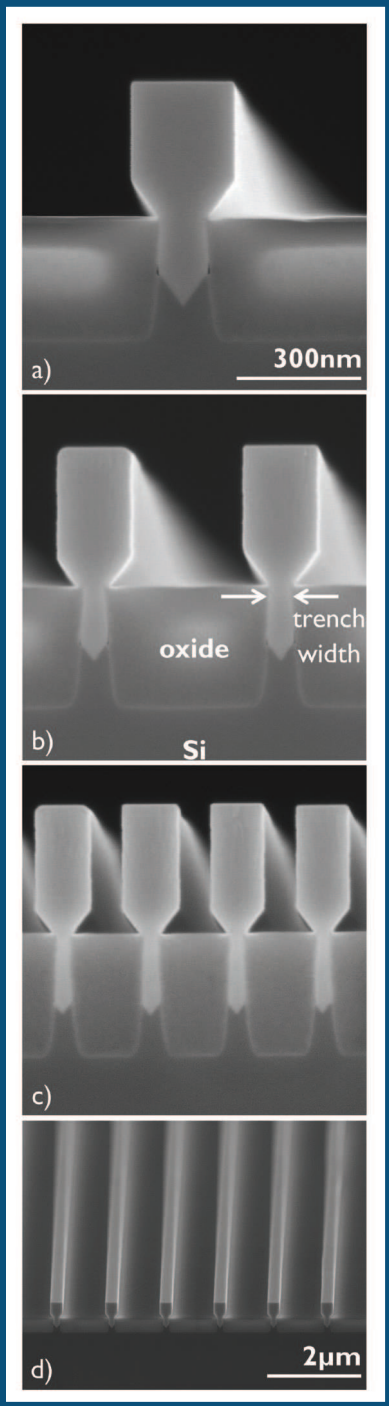


Figure 1. Cross-sectional, scanning electron micrograph images of cleaved GaAs nano-ridges. (a), (b) and (c) show GaAs nano-ridges on top of 100 nm, 40 nm and 20 nm wide oxide trenches, respectively. All structures were deposited in a single growth. (d) a tilted top-view scanning electron micrograph image of an nano-ridge array on top of 100 nm-wide trenches. Some of the images are modified and reprinted from B. Kunert *et al*. Appl. Phys. Lett. **109** 091101 (2016) with the permission of AIP Publishing.

nano-ridge engineering. It begins by depositing, by selective area growth, III-V material inside narrow oxide trenches that are formed on patterned 300 mm silicon substrates. Further growth of III-Vs creates nano-ridges.

This approach may appear esoteric, but it is not – it is compatible with standard processes used in the silicon CMOS industry. Patterning of silicon and its oxide is based on the shallow trench isolation process, and the growth of the III-Vs is by MOCVD.

The ingenuity of our approach is that the growth starts with the deposition of III-Vs in narrow trenches with a high aspect ratio – that is the height of the trench is far greater than its width. It's a technique that is known as aspect ratio trapping (ART), and it is successful with many different hetero-material systems. The geometry of the trench results in a very efficient dislocation trapping at the oxide side walls. Misfit and threading dislocations are constrained towards the bottom of the trench, creating a top region that is free from dislocation defects (more details on how it works can be found in the box "The art of aspect ratio trapping").

Aspect ratio trapping is particularly beneficial when combined with trenches oriented along <110> directions of silicon. This allows the preparation of a V-shaped silicon surface with two {111} planes. When III-Vs nucleate on a {111} silicon surface, this plane prevents the formation of anti-phase domains, which are detrimental to device performance.

When selective area growth continues, dislocation-free III-V material grows out of the trench. Adjusting the MOCVD growth parameters alters the form of the nano-ridge. For example, growth conditions can be selected to broaden the nano-ridge and thus increase the volume of III-V material, which can provide a foundation for new device architectures.

We have formed box-shaped GaAs nano-ridges on top of 100 nm, 40 nm and 20 nm wide trenches (see Figure 1). This series of growths shows that the fundamental shape evolution is independent of trench size. Viewing these structures from above with a scanning electron microscope reveals that the nano-ridges are of high quality and are highly uniform.

Our nano-ridge engineering also has great strength and flexibility. Adjusting the growth conditions enables the shape of the GaAs nano-ridge to be tuned to a tall rectangle, a triangle or various diamond-like shapes. Different structures result from selective manipulation of the growth rate hierarchy of the various nano-ridge facets. It is the facets with high growth rate that disappear quickly, while those with a low growth rate define the shape of the nano-ridge (see box "Nano-ridge engineering" for more details).

We are not the first to report the shape control of ridges. Others have announced homo-epitaxial selective-area growth of III-Vs on the micrometre scale – this is a fundamental feature of epitaxial growth. We break new ground by applying aspect ratio trapping to hetero-epitaxy of III-Vs on silicon, and realise astonishing control of nano-ridge formation on the nanometre scale.

The effectiveness of aspect ratio trapping is highlighted by images acquired by annular bright-field scanning transmission electron microscopy (see Figure 2). This technique reveals that threading dislocations, visible as dark blurry lines, are restricted to within the trench, while GaAs nano-ridge material, on top of the oxide pattern, is free from these imperfections.

We are currently exploring additional metrology techniques that may provide a better insight into defect statistics. To date, we have a very strong indication that dislocation trapping is extremely efficient in trenches with a width of 100 nm or less for 300 nm deep trenches. Nevertheless, along

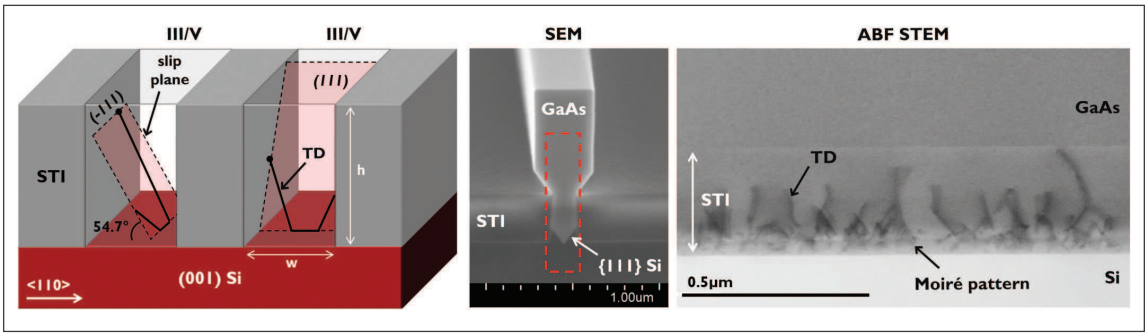


Figure 2. Left: An illustration of aspect ratio trapping of threading dislocations in {111} planes. Middle: Cross-sectional scanning electron micrograph images of a box-shaped GaAs nano-ridge surface. Right: Annular bright-field scanning transmission electron microscopy (ABF STEM) of a GaAs nano-ridge in cross-section along the trench. The transmission electron microscopy sample volume is also indicated in the scanning electron micrograph image by the red-dashed line. The dark blurry lines in the ABF STEM image are threading dislocations, which are all trapped inside the trench. The V-shaped {111} silicon surface induces a Moiré pattern in the transmission electron microscopy image close to the GaAs-silicon interface.

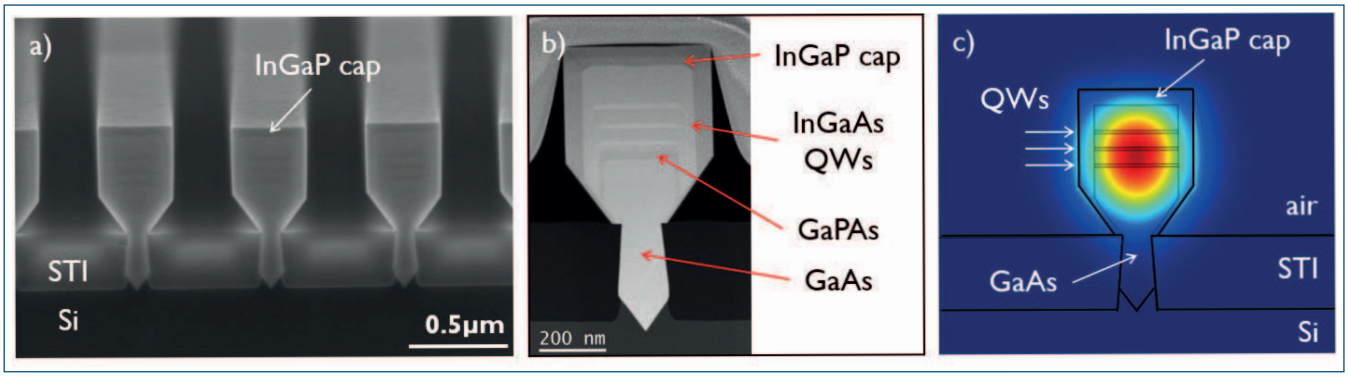


Figure 3. (a) Cross-section scanning electron micrograph images of InGaAs/GaAs nano-ridge lasers with an InGaP cap on top of 60 nm-wide trenches. (b) High-angle annular dark-field (HAADF) scanning transmission electron microscopy image of a nano-ridge laser sitting on a 100 nm-wide trench. c) Finite difference eigenmode simulation of the basic transverse electric (TE)-like mode, based on the dimensions of the nano-ridge laser shown in (b). Some of the images are modified and reprinted from Y. Shi et al Optica **4** 1468 (2017).

the nano-ridge length we can see planar defects, such as a micro twin every several micrometres. To eradicate these defects, we are devoting much effort to optimising the III-V nucleation and the pre-cleaning step for the trench-patterned wafer.

Lasers on the edge

The combination of impressive uniformity of the nano-ridge lines, the smooth surface morphology and a ridge with a width of several hundred nanometres lends itself to the production of a nano-ridge laser, where the nano-ridge acts as an optical waveguide. Working in partnership with Ghent University, we have produced such a device. It features $In_{0.2}Ga_{0.8}As$/GaAs multi-quantum wells, grown compressively strained on top of the (001) nano-ridge facet; and a lattice-matched $In_{0.49}Ga_{0.51}P$ cap layer, which surrounds the full nano-ridge, ensures carrier confinement and provides surface passivation.

Cross-sectional scanning electron microscopy imaging of our device layer stack, sitting on top of 60 nm-wide trenches, emphasises the impressive continuity from ridge to ridge (see Figure 3 (a)). The InGaP cap layer around the waveguide ridge is easy to identify, and it is possible to make out the positions of the quantum wells.

Greater detail is provided by high-angle annular dark-field scanning transmission electron microscopy. When this is used to image a nano-ridge laser on a 100 nm-wide trench each of its layers is clearly visible. The device also contains a GaPAs layer, which is explored for strain compensation and additional

The art of aspect ratio trapping

III-Vs AND SILICON are lattice-mismatched, so the growth of the former on the latter generates defects. However, these imperfections can be trapped with great efficiency by selective area growth in highly confined trenches oriented along <110> directions of silicon. The key is to use trenches that are far higher than they are wide.

When III-Vs are deposited on patterned silicon/SiO_2 substrates, misfit and threading dislocations form during the growth to release strain. A typical relaxation mechanism is the nucleation of dislocation half-loops at the growth surface, which glide down towards the interface between the III-V and silicon to efficiently release the strain.

If the dislocation Burgers vector is based on a 60° misfit dislocation, the slip plane is a {111} plane. Hence, as the dislocation half-loops start to glide down along the {111} plane and extend in width, the two threading dislocation 'arms' hit the oxide sidewall and are trapped. This trapping mechanism is easy to follow when the {111} slip plane is perpendicular to the trench sidewalls.

The {111} slip plane can also be parallel to the sidewall. When that's the case, the dislocation half-loop 'arms' finally hit the oxide wall as the trench gets filled due to the inclined angle of 54.7° of the {111} plane, so long as the aspect ratio of the trench – that is its height to width ratio – exceeds 1.43. As aspect ratios for trenches are far higher than this, all dislocation defects are fully trapped in both directions, so long as the relaxation process proceeds via threading dislocations gliding along {111} planes. Success hinges on enhancing pronounced dislocation nucleation close to the interface between the III-V and silicon, to ensure full strain release of the hetero-layer.

Note that stacking faults and micro twins, which are planar defects running in the <111> direction, are only trapped in {111} planes parallel to the sidewalls. Consequently, a planar defect that is running perpendicular to the sidewall could penetrate the full III-V structure. So, to prevent this from happening, planar defect formation has to be eradicated by optimising the growth conditions, the silicon surface pre-treatment and the fabrication process for the trenches.

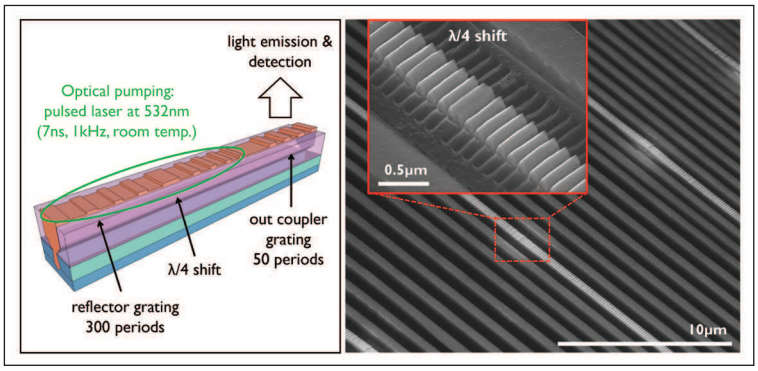


Figure 4. Left: An illustration of the distributed feedback laser design produced by imec, and the excitation geometry using for optical pumping. Right: Top-view scanning electron micrograph image of imec's fabricated nano-ridge lasers. The inserted, higher magnification image shows the λ/4-phase shift segment between the two reflector gratings.

carrier confinement.

We have modelled the performance of our lasers. Using a finite difference eigenmode solver, we have simulated the basic transverse electric-like mode for our nano-ridge laser (see Figure 3(c)). Results suggest that our device has a confinement factor for the transverse electric mode of 9.3 percent, which is more than sufficient to realise efficient optical gain. Light field losses into the silicon substrates are acceptable, with values less than 5 dB cm^{-1}.

Development of our devices began with the fabrication of distributed feedback lasers at Ghent University. Construction of these edge-emitters that are designed for optical pulse pumping involves processing, into the nano-ridge top surface, a first-order reflector grating with a λ/4-phase shift section. To couple the light out of the waveguide for detection, we add a second-order grating (see Figure 4 for an illustration of the design of the laser, the excitation geometry, the pumping laser conditions as well as top-view images of fabricated nano-ridge lasers).

Due to the narrow spacing of the nano-ridges, we processed isolated, clearly separated nano-ridges. Adopting this approach enabled optical pumping, from above, of a single nano-ridge laser.

Optical pumping of these structures produced a clear threshold behaviour, in line with a pronounced linewidth narrowing of the emission spectrum (see Figure 5(a)). These characteristics are indicative of laser operation at room temperature. As expected for a distributed feedback laser, there is a clear single-mode laser emission above the pumping threshold – in our case, the onset is at 37 mW, equating to a pump density of 33.6 kW cm^{-2}. Encouragingly, the peak emission intensity for excitation at 215 mW is 28 dB above the background, demonstrating excellent single-mode laser performance (see Figure 5(b)).

An interesting attribute of our lasers is that there is a

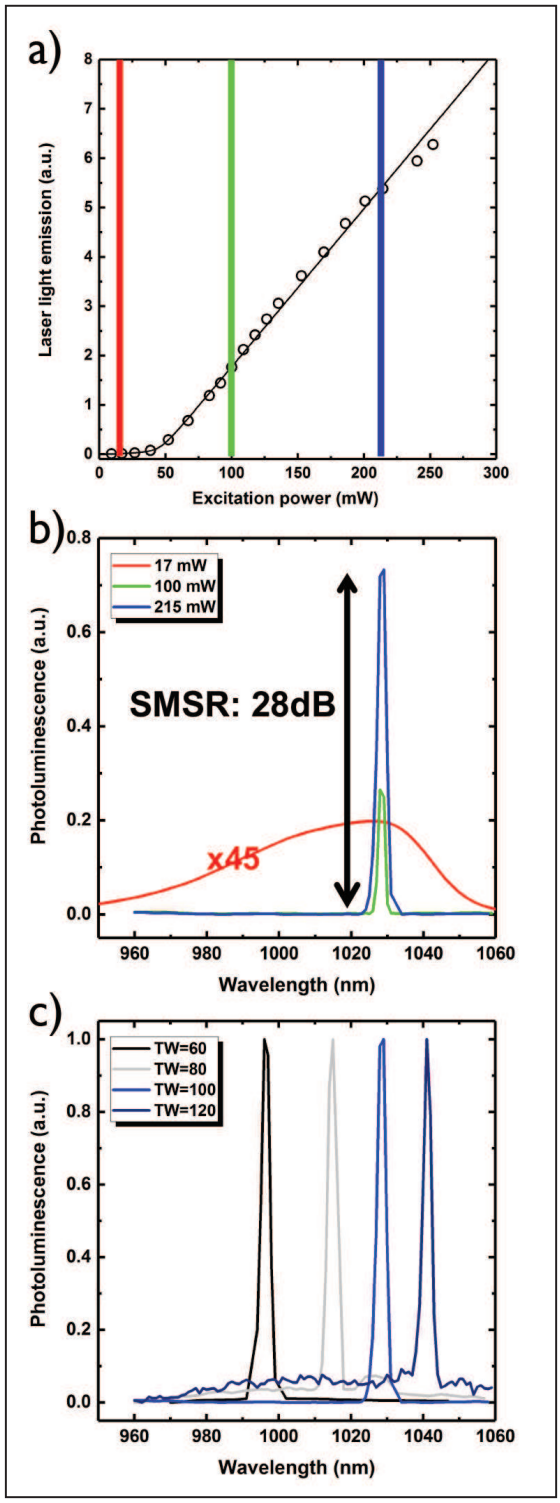


Figure 5. (a) Laser light emission versus excitation power for a distributed feedback nano-ridge laser (170 nm first-order grating period) on top of a 100 nm-wide trench. The corresponding emission spectra at the excitation power indicated by the red, green and blue lines are shown in (b). Note that the SMSR is the side mode suppression ratio. (c) Comparison of the emission spectrum for a nano-ridge laser based on trenches with widths of 60 nm, 80 nm, 100 nm and 120 nm. The emission intensity is normalized for better comparison. All the plots are reprinted from Y. Shi *et al*. Optica **4** 1468 (2017)

shift in emission wavelength with trench width (see Figure 5(c)). The shift, which may be useful in certain applications, stems from a change in nano-ridge volume.

Even though our work is in its infancy, it shows great promise. As the epitaxial growth conditions govern nano-ridge engineering, it can be applied to a multitude of device architectures and designs. This means that our laser diodes don't have to be restricted to designs made from InGaAs and GaAs – the door is open to pursue many new opportunities. With this in mind, while undertaking ongoing development of our nano-ridge lasers towards current injection, we will also be actively exploring nano-ridge engineering of different III-V material systems and device applications. So keep a look out for our next success, which we will soon report.

Further reading

B. Kunert *et al*. Appl. Phys. Lett. **109** 091101 (2016)
B. Kunert *et al*. ECS Trans. **75** 409 (2016)
Y. Shi *et al*. Optica **4** 1468 (2017)

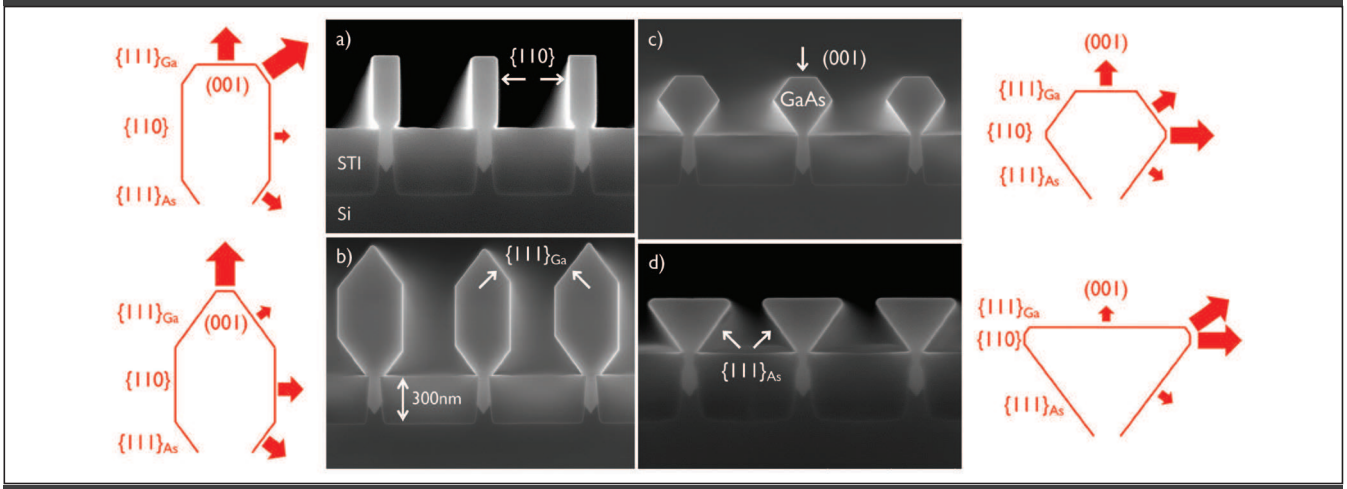
Nano-ridge engineering

APPLYING APPROPRIATE deposition conditions, and exploiting differences in growth rate on different facets, hold the key to III-V nano-ridge engineering. When a free-standing nano-ridge grows out of a trench, it contains several facets, exposed with different III-V surface configurations. For example, when GaAs is grown in trenches with V-shaped {111} silicon surfaces, they have normally a polarity that reveals a gallium-terminated top $\{111\}_{Ga}$ and an arsenic-terminated lower $\{111\}_{As}$ nano-ridge plane. For the surface configuration on {110} and (001), the situation is markedly different.

Surface reconstruction on the different facets is determined by the MOCVD growth conditions, such as the growth temperature, reactor pressure, precursor partial pressure and gas phase ratio. The rate of growth of any facet is determined by the precursor diffusion length, and the adsorption and desorption rates. Modifying the deposition conditions increases the growth rate on some facets, slows it on others, and ultimately controls the geometry of the nano-ridge. As the facet with the highest growth rate disappears quickly with deposition time, the shape of the nano-ridge is defined by the facets with lower growth rates.

Highlighting the impact of different growth conditions are cross-sectional scanning electron microscopy images, shown in the figure below. The trench formed in (a) results from a very high GaAs growth rate on the $\{111\}_{Ga}$ facets, a medium growth rate on the (001) plane and a very low deposition rate on the {110} and $\{111\}_{As}$ facets. Due to these conditions, the nano-ridge evolves into a rectangle with a high aspect ratio.

With structures (b), (c) and (d), the conditions have been modified to manipulate the growth rate hierarchy in a different way (note that the size of the red arrows in the figure indicates the strength of the growth rate on the different facets). For structure (b), the (001) facet disappears, while in (c) the {110} facet vanishes, and in (d) the $\{111\}_{Ga}$ and {110} facets vanish. Each of these conditions produces an exclusive nano-ridge shape. Different shapes may be better for integrating different types of III-V devices with silicon wafers.



Cross-section scanning electron microscopy images of GaAs nano-ridges deposited under different MOCVD growth conditions and the corresponding sketch to indicate the different growth rate hierarchies. The size of each red arrow indicates the growth rate on the particular facets (the bigger the arrow, the higher the GaAs growth rate).