Silicon-Integrated Hybrid-Cavity 850-nm VCSELs by Adhesive Bonding: Impact of Bonding Interface Thickness on Laser Performance

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***Abstract*—The impact of bonding interface thickness on the performance of 850-nm silicon-integrated hybrid-cavity vertical-cavity surface-emitting lasers (HC-VCSELs) is investigated. The HC-VCSEL is constructed by attaching a III–V "half-VCSEL" to a dielectric distributed Bragg reflector on a Si substrate using ultrathin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding. The thickness of the bonding interface, defined by the DVS-BCB layer together with a thin SiO_2 layer on the "half-VCSEL," can be used to tailor the performance, for e.g., maximum output power or modulation speed at a certain temperature, or temperature-stable performance. Here, we demonstrate an optical output power of 2.3 and 0.9 mW, a modulation bandwidth of 10.0 and 6.4 GHz, and error-free data transmission up to 25 and 10 Gb/s at an ambient temperature of 25 and 85 °C, respectively. The thermal impedance is found to be unaffected by the bonding interface thickness.**

***Index Terms*—Heterogeneous integration, high-speed modulation, large signal modulation, optical interconnects, semiconductor lasers, silicon photonics, vertical-cavity surface-emitting laser (VCSEL).**

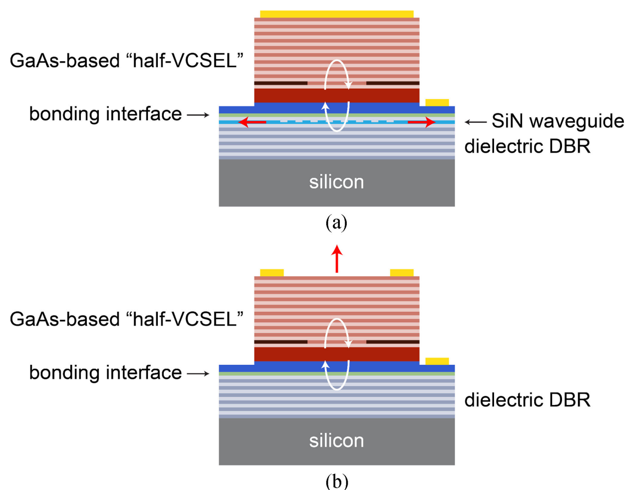

Fig. 1. (a) Hybrid vertical-cavity laser with in-plane emission, and (b) hybrid-cavity VCSEL.

I. Introduction

The integration of an efficient light source is considered the Holy Grail of silicon photonics (SiP) [1]. For short-wavelength SiP (i.e. silicon nitride (SiN) waveguide circuits), integration concepts utilizing GaAs-based vertical-cavity surface-emitting laser (VCSEL) technology are attractive, since the small modal and gain volumes facilitate energy efficient operation with demonstrated power conversion efficiencies exceeding 60% [2] for regular VCSELs. Such integration concepts can potentially enable fully integrated short-wavelength photonic integrated circuits (PICs) for optical interconnects and bio-sensing applications.

To equip SiP ICs with integrated light sources, several techniques have been explored, including flip-chip bonding [3] and direct growth of III-V material on Si [4]. Flip-chip bonding requires stringent alignment whereas direct growth struggles to achieve high-quality material. An alternative technique is heterogeneous integration where a III-V epitaxial structure grown on its native substrate is bonded to the SiP IC using direct or adhesive bonding [5]. This technique has been used to demonstrate silicon-integrated InP-based hybrid vertical-cavity lasers for surface and in-plane emission [6]–[8]. The hybrid cavity, which implies that the standing wave optical field extends over both the III-V and the silicon-based parts of the cavity, provides an opportunity to tap off light to an in-plane waveguide using e.g. an intra-cavity waveguide with a weak diffraction [9], see Fig. 1(a).

Recently, we demonstrated silicon-integrated GaAs-based hybrid-cavity VCSELs (HC-VCSELs) with 1.6 mW output power at 845 nm [10] and capable of 20 Gb/s error-free data transmission under direct current modulation [11]. Ultrathin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding was used to attach a III-V "half-VCSEL" to a dielectric distributed Bragg reflector (DBR) on Si, see Fig. 1(b).

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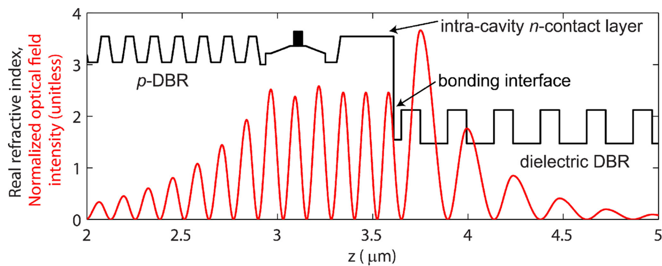

Fig. 2. Simulated standing-wave optical field intensity along the optical axis of the HC-VCSEL (red), together with the real refractive index profile (black).

While this device does not yet contain the intra-cavity waveguide with a diffraction grating for in-plane emission, and thus is surface emitting, it still allows the investigation and development of the integration concept and design.

In our previous work [10], [11], the output power and high temperature performance were limited by a too small detuning between the gain peak and the cavity resonance wavelengths. However, the hybrid-cavity concept offers the opportunity to control the detuning, and therefore the laser performance, by the thickness of the bonding interface, while in an ordinary VCSEL the detuning is set during epitaxial growth and cannot be adjusted in a post-growth process. Here, we present the results from an investigation where we have systematically varied the thickness of the bonding interface and monitored the impact on important laser performance parameters. We show, that the thickness can be chosen to optimize a certain performance parameter at a given temperature or to minimize the variation of performance with temperature. We also find that the thermal impedance of the HC-VCSEL is largely unaffected by the thickness of the bonding interface. Finally, we demonstrate error-free data transmission at bit rates up to 25 Gb/s and 10 Gb/s at 25 and 85 °C, respectively.

The paper is organized as follows. Section II describes the concept and design of the HC-VCSEL and presents results from simulations. In Section III the device fabrication is outlined, while Section IV presents results from static and dynamic measurements. The paper is concluded in Section V.

II. Design and Simulations

The HC-VCSEL design is illustrated in Fig. 1(b). A plot showing the variations of the real part of the refractive index and the intensity of the optical standing wave along the optical axis of the cavity is presented in Fig. 2. To the left of the bonding interface is the III-V "half-VCSEL" consisting of an n-$\mathrm{Al_{0.12}Ga_{0.88}As}$ intra-cavity contact layer, an active region with five 4 nm $\mathrm{In_{0.10}Ga_{0.90}As}$ quantum wells (QWs) with photoluminescence (PL) peak measured at 840 nm, a p-$\mathrm{Al_{0.98}Ga_{0.02}As}$ layer for the formation of an oxide aperture for transverse current and optical confinement, and a 23-pair p-$\mathrm{Al_{0.90}Ga_{0.10}As/Al_{0.12}Ga_{0.88}As}$ DBR. To the right of the interface is the 20-pair $\mathrm{SiO_2/Ta_2O_5}$ dielectric DBR on the Si substrate. The calculated reflectance (assuming lossless materials) is >99.99% at the center wavelength of 845 nm.

TABLE I
Cavity Parameters at a Resonance Wavelength of 845 nm

Optical confinement factor	0.0173
Cold cavity Q	16200
Total loss ($\mathrm{ps^{-1}}$)	0.138
Top DBR transmission loss ($\mathrm{ps^{-1}}$)	0.053
Bottom DBR transmission loss ($\mathrm{ps^{-1}}$)	$3{\cdot}10^{-5}$
Intra-cavity loss ($\mathrm{ps^{-1}}$)	0.085
Threshold QW gain ($\mathrm{cm^{-1}}$)	609
Photon lifetime (ps)	7.25

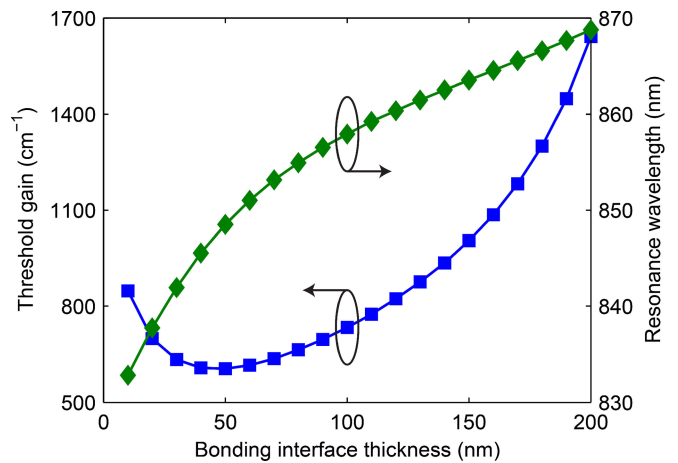

Fig. 3. Simulated dependence of resonance wavelength and threshold gain on bonding interface thickness.

The bonding interface is defined by a ∼40 nm DVS-BCB bonding layer and a thin $\mathrm{SiO_2}$ layer deposited on the dielectric DBR prior to bonding. The thickness of the $\mathrm{SiO_2}$ layer is used to control the interface thickness and therefore the cavity length, which sets the cavity resonance wavelength and the detuning between the gain peak (estimated at 852 nm from the PL wavelength) and resonance wavelengths. Detuning is an important design parameter as it controls the optical gain properties as well as the temperature dependence of important laser parameters since the gain peak red-shifts faster with temperature than the resonance wavelength [12]. The detuning can therefore be chosen for either optimized performance at a specific temperature or stable performance over temperature [13]. It should be noted however, that in a final design the desired detuning can be obtained with a bonding interface comprising only the DVS-BCB layer with appropriate thickness. The length of the cavity is 3λ to accommodate an n-contact layer with sufficient thickness for low electrical series resistance.

The optical cavity properties were analyzed using a 1D effective index model [14]. Table I lists some important cavity parameters when the interface thickness is adjusted for a resonance wavelength of 845 nm. The intra-cavity loss is due to free-carrier absorption in the n-contact layer and the p-DBR. The variations of QW threshold gain and cavity resonance wavelength with the thickness of the bonding interface are shown in Fig. 3. Over a ∼35 nm wavelength span (830–865 nm), the threshold gain is below 1000 $\mathrm{cm^{-1}}$, which should allow for low threshold currents.

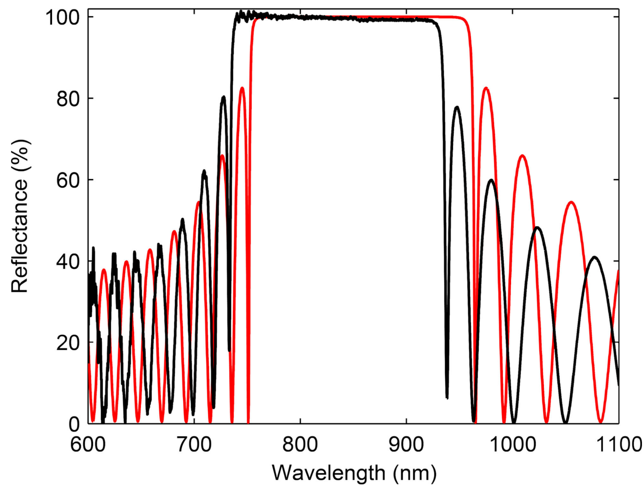

Fig. 4. Simulated (red) and measured (black) spectral reflectance for the 20-pair SiO_2/Ta_2O_5 dielectric DBR.

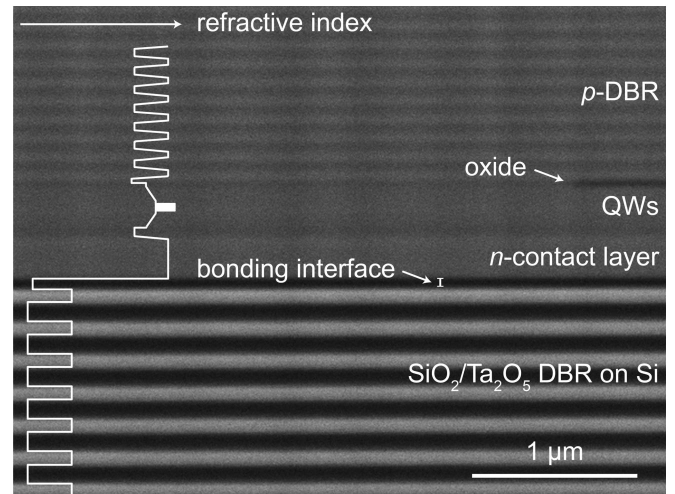

Fig. 5. SEM micrograph of a FIB cross-section through a HC-VCSEL with an overlay of the refractive index profile. The bonding interface between the III-V "half-VCSEL" and SiO_2/Ta_2O_5 DBR on Si is indicated.

III. Fabrication

The 20-pair SiO_2/Ta_2O_5 dielectric DBR was deposited on a polished Si substrate. A comparison of simulated and measured reflectance spectra (Fig. 4) shows good agreement in terms of the width of the stopband ($\sim$200 nm) and a slight blue-shift of the measured center wavelength ($\sim$20 nm) with respect to simulations.

The III-V "half-VCSEL" epitaxial structure was grown on a GaAs substrate by metal-organic chemical vapor deposition at IQE Europe Ltd. Dies (8 mm $\times$ 10 mm) of the epitaxial structure were bonded to the dielectric DBR using ultra-thin DVS-BCB adhesive bonding [5]. The bonding process includes spin-coating of DVS-BCB:mesitylene on the dielectric DBR, which was partially cured before the "half-VCSEL" die was attached with the epitaxial structure facing the dielectric DBR. The die and dielectric DBR were clamped between two glass wafers and mounted in a wafer bonding tool where pressure was applied on the "half-VCSEL" die while the DVS-BCB bonding interface was fully cured. The bonding process results in a DVS-BCB thickness of $\sim$40 nm, which is controllable within $\pm$10 nm and with a uniformity of $\pm$5 nm for both dies and wafers [5]. Prior to bonding, thin SiO_2 layers with varying thickness were deposited on dielectric DBR samples by plasma-enhanced chemical vapor deposition (PECVD). This layer has similar refractive index as DVS-BCB and the thickness can be controlled with an accuracy of 5%. The effects of thickness variation on performance is shown in Section IV. Four samples with an interface thickness of 35, 65, 125, and 180 nm and cavity resonance wavelengths of 843, 853, 861, and 867 nm were prepared, corresponding to a gain-to-resonance detuning of approximately +9, −1, −9, and −15 nm, respectively. The resonance wavelengths were extracted from optical emission spectra of fully fabricated HC-VCSELs biased below threshold at 25 °C.

HC-VCSELs were fabricated using a standard process for oxide-confined VCSELs after removal of the GaAs substrate using mechanical thinning for the first part and selective wet etching for the remaining part of the substrate [10]. Ti/Pt/Au contact rings and alignment marks were evaporated on the top highly *p*-doped GaAs contact layer. The devices were isolated by etching trenches through the III-V using inductively coupled plasma reactive ion etching (ICP-RIE) with $SiCl_4$ chemistry. This was done to allow residual gas trapped at the bonding interface to escape during subsequent high-temperature processing steps. Circular mesas were then etched using the same dry etching technique. An *in-situ* end-point detection system was used to accurately stop within the thin ($\sim$280 nm) $Al_{0.12}Ga_{0.88}As$ *n*-contact layer and expose the $Al_{0.98}Ga_{0.02}As$ layer for oxidation. The mesa surface and the *n*-contact layer were protected during oxidation by a 100 nm thick Si_xN_y layer deposited by PECVD. Just before oxidation, this layer was removed on the mesa side walls using ICP etching with NF_3 chemistry. The oxide formation was performed at 420 °C in a wet oxidation furnace with *in-situ* monitoring of the oxidation front. After oxidation, the protective Si_xN_y layer was removed using ICP etching with NF_3 chemistry to allow evaporation of Ni/Ge/Au intra-cavity *n*-contacts, which were annealed 30 s at 430 °C. Finally, the mesas were planarized with a thick BCB layer to allow sputtering of low capacitance Ti/Au ground-signal-ground (GSG) bondpads with 100 μm pitch.

In Fig. 5, a scanning electron microscope (SEM) micrograph of a focused ion beam (FIB) cross-section through a fully fabricated HC-VCSEL is shown with an overlay of the refractive index profile. The micrograph clearly shows that the III-V "half-VCSEL" is attached to the SiO_2/Ta_2O_5 DBR on Si at the indicated bonding interface.

IV. Measurements

A. Static Performance

Four HC-VCSELs denoted A–D, with resonance wavelengths of 843, 853, 861, and 867 nm were investigated. The diameter of the oxide aperture is 10 μm. The output power and voltage versus current measured at ambient temperatures ranging from

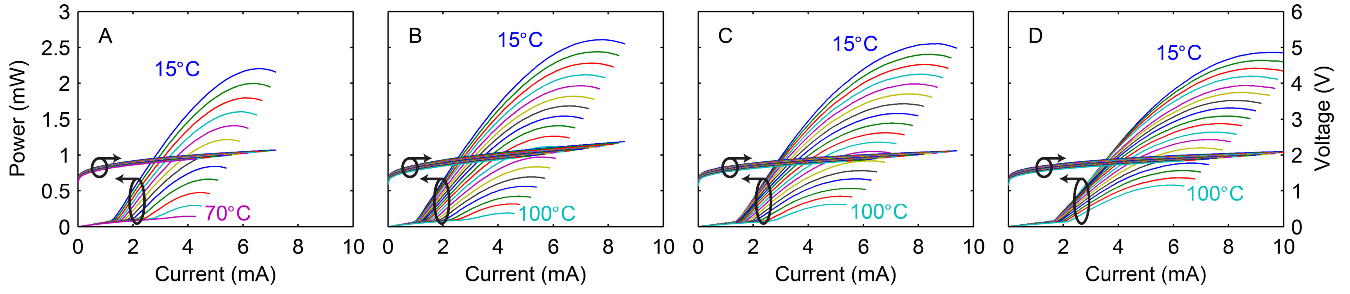

Fig. 6. Output power and voltage versus current for HC-VCSELs A–D measured at ambient temperatures ranging from 15 to 100 °C in steps of 5 °C.

TABLE II
STATIC PERFORMANCE PARAMETERS

Parameter	Temp. (°C)	HC-VCSEL A	B	C	D
Resonance wavelength (nm)	25	843	853	861	867
Peak gain-to-resonance detuning (nm)	25	+9	−1	−9	−15
Temperature at min. threshold current (°C)		6	27	36	54
Threshold current (mA)	25	1.42	1.07	1.42	1.85
	55	2.18	1.36	1.52	1.64
	85	n/a	2.10	2.08	1.87
	100	n/a	3.00	2.77	2.24
Maximum optical output power (mW)	25	1.8	2.3	2.3	2.2
	55	0.66	1.4	1.4	1.5
	85	n/a	0.56	0.67	0.89
	100	n/a	0.19	0.31	0.58
Thermal roll-over current (mA)	25	6.2	7.4	8.2	9.0
	55	4.8	6.2	7.1	7.9
	85	n/a	5.0	5.7	6.6
	100	n/a	4.3	5.0	5.9
Slope efficiency (W/A)	25	0.54	0.55	0.54	0.50
	55	0.30	0.42	0.41	0.39
	85	n/a	0.25	0.26	0.28
	100	n/a	0.09	0.16	0.22
Differential resistance at 4 mA (Ω)	25	61	81	55	51
	55	62	79	54	50
	85	n/a	79	55	50
	100	n/a	81	55	51
Differential resistance at thermal roll-over (Ω)	25	48	61	33	28
	55	60	67	41	34
	85	n/a	76	48	42
	100	n/a	81	53	45

15 to 100 °C, in steps of 5 °C, are shown in Fig. 6 while the corresponding static performance characteristics are summarized in Table II.

The variation of threshold current with the bonding interface thickness at 25 °C follows the variation of threshold gain predicted by the simulations (Fig. 3). Minimum threshold current (1.1 mA) is obtained for HC-VCSEL B which has the smallest gain-to-resonance detuning at 25 °C. At higher ambient temperatures, HC-VCSELs C and D have lower threshold currents since the detuning is reduced with temperature as a result of the ∼4 times faster redshift of the gain peak with respect to the cavity resonance [15]. The threshold currents from Fig. 6 are shown versus ambient temperature in Fig. 7(a). The temperatures for minimum threshold current were identified by fitting a second order polynomial to the dependence of threshold current on temperature, as seen in Fig. 7(b). At the temperature for minimum threshold current, the wavelengths of the cavity resonance and the gain peak are aligned. At 25 °C this occurs at 852 nm as estimated in Section II. While the threshold current of HC-VCSEL D is higher than that of HC-VCSEL B at 25 °C, it is lower at high temperatures and shows a weaker dependence on temperature. Therefore, the thickness of the bonding interface can be chosen for either minimum threshold current at a specific ambient temperature or a small variation of threshold current over the temperature range.

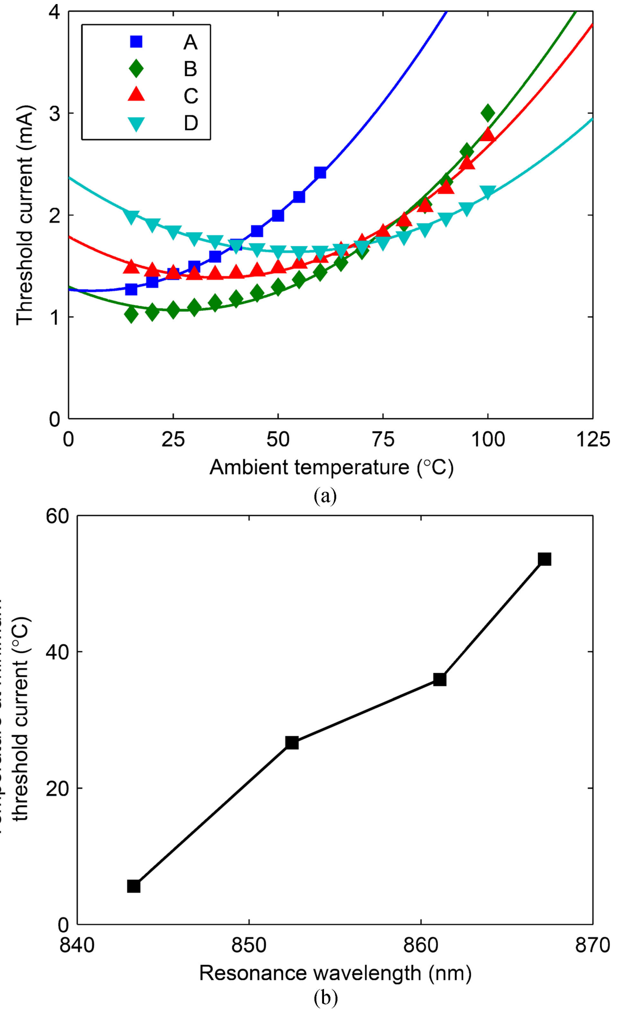

Fig. 7. (a) Threshold current versus ambient temperature and (b) estimated temperature at minimum threshold current versus resonance wavelength.

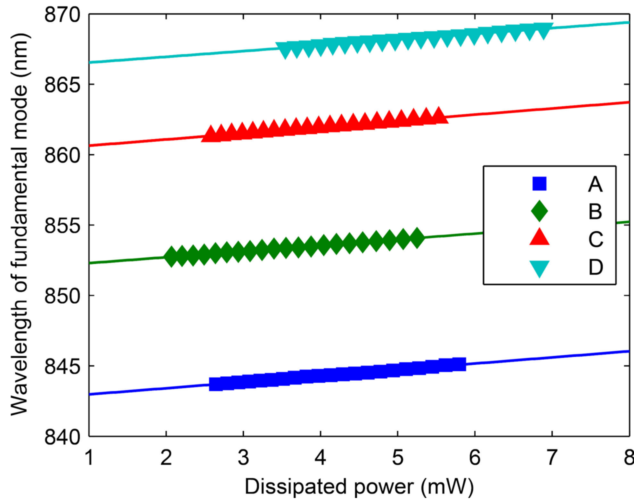

Fig. 8. Wavelength of the fundamental mode versus dissipated power at 25 °C for HC-VCSELs A–D with fits to extract the thermal impedance.

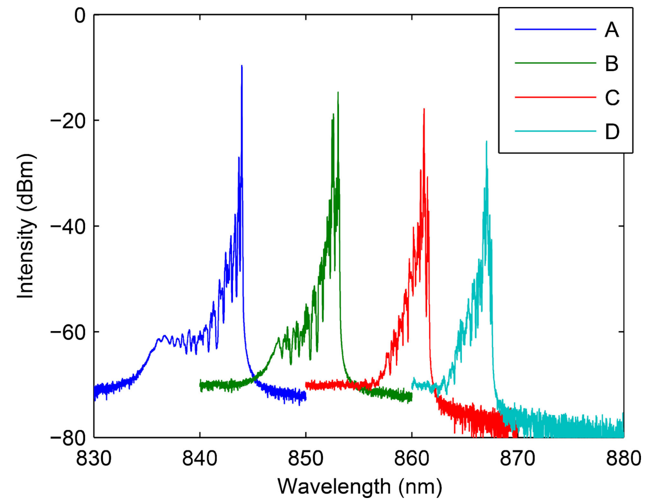

Fig. 9. Emission spectra at 25 °C for HC-VCSELs A–D biased at 2 mA.

The achievable output power depends on the threshold current, the slope efficiency and the thermal roll-over current. All HC-VCSELs have similar slope efficiency (∼ 0.5 W/A at 25 °C), with a slight variation caused by an uncertainty in the thickness of the topmost *p*-DBR layer after substrate removal. At high temperatures, the slope efficiency is reduced as a result of increased internal optical loss (free carrier absorption) and reduced internal quantum efficiency [16]. The thermal roll-over current is largely determined by the thermal impedance and the dependence of threshold current on temperature since the internal temperature increases with current due to heat dissipation caused by the electrical resistance and the free carrier absorption [16]. Therefore, while HC-VCSEL B and C produce the highest output power at 25 °C (2.3 mW), HC-VCSEL D shows improved high temperature and high current performance since the gain peak aligns with the resonance wavelength at higher internal temperature. The maximum output power at 100 °C is 0.6 mW. The rapid increase of threshold current with temperature for HC-VCSEL A limits the maximum operating temperature to 70 °C. Again, the thickness of the bonding interface can be chosen for either optimum performance at a specific ambient temperature or a small variation in performance over the temperature range.

Thermal impedance was measured by tracking the wavelength shift of the fundamental mode with dissipated power and ambient temperature [17]. The fundamental mode redshifts with temperature by 0.059 nm/K, while it redshifts with dissipated power by 0.42 nm/mW (Fig. 8). This gives a thermal impedance of 7 K/mW for all HC-VCSELs, regardless of the thickness of the bonding interface. This indicates that the thermal impedance is to a large extent determined by heat transport through the dielectric DBR. With the thermal impedance being ∼4 times larger than for ordinary GaAs-based oxide-confined VCSELs [16], the thermal roll-over currents are relatively low, which limits the maximum output power.

The differential resistances are comparable (50–60 Ω), with negligible dependence on temperature, since the bonding interface thickness should have no impact on the electrical characteristics. The somewhat higher resistance of HC-VCSEL B (80 Ω) is believed to be due to residues from the removal of the substrate, which led to a higher *p*-contact resistance. The performance of HC-VCSEL B is still superior in terms of maximum output power at temperatures up to 25 °C.

Optical emission spectra, measured at a bias current of 2 mA, are shown in Fig. 9. The dependence of wavelength on the bonding interface thickness agrees well with the simulations in Fig. 3. Also the modal characteristics are affected by the bonding interface thickness, which controls the gain-to-resonance detuning, with the lower order (longer wavelength) modes favored by positive detuning and higher order (shorter wavelength) modes by negative detuning.

B. *Dynamic Performance*

The dependence of the dynamic performance on bonding interface thickness/detuning was investigated by recording the small-signal modulation response at 25, 55, and 85 °C. Measurements were performed using a 67 GHz vector network analyzer (Rohde & Schwarz ZVA67), with internal bias-T, connected to the HC-VCSEL with a high-speed probe (Picoprobe 40A-GSG-100P) matching the HC-VCSEL bondpad pitch. The output was coupled to a 1 m long OM4 multimode optical fiber through an antireflection (AR) coated lens package, followed by a 25 GHz photodetector (New Focus 1481-S-50) and the network analyzer. A variable optical attenuator (EXFO FVA-3150) was inserted before the photodetector to avoid saturation of the photodetector.

The modulation response for HC-VCSELs A–D at 25 and 85 °C, compensated for the frequency response of the probe and the photodetector, are shown in Fig. 10. A three-pole transfer function [18] was fitted to the measured modulation response to extract the resonance frequency and damping rate, as well as the parasitic pole frequency. The dynamic performance characteristics of all HC-VCSELs at three ambient temperatures are summarized in Table III.

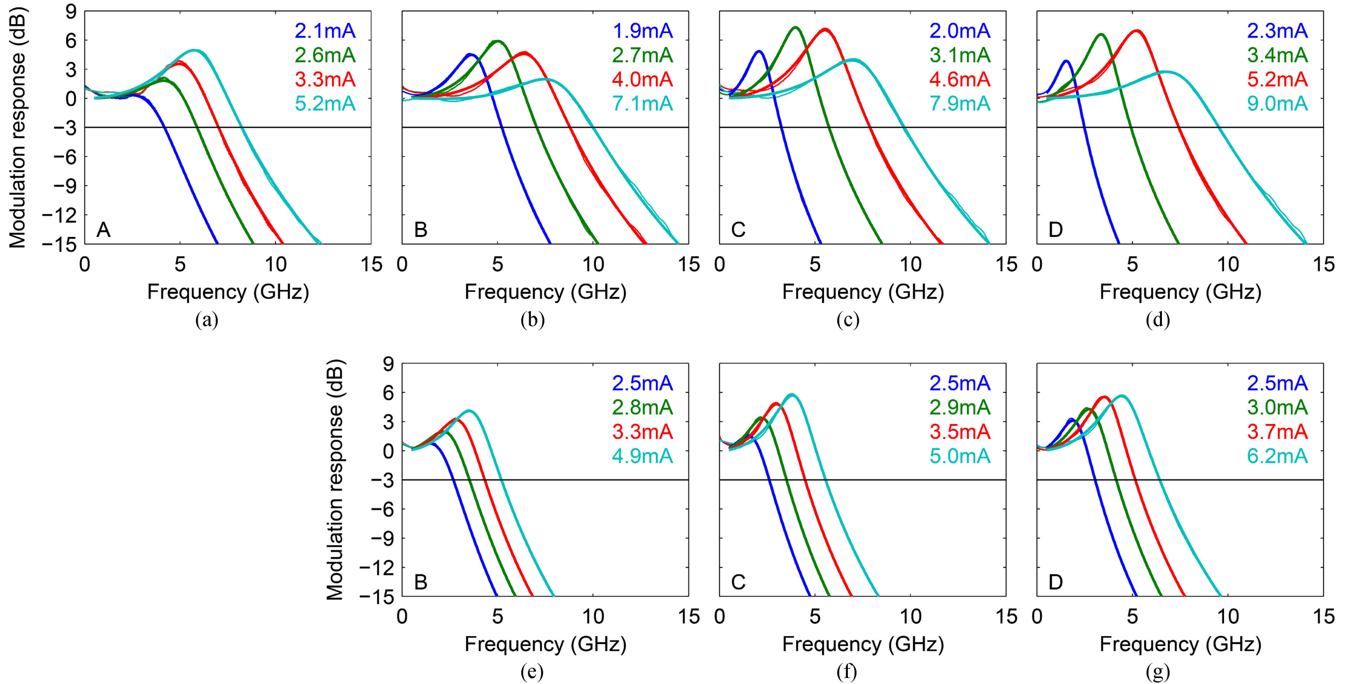

Fig. 10. Small-signal modulation response at 25 °C (a)–(d) and 85 °C (e)–(g) for HC-VCSELs A–D at indicated bias currents. The maximum 3 dB modulation bandwidth is reached at the highest bias currents indicated.

TABLE III
DYNAMIC PERFORMANCE PARAMETERS

Parameter	Temp. (°C)	HC-VCSEL A	HC-VCSEL B	HC-VCSEL C	HC-VCSEL D
Maximum 3 dB bandwidth (GHz)	25	8.2	10.0	9.7	9.5
	55	4.3	8.1	8.1	8.1
	85	n/a	5.2	5.6	6.4
Bias current at max. 3 dB bandwidth (mA)	25	5.2	7.1	7.9	9.0
	55	4.4	5.8	6.9	7.1
	85	n/a	4.9	5.0	6.2
D-factor (GHz/mA$^{1/2}$)	25	4.8	4.2	3.3	3.0
	55	2.8	4.2	3.3	2.9
	85	n/a	3.1	2.6	2.7

All HC-VCSELs show a strongly resonant modulation response caused by the relatively low photon density established in the cavity at thermal roll-over. A more damped response is desired to reduce overshoot and jitter during large signal modulation and data transmission [19].

Although the modulation bandwidth is largely limited by the capacitance over the single oxide layer (with a parasitic pole frequency of 6–8 GHz), there are clear differences in the maximum modulation bandwidth related to the differences in bonding interface thickness and gain-to-resonance detuning. The maximum modulation bandwidth depends on how fast the resonance frequency increases with bias current (quantified by the *D*-factor) and the highest photon density that can be achieved [20].

The *D*-factors were extracted from the measured dependence of the resonance frequency on the square root of current above threshold, as shown in Fig. 11(a) at 25 °C. The *D*-factors are plotted in Fig. 11(b). Clearly, the *D*-factor is reduced with increasing resonance wavelength. This is caused by the differential gain being lower on the long-wavelength side of the gain peak. At higher temperatures (Table III), the *D*-factors are further reduced due to a reduction of differential gain with temperature and a more pronounced reduction of internal quantum efficiency at the highest temperature.

The maximum photon density is reached at the thermal roll-over current. Therefore, higher photon densities can be established in HC-VCSELs with low threshold current and weak dependence of threshold current on temperature.

As a consequence of these dependencies, HC-VCSEL B has the highest 3 dB modulation bandwidth at 25 °C (10.0 GHz) while HC-VCSEL D has the highest bandwidth at 85 °C (6.4 GHz). HC-VCSEL D also shows the smallest dependence of bandwidth on temperature. Similar to the threshold current and the maximum output power, the bonding interface thickness can be chosen for either a maximum bandwidth at a specific ambient temperature or a more temperature-stable bandwidth.

C. Data Transmission

A HC-VCSEL with similar resonance wavelength (859 nm) as HC-VCSEL C, but with a smaller oxide aperture diameter (5 μm), was chosen for back-to-back data transmission experiments. The smaller aperture device has a slightly more damped modulation response and a higher photon density at low bias currents. The small signal 3 dB modulation bandwidth for this device is 12.1 and 8.9 GHz at 25 and 85 °C, respectively.

A non-return-to-zero pseudo random bit sequence (PRBS) signal with word length 2^7-1 was generated by a bit pattern

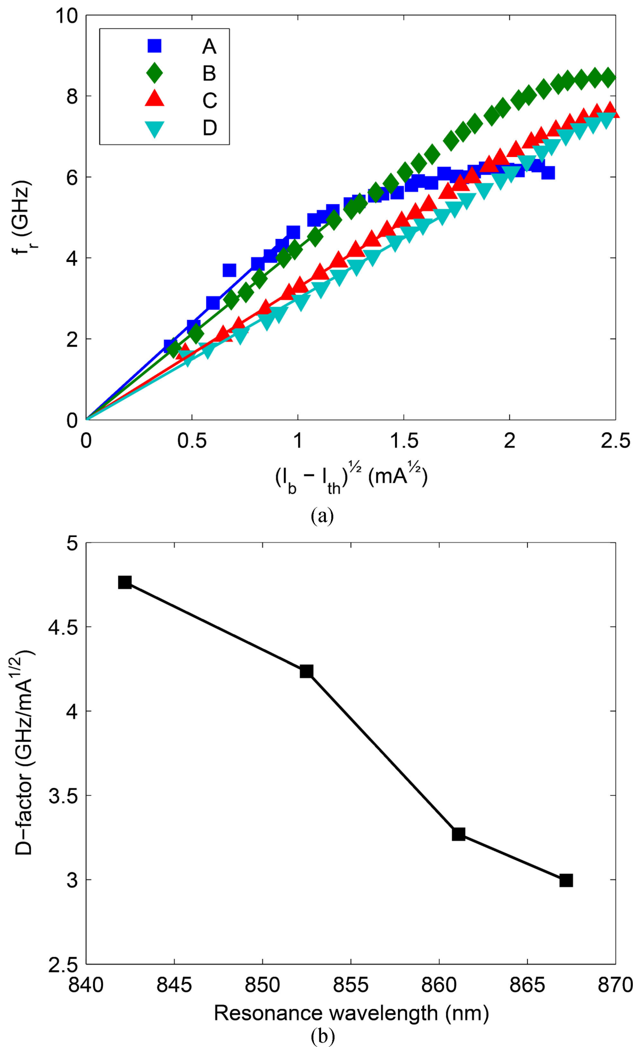

Fig. 11. (a) Resonance frequency versus square root of current above threshold at 25 °C with fits to extract the *D*-factors, which are shown versus resonance wavelength in (b).

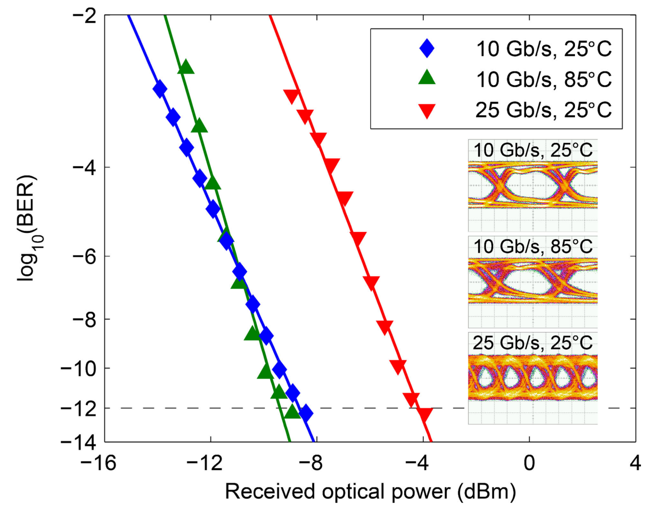

Fig. 12. Measured BER versus received optical power for a 5-μm oxide-aperture diameter HC-VCSEL with similar resonance wavelength as HC-VCSEL C at data rates up to 25 Gb/s at 25 °C and 10 Gb/s at 85 °C. Insets: Corresponding optical eye diagrams (scales: 100 mV/div and 20 ps/div).

generator (SHF 12103A) and fed to the HC-VCSEL through the high-speed probe. A high-speed bias-T was inserted before the probe to allow DC biasing of the HC-VCSEL. The light from the HC-VCSEL was coupled into a 1 m long OM4 multimode optical fiber using the AR coated lens package. The fiber was connected to a 30 GHz limiting photoreceiver (VI Systems R40-850) via a variable optical attenuator. The photoreceiver was finally connected to either an error analyzer (SHF 11100B) to measure the bit error ratio (BER) or a 70 GHz equivalent time sampling oscilloscope (Agilent Infiniium DCA-J 86100C) to record eye diagrams.

With a bias current of 4.5 mA, a modulation voltage of 350 $\mathrm{mV_{pp}}$, and the HC-VCSEL held at 25 °C, error-free transmission ($\mathrm{BER} < 10^{-12}$) was achieved at data rates up to 25 Gb/s with an extinction ratio (ER) of 5.6 dB (Fig. 12). At 85 °C, a bias current of 3.5 mA and modulation voltage of 180 $\mathrm{mV_{pp}}$ enabled error-free transmission at data rates up to 10 Gb/s ($\mathrm{ER} = 5.9$ dB). The lower bias current and modulation voltage used at 85 °C were required to maintain high modulation efficiency and avoid operation below threshold at the off-state. The same biasing and modulation conditions were also used with the HC-VCSEL held at 25 °C and modulated at 10 Gb/s for comparison, resulting in a reduction of the ER to 3.9 dB due to the lower threshold current. At 10 Gb/s, there is no power penalty when increasing the temperature from 25 to 85 °C due to the higher ER at 85 °C, but the power budget is 2.3 dB larger at 25 °C. However, increasing the data rate from 10 to 25 Gb/s at 25 °C results in a 4 dB power penalty.

V. Conclusion

By varying the bonding interface thickness of silicon-integrated hybrid-cavity VCSELs we have studied its impact on important static and dynamic performance parameters. The variable thickness offers the opportunity to either optimize performance (e.g. threshold current, output power, modulation bandwidth) at a specific ambient temperature or optimize for more temperature-stable performance.

With a 10-μm oxide-aperture diameter we reach an output power (modulation bandwidth) of 2.3 mW (10.0 GHz) at 25 °C and 0.9 mW (6.4 GHz) at 85 °C for HC-VCSELs with different interface thicknesses and detuning. The HC-VCSEL with the largest detuning of -15 nm (thickest bonding interface) also shows weak temperature dependencies of the threshold current and the modulation bandwidth over the temperature range 25–85 °C. We also found the thermal impedance to be independent of the thickness of the bonding interface, therefore being largely determined by the thermal conductivity of the dielectric DBR. Finally, we demonstrated error-free data transmission back-to-back at bit rates up to 25 and 10 Gb/s at 25 and 85 °C, respectively, using a 5-μm oxide-aperture diameter HC-VCSEL with moderately large gain-to-resonance detuning.

REFERENCES

[1] Z. Zhou, B. Yin, and J. Michel, "On-chip light sources for silicon photonics," *Light Sci. Appl.*, vol. 4, no. 11, Nov. 2015, Paper no. e358.

[2] K. Takaki *et al.*, "A recorded 62% PCE and low series and thermal resistance VCSEL with a double intra-cavity structure," in *Proc. IEEE Int. Semicond. Laser Conf.*, 2008, Paper no. PDP1.

[3] Y. Wang *et al.*, "Vertical-cavity surface-emitting laser flip-chip bonding to silicon photonics chip," in *Proc. IEEE Opt. Interconnects Conf.*, 2015, vol. 6, pp. 122–123.

[4] R. Chen *et al.*, "Nanolasers grown on silicon," *Nature Photon.*, vol. 5, no. 3, pp. 170–175, Mar. 2011.

[5] S. Keyvaninia *et al.*, "Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate," *Opt. Mater. Express*, vol. 3, no. 1, pp. 35–46, Jan. 2013.

[6] Y. Tsunemi *et al.*, "1.55-μm VCSEL with polarization-independent HCG mirror on SOI," *Opt. Express*, vol. 21, no. 23, pp. 28685–28692, Nov. 2013.

[7] J. Ferrara, W. Yang, L. Zhu, P. Qiao, and C. J. Chang-Hasnain, "Heterogeneously integrated long-wavelength VCSEL using silicon high contrast grating on an SOI substrate," *Opt. Express*, vol. 23, no. 3, pp. 2512–2523, Feb. 2015.

[8] G. C. Park *et al.*, "Hybrid vertical-cavity laser with lateral emission into a silicon waveguide," *Laser Photon. Rev.*, vol. 9, no. 3, pp. L11–L15, May 2015.

[9] D. A. Louderback *et al.*, "VCSELs with monolithic coupling to internal horizontal waveguides using integrated diffraction gratings," *Electron. Lett.*, vol. 40, no. 17, pp. 1064–1065, Aug. 2004.

[10] E. P. Haglund *et al.*, "Silicon-integrated short-wavelength hybrid-cavity VCSEL," *Opt. Express*, vol. 23, no. 26, pp. 33634–33640, Dec. 2015.

[11] E. P. Haglund *et al.*, "20-Gb/s modulation of silicon-integrated short-wavelength hybrid-cavity VCSELs," *IEEE Photon. Technol. Lett.*, vol. 28, no. 8, pp. 856–859, Apr. 2016.

[12] D. B. Young *et al.*, "Enhanced performance of offset-gain high-barrier vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, vol. 29, no. 6, pp. 2013–2022, Jun. 1993.

[13] H. Li *et al.*, "Impact of the quantum well gain-to-cavity etalon wavelength offset on the high temperature performance of high bit rate 980-nm VCSELs," *IEEE J. Quantum Electron.*, vol. 50, no. 8, pp. 613–621, Aug. 2014.

[14] G. R. Hadley, "Effective index model for vertical-cavity surface-emitting lasers," *Opt. Lett.*, vol. 20, no. 13, pp. 1483–1485, Jul. 1995.

[15] R. Michalzik, "VCSEL fundamentals," in *VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers*, R. Michalzik, Ed. Berlin, Heidelberg: Springer, 2013, pp. 19–75.

[16] P. P. Baveja *et al.*, "Assessment of VCSEL thermal rollover mechanisms from measurements and empirical modeling," *Opt. Express*, vol. 19, no. 16, pp. 15490–15505, Aug. 2011.

[17] W. Nakwaski, "Thermal aspects of efficient operation of vertical-cavity surface-emitting lasers," *Opt. Quantum Electron.*, vol. 28, no. 4, pp. 335–352, Apr. 1996.

[18] L. Coldren and S. Corzine, *Diode Lasers and Photonic Integrated Circuits*. New York, NY, USA: Wiley, 1995.

[19] E. P. Haglund, P. Westbergh, J. S. Gustavsson, and A. Larsson, "Impact of damping on high-speed large signal VCSEL dynamics," *J. Light. Technol.*, vol. 33, no. 4, pp. 795–801, Feb. 2015.

[20] A. Larsson, "Advances in VCSELs for communication and sensing," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 6, pp. 1552–1567, Nov. 2011.

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