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Compound Semiconductor Week 2016

Heterogeneous Integration of InP Devices on Silicon

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Abstract **— In the paper, we review our work on heterogeneous integration of InP photonic devices on silicon. We elaborate on two integration technologies that have been widely explored in the Photonics Research group, i.e. the relatively mature adhesive bonding based integration scheme and a newly demonstrated buffer-less epitaxial growth approach. Based on these techniques, we describe a broad range of photonic devices including mode-locked lasers, high speed directly modulated distributed feedback lasers, electro-absorption modulators, photodetectors, super-luminescent light emitting diodes, etc.**

Keywords—heterogeneous integration; epitaxial growth; optical communication; photonic integration, optical sensing

I. INTRODUCTION

Emerging as an attractive integrated photonics platform, silicon photonics uses 200mm or 300mm CMOS fabrication infrastructure to manufacture compact photonic ICs with capability of mass production and hence low cost[1]. In addition, the co-integration of electronics with photonics is also becoming a reality[2]. While 56Gbps photodetectors and optical modulators are readily available[3], an efficient way of light generation on chip becomes the fundamental limit that hinders the wide adoption of silicon photonics. Here, we review two technologies that can integrate InP-based laser sources and other opto-electronic components on silicon in a scalable way.

II. HETEROGENEOUS INTEGRATION TECHNOLOGIES

Over the past decade, the bonding technology has been well-developed[4]. By using adhesive agents, benzocyclobutene (BCB) in this case, we are able to realize wafer scale integration of InP-based epitaxial layer structures on silicon with high yield, and an example of a silicon photonic chip with multiple bonded InP dies can be found in Fig. 1. After the III-V material is bonded onto silicon photonic ICs, the post-processed photonic components are lithographically aligned to the underlying silicon waveguide circuit (see Fig. 1). As a near-/mid-term solution, the adhesive bonding technology suits well the primary target of silicon photonics, i.e. optical interconnects, with the possibility of scaling from the first commercially available 4x28G transceivers to 400G or 1.6T transceivers by integrating arrays of III-V lasers on silicon in a cost-effective way. We will elaborate on some photonic devices that were demonstrated in the past few years, including single wavelength InP DFB lasers, tunable extended cavity lasers, multi-wavelength lasers, modelocked lasers, but also electro-absorption modulators and photodetectors (see an example of MLL in Fig. 2). Also GaAs VCSELs have recently been integrated onto a silicon photonics platform. Beyond the field of optical interconnects, silicon photonics is expected to also have an impact on the field of optical sensing. Such optical spectroscopic sensor systems integrated on a silicon chip require the integration of light sources and photodetectors operating at wavelengths outside the telecommunication wavelength window. In this paper we will present the integration of broadband waveguide coupled LEDs and spectrometer photodetector arrays covering the 1.5 to 4 μm wavelength range (see an example of type II InP QW photodiodes in Fig. 3).

As a long-term solution, the possibility of growing III-V materials directly on silicon enables to fully benefit from the economies of scale offered by processing in advanced CMOS foundries on large wafers. For this to become reality considerable hurdles need to be overcome: the large lattice mismatch (εInP/Si = 8.06%), the difference in thermal expansion and the different polarity of the materials result in large densities of crystal defects. Recently, boosted by the renewed interest of the electronics industry in using high-mobility compound semiconductors in next-generation CMOS, considerable progress has been made on low-defect-density direct growth of III-Vs on silicon. Well-optimized epitaxial technology confines the defect layer within 20 nm at the interface of InP and silicon. Such buffer-less growth techniques has led to the recent demonstration of an InP DFB laser array grown directly on silicon (Fig. 4)[5]. The possibility of using well-established in-plane laser configuration and the top-down integration scheme provide a route towards the monolithic integration of dense arrays of III–V laser sources with Si photonic circuits.

III. REFERENCES

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2. Sun, Chen, et al. "Single-chip microprocessor that communicates directly using light." *Nature* 528.7583 (2015): 534-538.
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5. Wang, Zhechao, et al. "Room-temperature InP distributed feedback laser array directly grown on silicon." *Nature Photonics* 9.12 (2015): 837-842.

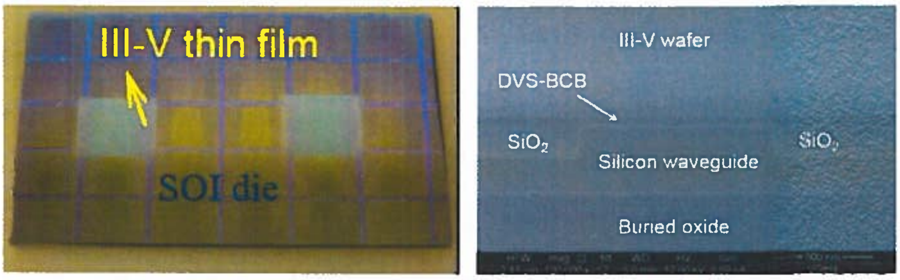


Fig. 1 (left) Multiple InP dies bonded on a silicon photonic IC. (right) A scanning electron microscope (SEM) image of the cross-section of the InP wafer bonded on top of a silicon waveguide.

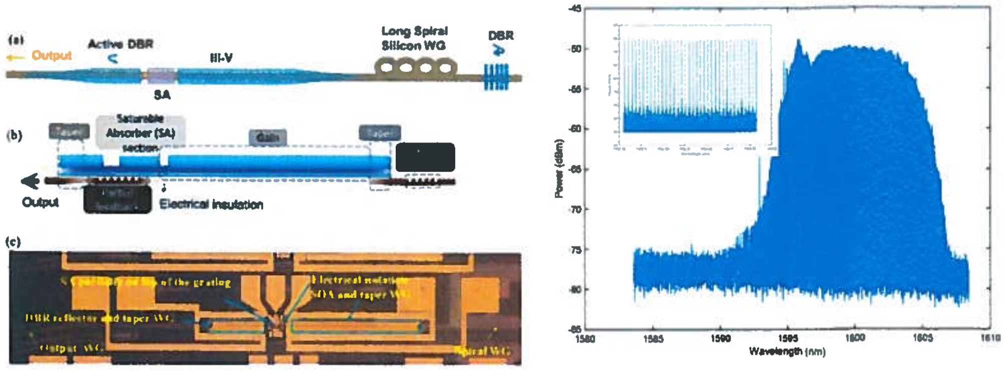


Fig. 2 (left) Layout of the III–V-on-silicon mode-locked laser cavity: (a) top view; (b) longitudinal cross-section. A microscope image of the fabricated device is shown in (c). (right) High-resolution optical spectrum of the ps output pulse (20 MHz spectral resolution). Insert shows a zoom-in image of the optical spectrum, representing an optical frequency comb with 1 GHz spacing.

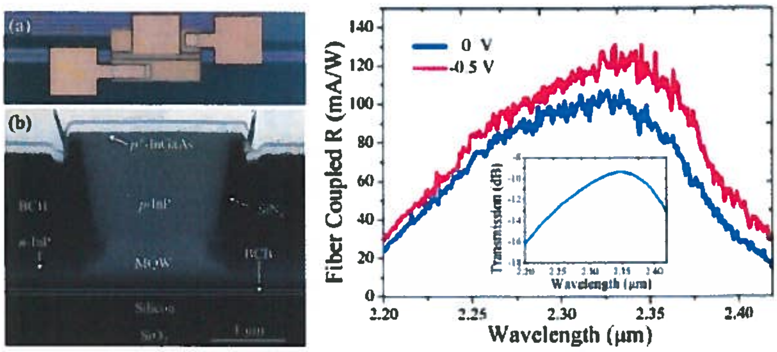


Fig. 3 (left) (a) Microscope image of the heterogeneously integrated type-II quantum well photodiode; (b) SEM image of the cross section of the fabricated devices. (right) Dependence of the fiber coupled responsivity (R) on the input laser wavelength under reverse bias of 0 V and 0.5 V, the inset figure shows the grating coupler efficiency as a reference.

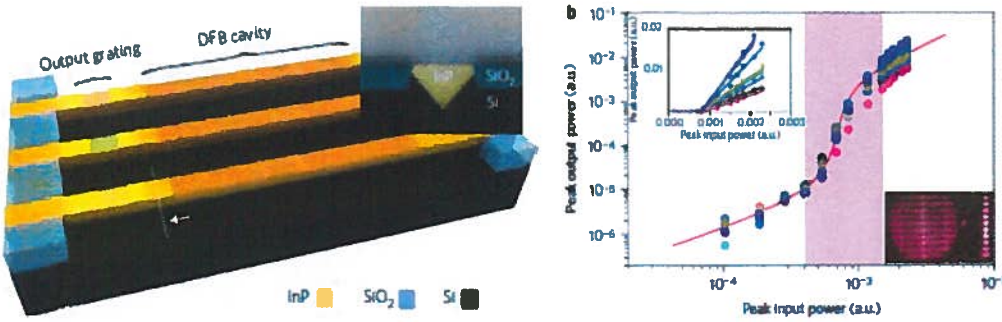
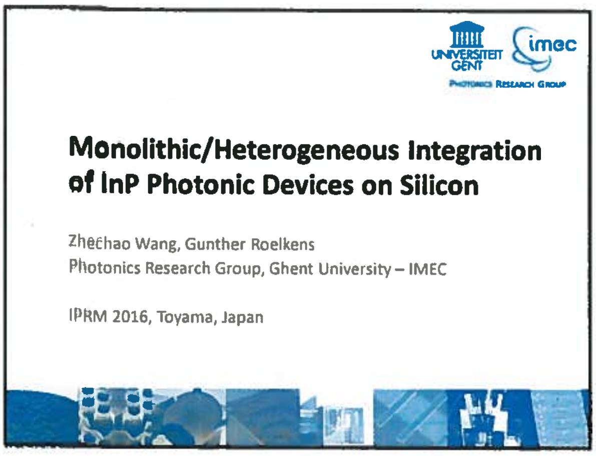


Fig. 4 (left) Schematic plot of the InP DFB laser array integrated on silicon. Insert: SEM image of a InP-on-Si waveguide (right) Measured L–L curves of an array of ten DFB lasers. Inset (top): linear-scale version of the ten log-scale L–L curves presented in the main panel. Inset (bottom): camera-recorded photoluminescence image of ten working lasers under a large-area pumping condition.



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Monolithic/Heterogeneous Integration of InP Photonic Devices on Silicon

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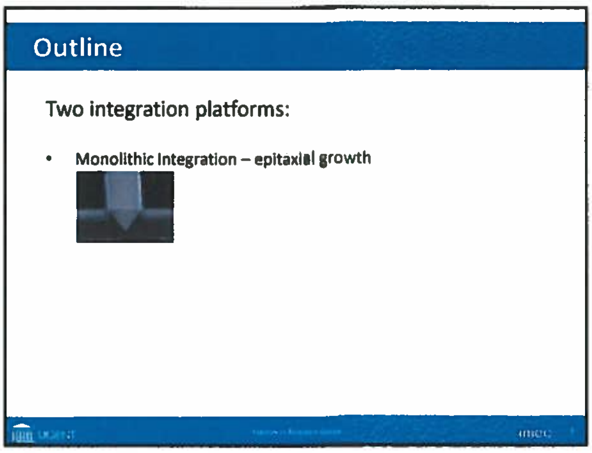
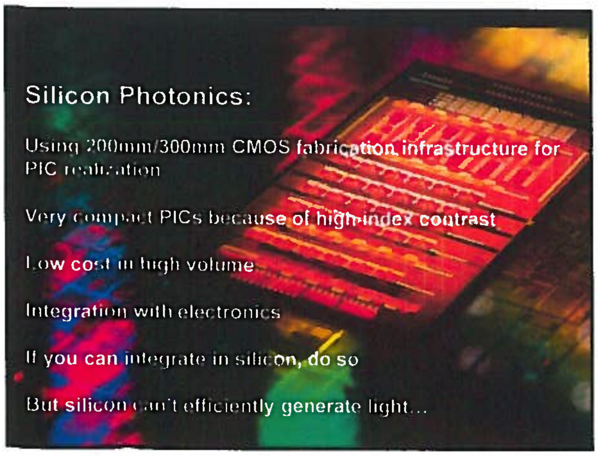
IPRM 2016, Toyama, Japan



Outline

Two integration platforms:

- Monolithic integration – epitaxial growth



Silicon Photonics:

Using 200mm/300mm CMOS fabrication infrastructure for PIC realization

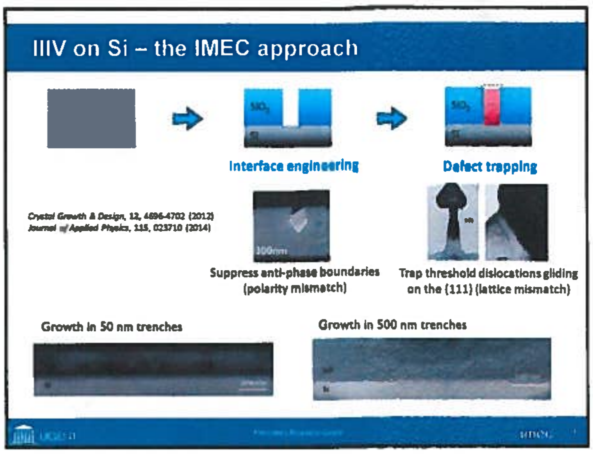
Very compact PICs because of high-index contrast

Low cost in high volume

Integration with electronics

If you can integrate in silicon, do so

But silicon can't efficiently generate light…



IIIV on Si – the IMEC approach

Interface engineering

Defect trapping

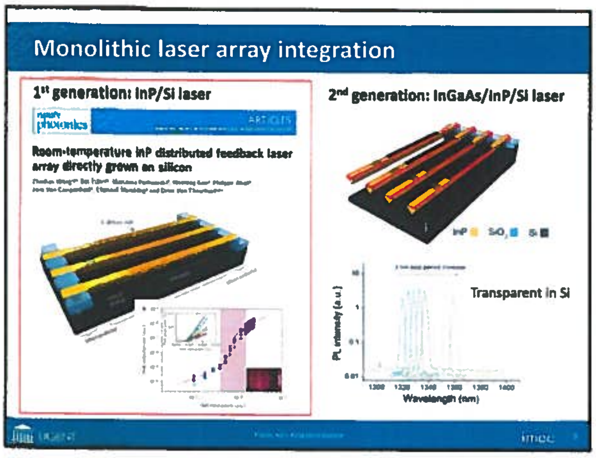
Crystal Growth & Design, 12, 4696-4702 (2012)
Journal of Applied Physics, 115, 023710 (2014)

Suppress anti-phase boundaries (polarity mismatch)

Trap threshold dislocations gliding on the {111} (lattice mismatch)

Growth in 50 nm trenches

Growth in 500 nm trenches



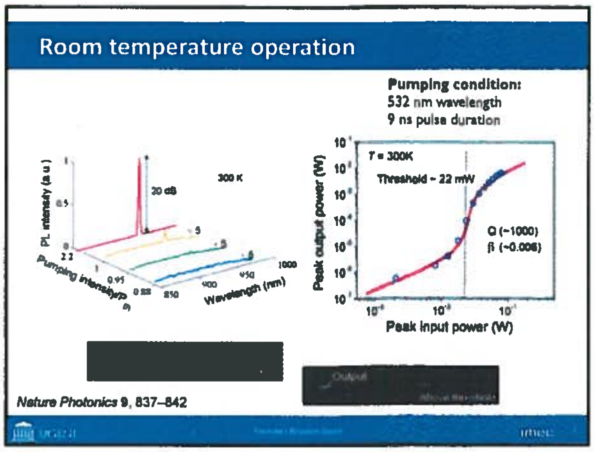
Monolithic laser array integration

1st generation: InP/Si laser

Room-temperature InP distributed feedback laser array directly grown on silicon

2nd generation: InGaAs/InP/Si laser

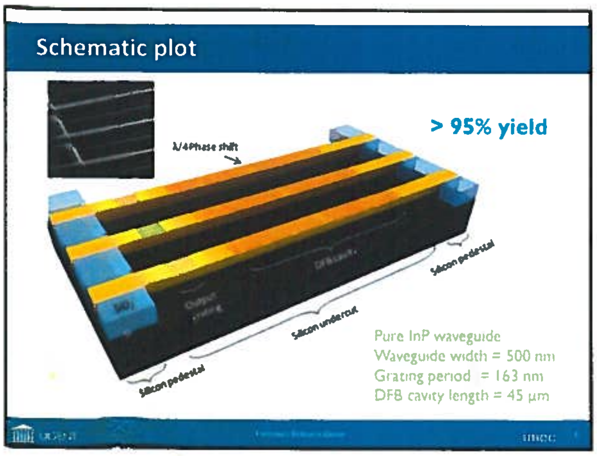
Transparent in Si



Room temperature operation

Pumping condition:
532 nm wavelength
9 ns pulse duration

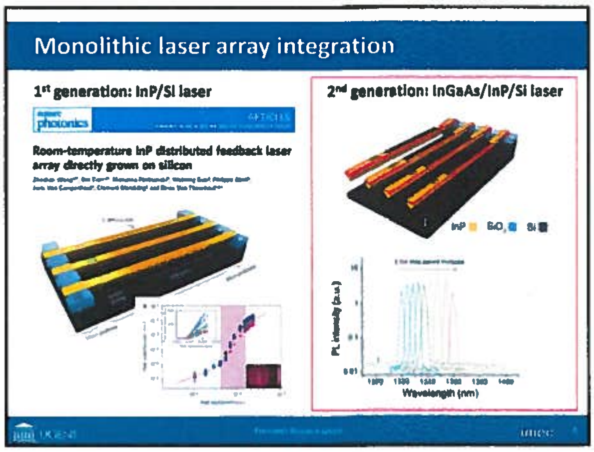
Nature Photonics 9, 837–842



Schematic plot

> 95% yield

Pure InP waveguide
Waveguide width = 500 nm
Grating period = 163 nm
DFB cavity length = 45 µm



Monolithic laser array integration

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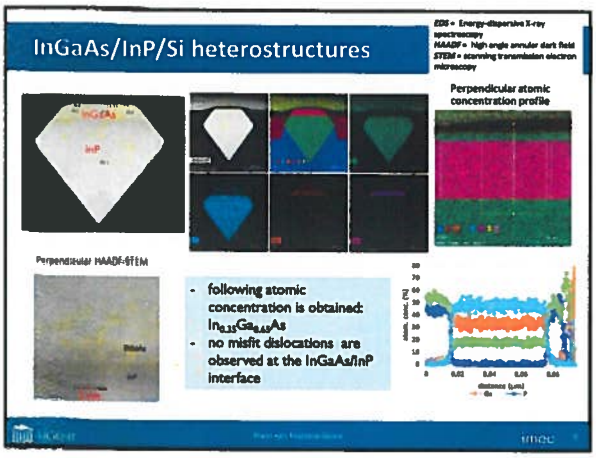
Room-temperature InP distributed feedback laser array directly grown on silicon

2nd generation: InGaAs/InP/Si laser



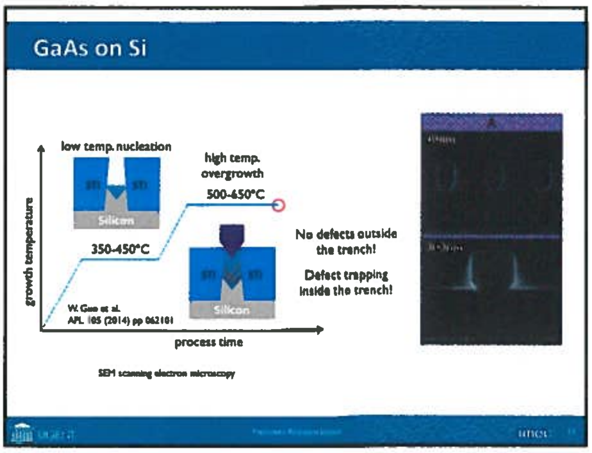
InGaAs/InP/Si heterostructures

EDS = Energy-dispersive X-ray spectroscopy
HAADF = high angle annular dark field
STEM = scanning transmission electron microscopy

Perpendicular atomic concentration profile

Perpendicular HAADF-STEM

- following atomic concentration is obtained: $In_{0.15}Ga_{0.85}As$
- no misfit dislocations are observed at the InGaAs/InP interface



GaAs on Si

low temp. nucleation

high temp. overgrowth

500-650°C

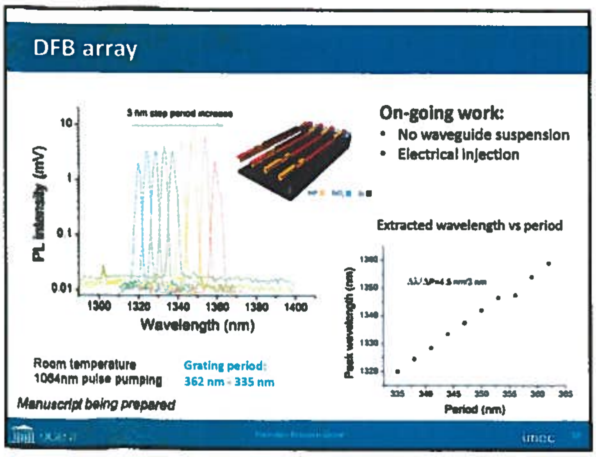
350-450°C

No defects outside the trench!

Defect trapping inside the trench!

W. Guo et al.
APL 105 (2014) pp 062101

SEM scanning electron microscopy



DFB array

On-going work:

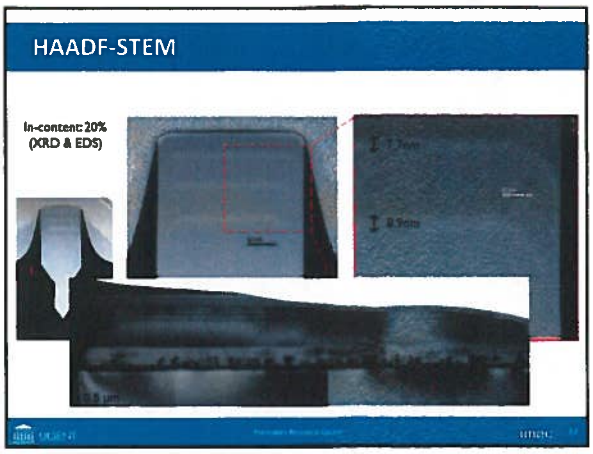
- No waveguide suspension
- Electrical injection

Room temperature
1064nm pulse pumping

Grating period:
362 nm - 335 nm

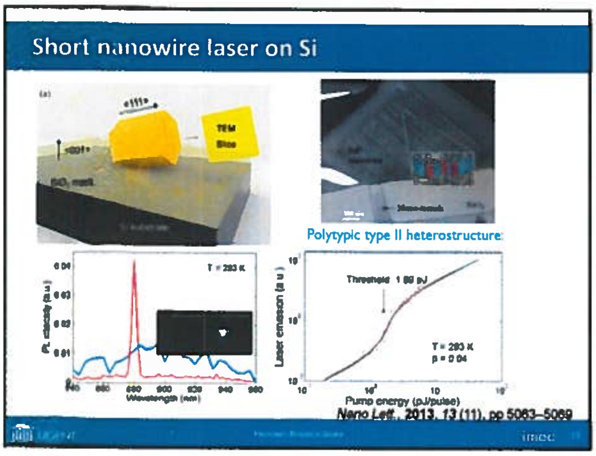
Manuscript being prepared

Extracted wavelength vs period



HAADF-STEM

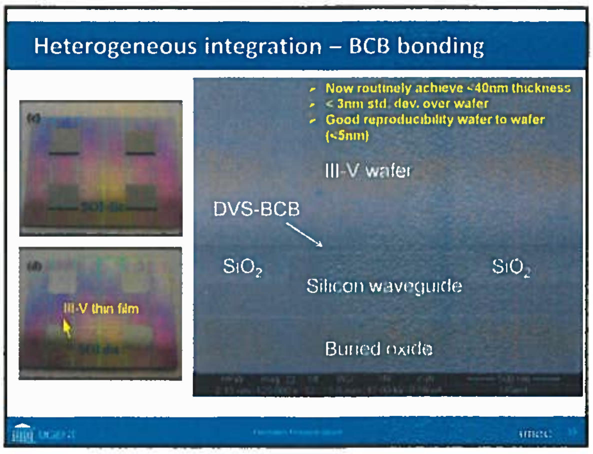
In-content: 20%
(XRD & EDS)



Short nanowire laser on Si

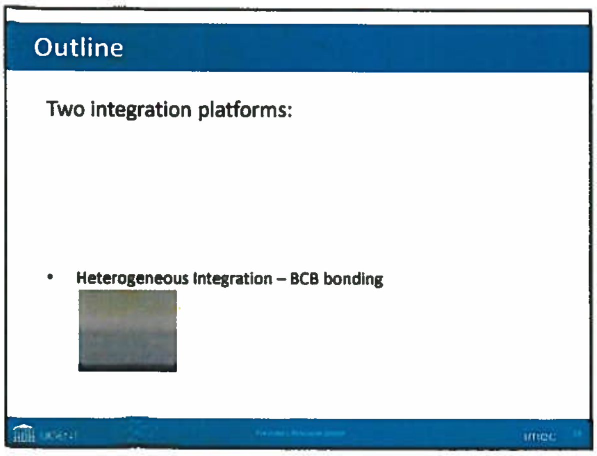
Polytypic type II heterostructure

Nano Lett., 2013, *13* (11), pp 5063–5069



Heterogeneous integration – BCB bonding

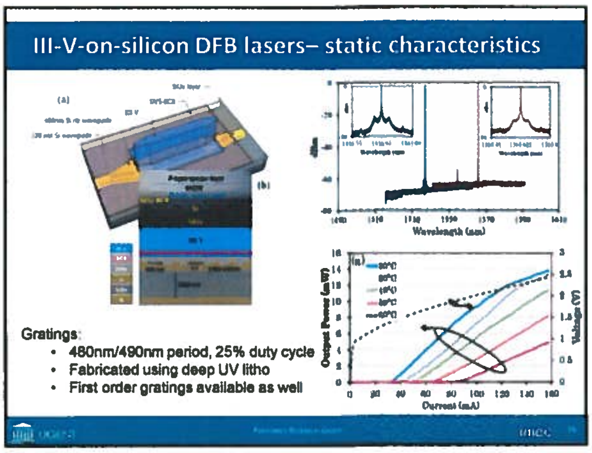
- Now routinely achieve <40nm thickness
- < 3nm std. dev. over wafer
- Good reproducibility wafer to wafer (<5nm)



Outline

Two integration platforms:

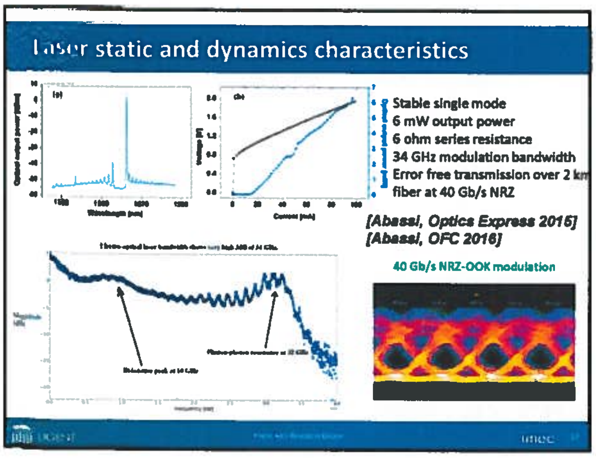
- Heterogeneous Integration – BCB bonding



III-V-on-silicon DFB lasers– static characteristics

Gratings:

- 480nm/490nm period, 25% duty cycle
- Fabricated using deep UV litho
- First order gratings available as well

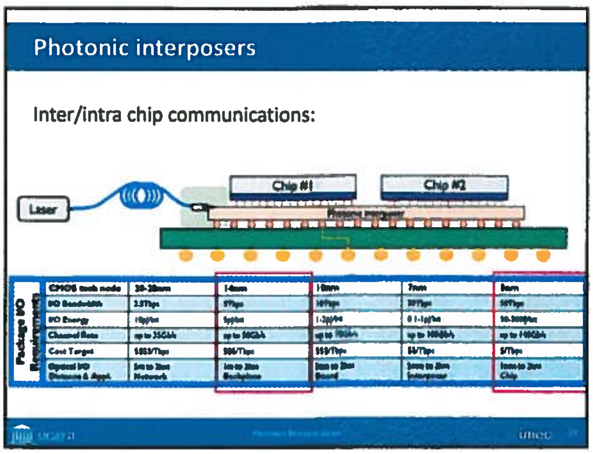


Laser static and dynamics characteristics

- Stable single mode
- 6 mW output power
- 6 ohm series resistance
- 34 GHz modulation bandwidth
- Error free transmission over 2 km fiber at 40 Gb/s NRZ

[Abassi, Optics Express 2016]
[Abassi, OFC 2016]

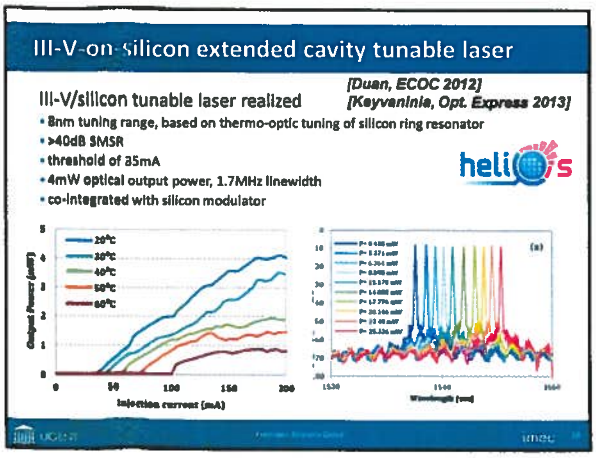
40 Gb/s NRZ-OOK modulation



Photonic interposers

Inter/intra chip communications:

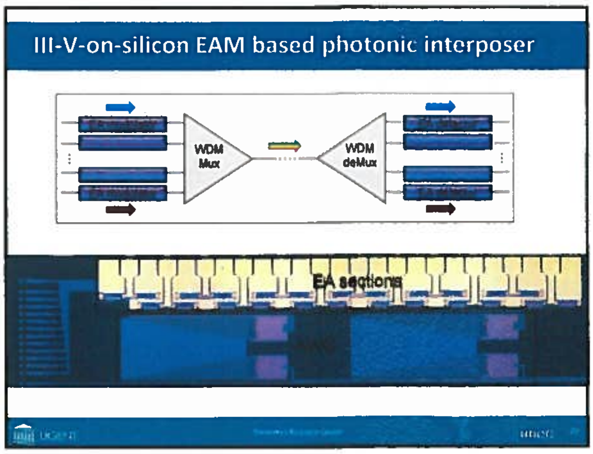
Package I/O Requirements					
CMOS tech node	20-28nm	14nm	10nm	7nm	5nm
I/O Bandwidth	2.5Tbps	5Tbps	10Tbps	20Tbps	50Tbps
I/O Energy	10pJ/bit	5pJ/bit	1-2pJ/bit	0.1-1pJ/bit	10-300fJ/bit
Channel Rate	up to 25Gb/s	up to 50Gb/s	up to 100Gb/s	up to 100Gb/s	up to 140Gb/s
Cost Target	$$$$/Tbps	$$$/Tbps	$$$/Tbps	$$/Tbps	$/Tbps
Optical I/O Distance & Appl.	5m to 2km Network	1m to 2m Backplane	1cm to 2m Board	1mm to 2cm Interposer	1mm to 2cm Chip



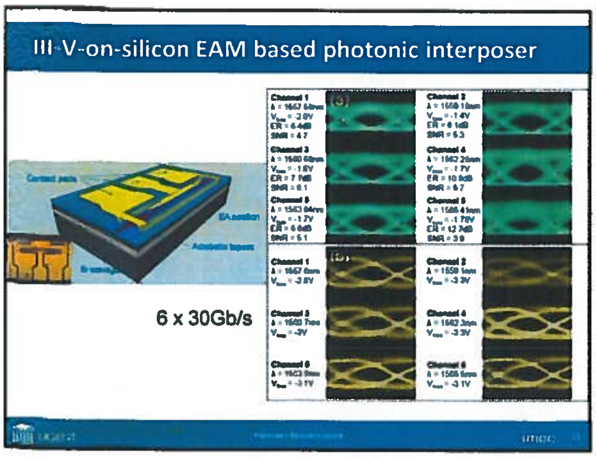
III-V-on-silicon extended cavity tunable laser

[Duan, ECOC 2012]
[Keyvaninia, Opt. Express 2013]

III-V/silicon tunable laser realized
- 8nm tuning range, based on thermo-optic tuning of silicon ring resonator
- >40dB SMSR
- threshold of 35mA
- 4mW optical output power, 1.7MHz linewidth
- co-integrated with silicon modulator

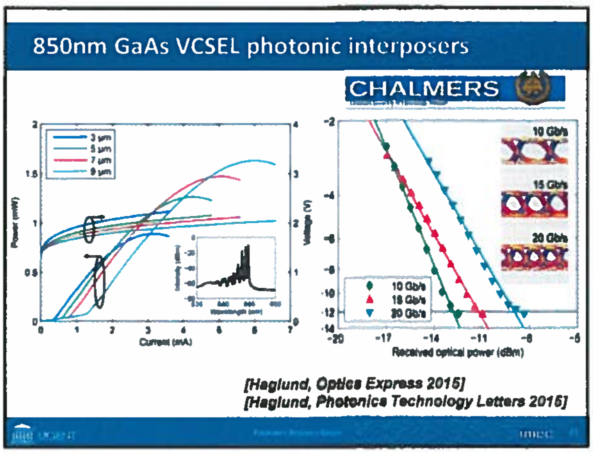


III-V-on-silicon EAM based photonic interposer



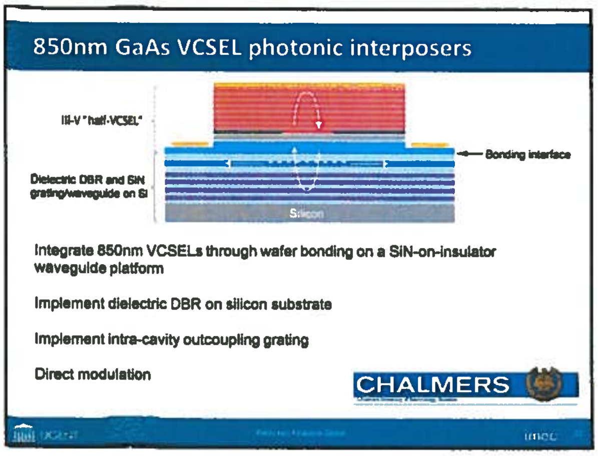
III-V-on-silicon EAM based photonic interposer

6 x 30Gb/s



850nm GaAs VCSEL photonic interposers

[Haglund, Optics Express 2015]
[Haglund, Photonics Technology Letters 2015]



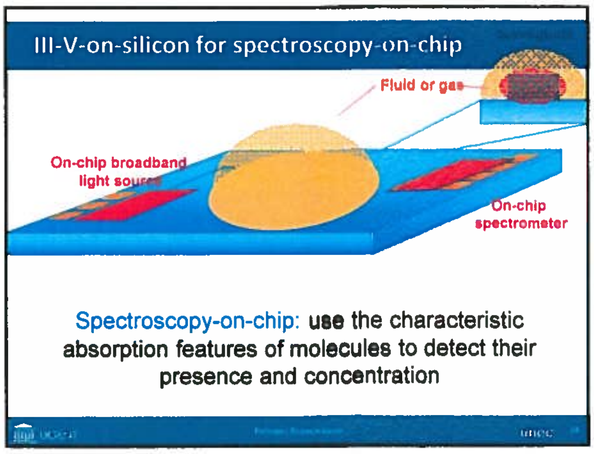
850nm GaAs VCSEL photonic interposers

Integrate 850nm VCSELs through wafer bonding on a SiN-on-insulator waveguide platform

Implement dielectric DBR on silicon substrate

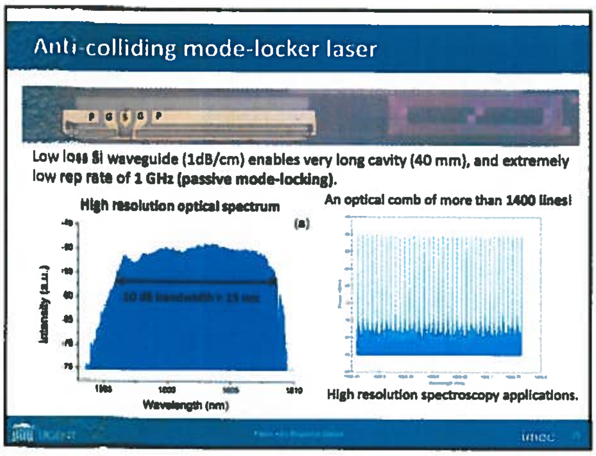
Implement intra-cavity outcoupling grating

Direct modulation



III-V-on-silicon for spectroscopy-on-chip

Spectroscopy-on-chip: use the characteristic absorption features of molecules to detect their presence and concentration



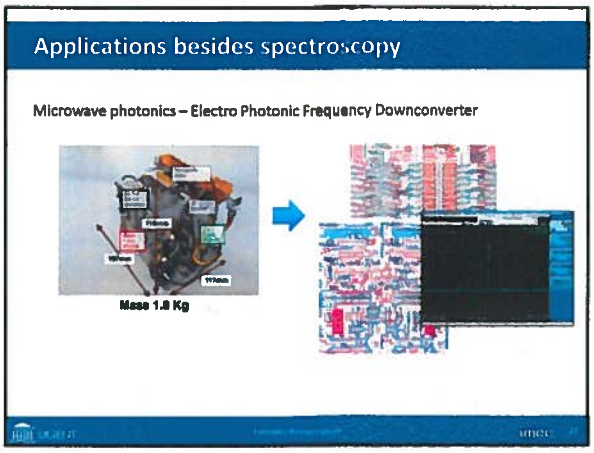
Anti-colliding mode-locker laser

Low loss Si waveguide (1dB/cm) enables very long cavity (40 mm), and extremely low rep rate of 1 GHz (passive mode-locking).

High resolution optical spectrum

An optical comb of more than 1400 lines!

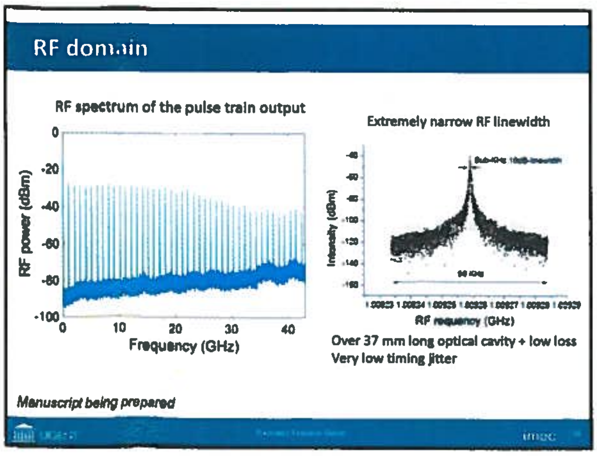
High resolution spectroscopy applications.



Applications besides spectroscopy

Microwave photonics – Electro Photonic Frequency Downconverter

Mass 1.8 Kg



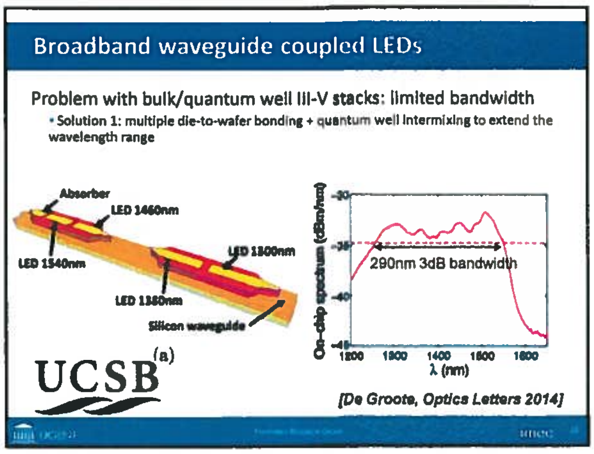
RF domain

RF spectrum of the pulse train output

Extremely narrow RF linewidth

Over 37 mm long optical cavity + low loss
Very low timing jitter

Manuscript being prepared

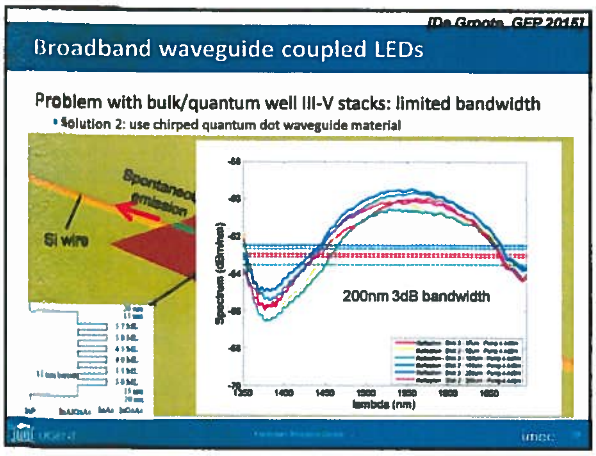


Broadband waveguide coupled LEDs

Problem with bulk/quantum well III-V stacks: limited bandwidth

- Solution 1: multiple die-to-wafer bonding + quantum well intermixing to extend the wavelength range

[De Groote, Optics Letters 2014]

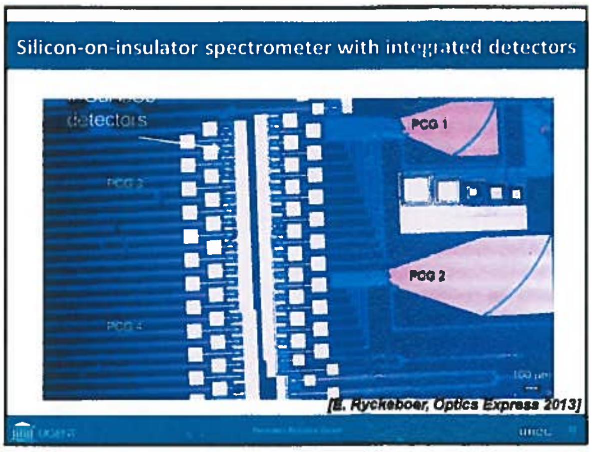


[De Groote, GFP 2015]

Broadband waveguide coupled LEDs

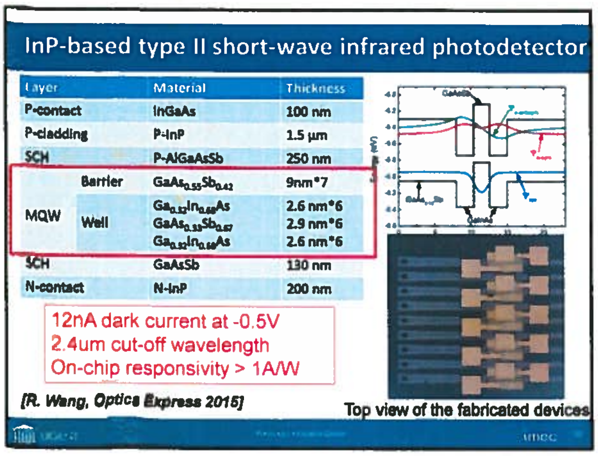
Problem with bulk/quantum well III-V stacks: limited bandwidth

- Solution 2: use chirped quantum dot waveguide material



Silicon-on-insulator spectrometer with integrated detectors

[E. Ryckeboer, Optics Express 2013]



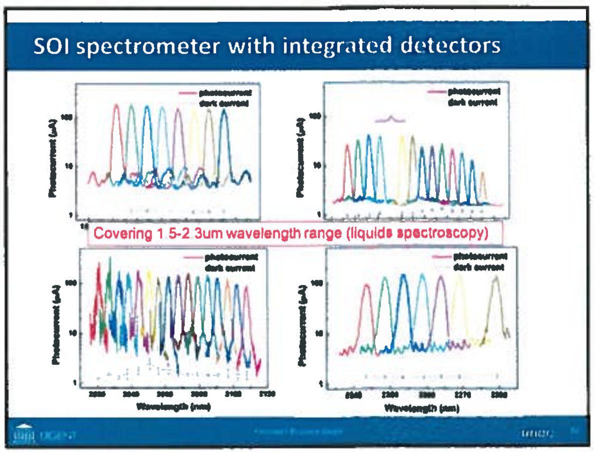
InP-based type II short-wave infrared photodetector

Layer		Material	Thickness
P-contact		InGaAs	100 nm
P-cladding		P-InP	1.5 µm
SCH		P-AlGaAsSb	250 nm
MQW	Barrier	GaAs$_{0.55}$Sb$_{0.42}$	9nm*7
	Well	Ga$_{0.32}$In$_{0.68}$As GaAs$_{0.33}$Sb$_{0.67}$ Ga$_{0.32}$In$_{0.68}$As	2.6 nm*6 2.9 nm*6 2.6 nm*6
SCH		GaAsSb	130 nm
N-contact		N-InP	200 nm

12nA dark current at -0.5V
2.4um cut-off wavelength
On-chip responsivity > 1A/W

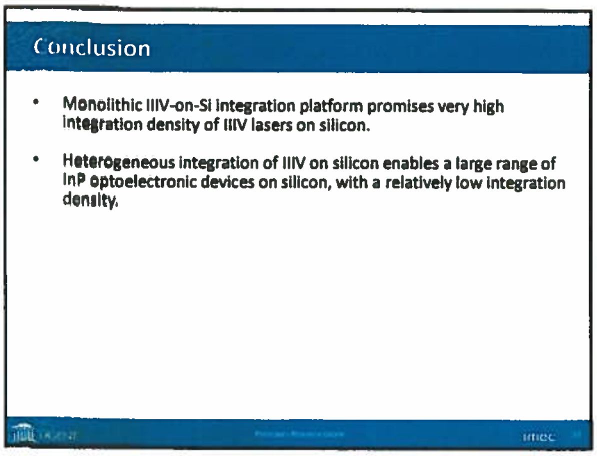
[R. Wang, Optics Express 2015]

Top view of the fabricated devices



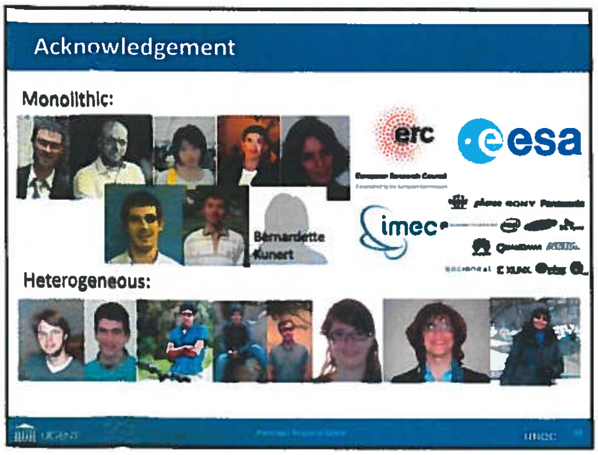
SOI spectrometer with integrated detectors

Covering 1.5-2.3um wavelength range (liquids spectroscopy)



Conclusion

- Monolithic IIIV-on-Si integration platform promises very high integration density of IIIV lasers on silicon.
- Heterogeneous integration of IIIV on silicon enables a large range of InP optoelectronic devices on silicon, with a relatively low integration density.



Acknowledgement

Monolithic:

Bernardette Kunert

Heterogeneous:

Foreword

We welcome you to Compound Semiconductor Week (CSW) 2016 in Toyama, Japan.

Following the great success of CSW2015 in Santa Barbara, USA and CSW2014 in Montpellier, France, CSW2016 is a joint venue for the 43rd International Symposium on Compound Semiconductors (ISCS) and the 28th International Conference on Indium Phosphide and Related Materials (IPRM). CSW2016 aims to be the premier forum for science, technology, and applications in all areas of compound semiconductors.

ISCS is the preeminent international conference in the field of III-V, II-VI, and IV-IV semiconductors. The ISCS series was initiated in 1966 under the name of "International Symposium on GaAs". Later, in 1970 (the 3rd conference), the name of the conference was changed to "International Symposium on GaAs and Related Compounds" in order to cover not only GaAs but also GaP, InP, and their alloys in the scope of the conference. Since 1994 (the 21st conference), the conference name has been changed to "International Symposium on Compound Semiconductors (ISCS)". The current name reflects the broadening of the conference scope due to the wide variety of compound semiconductors vital to materials for modern electronic and optoelectronic devices. IPRM is the major conference worldwide on Indium Phosphide and Related Materials, from physics to applications. The first conference was held in in 1989, Norman, OK, USA. The IPRM technical conference and exhibit is held yearly and its location alternates between North America, the Pacific Rim and Europe.

CSW2016 will start on Sunday, the 26th of June with two short courses, given by Prof. Susumu Noda, Kyoto University, on *Manipulation of Photons by Photonic Crystals*, and by Prof. Akira Ohtomo, Tokyo Institute of Technology, and Dr. Masataka Higashiwaki, National Institute of Information and Communications Technology, on *New Perspectives for Oxide Semiconductors and Their Applications.*

On Monday, the 27th of June, CSW2016 will open with plenary sessions addressing recent and important developments in compound semiconductor research. The four distinguished plenary speakers this year are Prof. Jerome Faist, ETH Zurich, with a talk on *Quantum Cascade Laser Frequency Combs: Physics and Applications*; Prof. Hideo Hosono, Tokyo Institute of Technology, who will discuss *Novel Oxide Semiconductors for OLEDs and Catalysis*; Prof. Jesús A. del Alamo, Massachusetts Institute of Technology, who will speak about *Nanometer-Scale III-V CMOS*; and Dr. Hajime Shoji, Sumitomo Electric Industries, Ltd., who will present his vision in a talk on *InP-Based Integrated Optical Devices – Present and Future –*. The opening session will be followed by the ISCS/IPRM awards session.

At CSW2016, 37 invited talks, 142 contributed oral and 169 poster papers will be presented during the course of both the ISCS and IPRM conferences. We are confident that you will find a lot of interesting papers in your related fields, while the industrial exhibition will offer you opportunities to discover new products. Finally, joint excursions and the conference dinner on Wednesday will complete CSW 2016. The proceedings are published in IEEE conference proceedings (IEEE Xplore) and we are also planning to publish a special conference issue in Physica Status Solidi (a/b) to highlight the most exciting new results presented at CSW2016.