Invited Paper

Hybrid vertical-cavity laser integration on silicon

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ABSTRACT

The hybrid vertical-cavity laser is a potential low current, high-efficiency, and small footprint light source for silicon photonics integration. As part of the development of such light sources we demonstrate hybrid-cavity VCSELs (HC-VCSELs) on silicon where a GaAs-based half-VCSEL is attached to a dielectric distributed Bragg reflector on silicon by adhesive bonding. HC-VCSELs at 850 nm with sub-mA threshold current, >2 mW output power, and 25 Gbit/s modulation speed are demonstrated. Integration of short-wavelength lasers will enable fully integrated photonic circuits on a silicon-nitride waveguide platform on silicon for applications in life science, bio-photonics, and short-reach optical interconnects.

Keywords: hybrid vertical-cavity, vertical-cavity surface-emitting laser, heterogeneous integration, photonic integration, silicon photonics

1. INTRODUCTION

Integration of light sources on silicon enables fully integrated silicon photonic circuits with a high degree of functionality and performance complexity for various applications [1]. Among the possible light source integration technologies, the hybrid vertical-cavity laser (HVCL) by heterogeneous integration is attractive as it has the potential for low drive current, high efficiency, and small footprint [2-4]. Coupling to an in-plane waveguide can be accomplished by e.g. an intra-cavity waveguide with a weak diffraction grating (Fig.1) [5].

We have developed a technology for hybrid-cavity VCSEL (HC-VCSEL) integration where a GaAs-based half-VCSEL is attached to a dielectric distributed Bragg reflector (DBR) on silicon by adhesive bonding (Fig.2) [6-8]. While this device does not yet contain elements for coupling to an in-plane waveguide, it lends itself to the development and implementation of the integration concept. HC-VCSELs at 850 nm with sub-mA threshold current, >2 mW output power, and 25 Gbit/s modulation speed are demonstrated. In addition, we show that the thickness of the bonding interface can be used to optimize a certain performance parameter at a given temperature or to minimize the variation of performance over temperature. Integration of such short-wavelength light sources on a silicon-nitride waveguide platform on silicon may enable fully integrated silicon photonic circuits for applications in life science, bio-photonics, and short-reach optical interconnects.

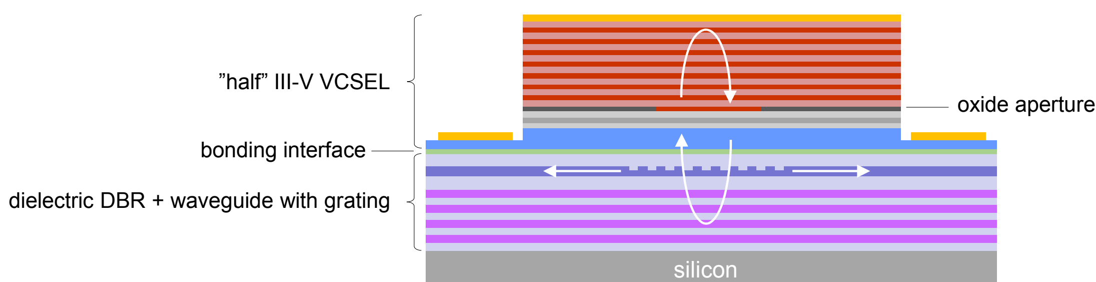

Figure 1. Schematic cross-section of a HVCL with an intra-cavity waveguide with a diffraction grating for tapping off power to the in-plane waveguide. The III-V part is bonded to the Si-based part using adhesive bonding.

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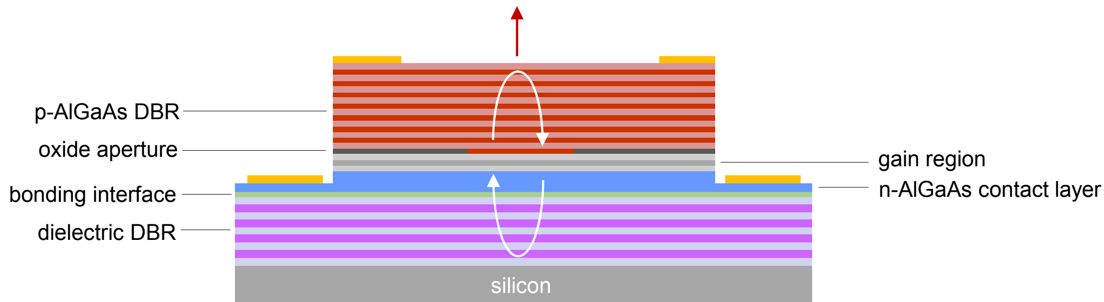

Figure 2. Schematic cross-section of the HC-VCSEL. The III-V part is bonded to the Si-based part using adhesive bonding.

2. CONCEPT AND DESIGN

The HC-VCSEL cavity consists of a III-V part (a semiconductor DBR and active region) and a Si-based part (a dielectric DBR on Si) and is therefore a hybrid cavity (Fig.2). The III-V part contains an *n*-doped AlGaAs contact layer, an InGaAs/AlGaAs multi-quantum well (QW) active region, a *p*-doped $Al_{0.98}Ga_{0.02}As$ layer for the formation of an oxide aperture, and a *p*-doped AlGaAs DBR. The dielectric DBR is a 20-pair SiO_2/Ta_2O_5 DBR. Between the parts is a thin layer of SiO_2 (deposited on the dielectric DBR) and an ultra-thin layer of divinylsiloxane-bis-benzocyclobutene (DVS-BCB). The DVS-BCB layer is used as the adhesive bonding agent [9]. The two layers define the bonding interface, where the thickness of the DVS-BCB layer is kept constant while the thickness of the SiO_2 layer is used to control the interface thickness and therefore the length of the cavity, the resonance wavelength, and the offset between the resonance and gain peak wavelengths.

The optical cavity properties were analyzed using a 1D effective index model [10]. The intensity of the optical standing-wave along the optical axis of the cavity is shown in Fig.3. Important cavity parameters at a resonance wavelength of 845 nm are listed in Table 1. The intra-cavity loss is due to free-carrier absorption in the *n*-doped contact layer and the *p*-doped DBR. The variations of resonance wavelength and threshold gain with bonding interface thickness are shown in Fig.4. Over a wavelength range of 35 nm (830-865 nm), the threshold gain is below 1000 cm^{-1}, which should allow for low threshold currents.

More details on the design and results from the simulations can be found in [6-8].

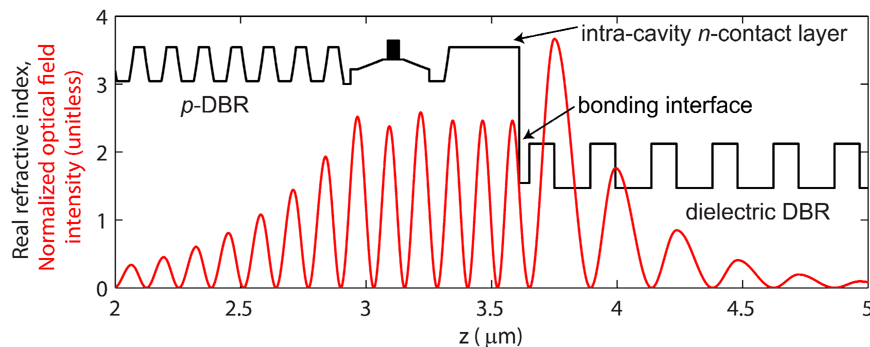

Figure 3. Simulated standing-wave optical field intensity along the optical axis of the HC-VCSEL (red) and the real refractive index profile (black).

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Table 1. Cavity parameters at a resonance wavelength of 845 nm.

Optical confinement factor	0.0173
Cold cavity Q	16200
Total loss (ps^{-1})	0.138
Top DBR transmission loss (ps^{-1})	0.053
Bottom DBR transmission loss (ps^{-1})	0.00003
Intra-cavity loss (ps^{-1})	0.085
Threshold gain (cm^{-1})	609
Photon lifetime (ps)	7.25

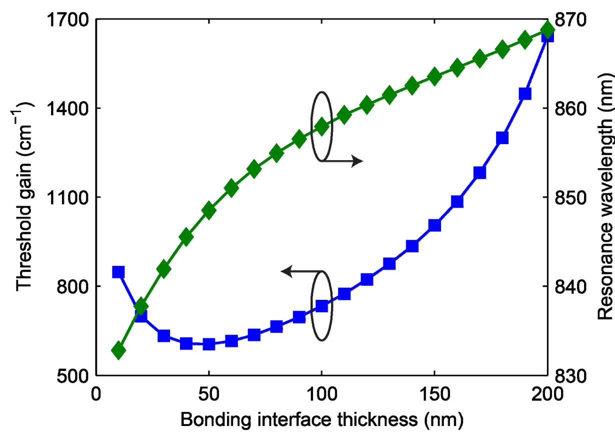

Figure 4. Simulated dependence of resonance wavelength and threshold gain on bonding interface thickness.

3. FABRICATION

Fabrication starts with the deposition of the dielectric SiO_2/Ta_2O_5 DBR on a Si wafer and growth of the epitaxial III-V structure on a GaAs substrate. The comparison of simulated and measured reflectance for the dielectric DBR in Fig.5 shows good agreement in terms of the width of the stopband and a slight blue-shift of the measured center wavelength (20 nm) with respect to simulations.

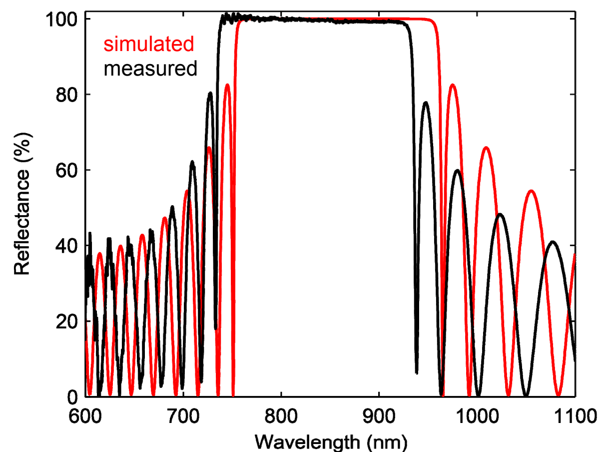

Figure 5. Simulated (red) and measured (black) spectral reflectance of the 20-pair SiO_2/Ta_2O_5 dielectric DBR.

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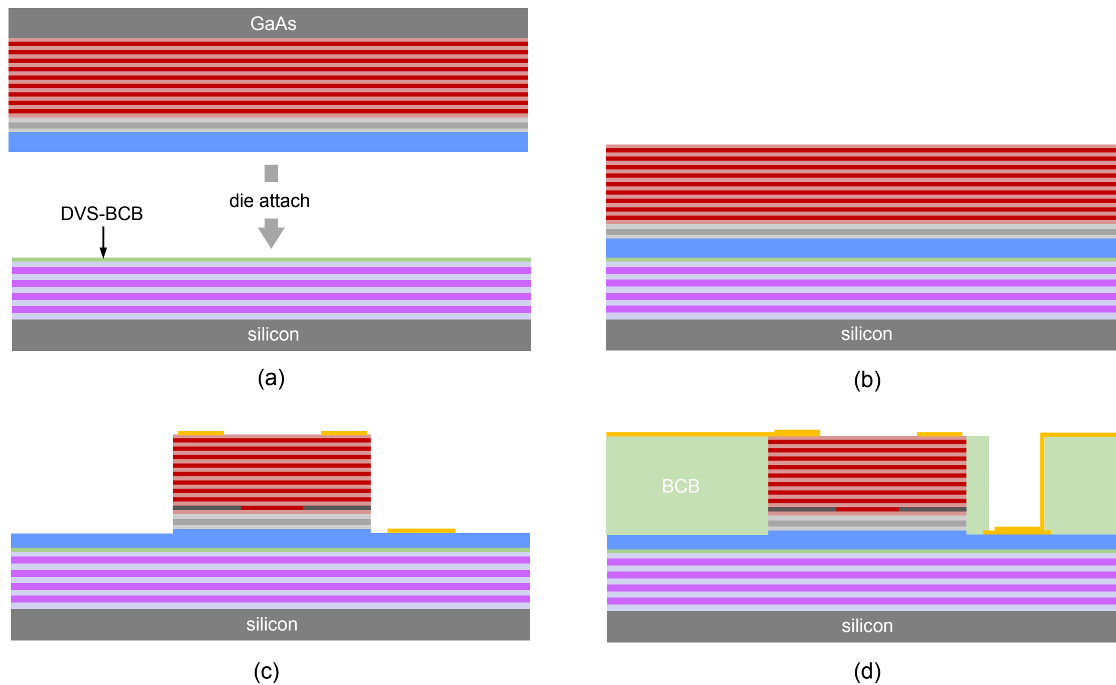

Figure 6. Fabrication process flow for the hybrid-cavity VCSEL. (a) bonding of GaAs die with epitaxial structure to the dielectric DBR on Si, spin-coated with DVS-BCB, (b) removal of GaAs substrate, (c) top *p*-contact metallization, mesa etching, selective oxidation, and intra-cavity *n*-contact metallization, (d) planarization with BCB and pad metal deposition.

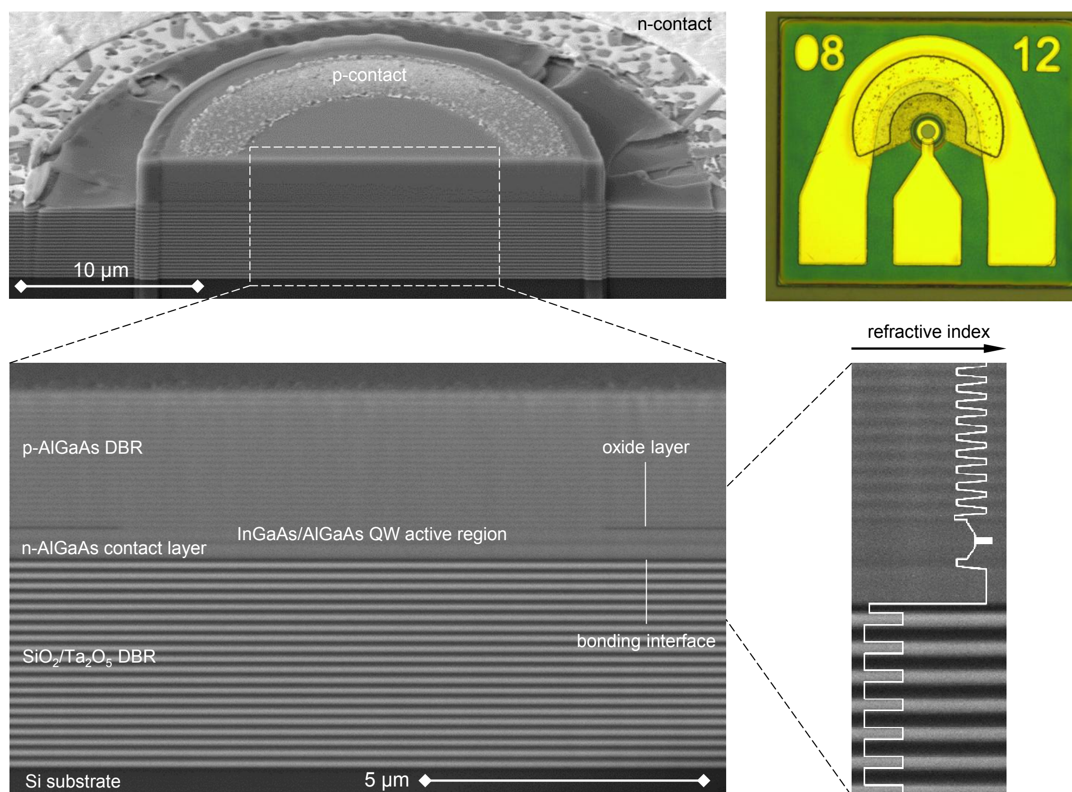

Figure 7. SEM images of a focused ion beam cross-section and microscope top image (upper right) of a fabricated HC-VCSEL.

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The process flow for HC-VCSEL fabrication is illustrated in Fig.6. It starts with deposition of the thin SiO_2 layer on the dielectric DBR, followed by spin-coating and partial curing of the DVS-BCB bonding layer. The III-V die is then bonded to the dielectric DBR and fully cured using the process described in [6]. The bonding process results in a DVS-BCB thickness of ~40 nm. This is followed by removal of the GaAs substrate. Finally, oxide-confined HC-VCSELs are fabricated using processes commonly used for the fabrication of oxide-confined VCSELs. This involves *p*-contact metallization, mesa etching, selective oxidation, and *n*-contact metallization. The structure was also planarized with BCB before pad metallization.

Fig.7 shows SEM images under different magnification of a focused ion beam cross-section for a fabricated HC-VCSEL, as well as a microscope top image. In the SEM images, the bonding interface, the DBRs, and the oxide aperture used for transverse current and optical confinement are clearly visible. Four different bonding interface (DVS-BCB + SiO_2) thicknesses (35, 65, 125, and 180 nm) were used. For each, HC-VCSELs with an oxide aperture diameter varying from 3 to 10 μm were fabricated.

4. PERFORMANCE EVALUATION AND DEPENDENCE ON BONDING INTERFACE THICKNESS

For the HC-VCSELs with four different bonding interface thicknesses (device A-D), the corresponding cavity resonance wavelengths and differences between the gain peak wavelength and cavity resonance wavelength (gain-resonance offset) at 25°C are listed in Table 2. The gain peak wavelength was estimated from photoluminescence measurements performed on the QWs used in the epitaxial structure. The offset changes with temperature since the gain spectrum red-shifts ~4 times faster than the resonance wavelength [11]. It is therefore an important parameter that controls the optical gain properties as well as the temperature dependence of several important performance parameters.

Table 2. Bonding interface thicknesses and corresponding cavity resonance wavelengths and gain-resonance offsets at 25°C.

	Device A	Device B	Device C	Device D
Bonding interface thickness (nm)	35	65	125	180
Cavity resonance wavelength (nm)	843	853	861	867
Gain-resonance offset (nm)	+9	-1	-9	-15

Fig.8 shows the measured output power and voltage as a function of current for devices A-D with an oxide aperture diameter of 10 μm in the temperature range 15-100°C. The measured dependence of threshold current on temperature and emission spectra at 25°C/2 mA are shown in Fig.9. At 25°C, the dependence of threshold current on the bonding interface thickness follows the variation of threshold gain predicted by simulations (Fig.4), with minimum threshold current for device B which has the smallest gain-resonance offset at this temperature. At high temperature, C and D have lower threshold current since for these devices the cavity resonance and gain peak align at higher temperatures.

The achievable output power is largely determined by the slope efficiency and the thermal roll-over current. With a relatively high slope efficiency (~0.5 W/A at 25°C, and decreasing at high temperatures due to increased internal loss

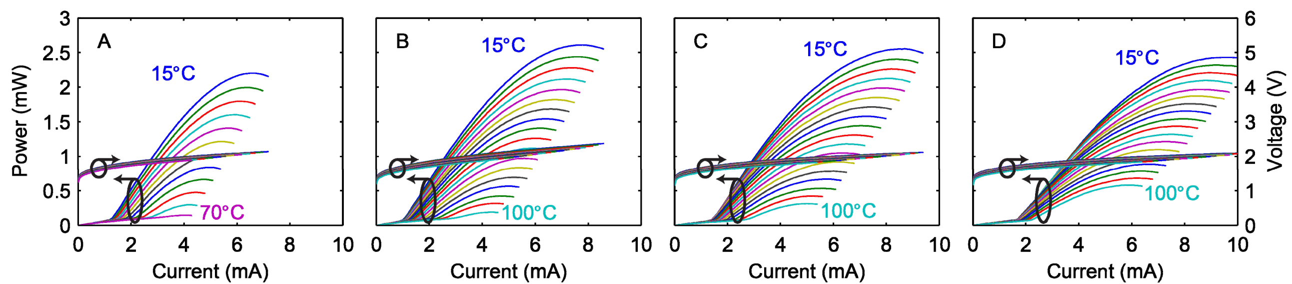

Figure 8. Output power and voltage vs. current from 15 to 100°C (5°C steps) for devices A-D, all with a 10 μm oxide aperture diameter.

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and reduced internal quantum efficiency), output power is to a large extent limited by the relatively low roll-over current. This is due to the high thermal impedance caused by the low thermal conductivity of the dielectric DBR. The measured thermal impedance is 7 K/mW, which is ~4 times higher than for a conventional GaAs-based oxide-confined VCSEL [12]. This results in a maximum power of 2.3 mW at 25°C from devices B and C, and 0.6 mW at 100°C from device D. For most devices, the differential resistance is 50-60 Ω and largely independent of temperature. This indicates that the *n*-AlGaAs layer provides a low resistance path for intra-cavity current injection.

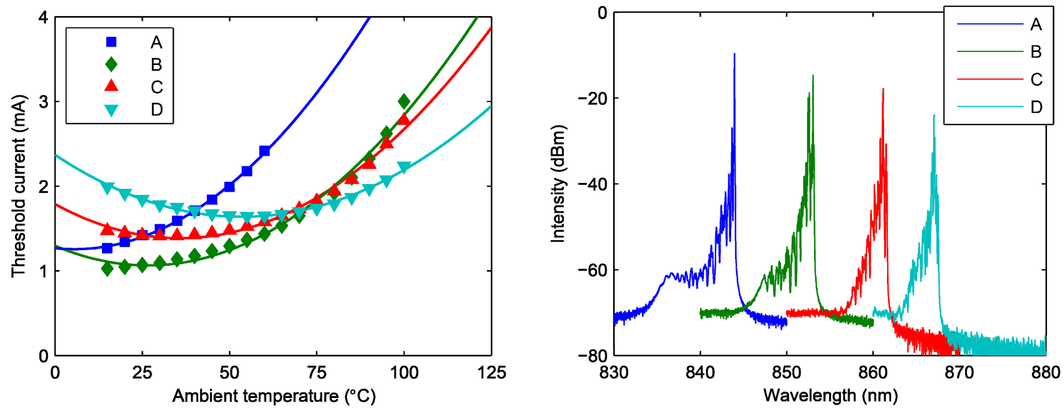

Figure 9. Threshold current vs. temperature (left) and emission spectrum at 25°C and 2 mA current for devices A-D.

The small-signal modulation response, along with fits to a three-pole transfer function for extracting the resonance frequency, damping rate, and parasitic pole frequency and their dependencies on current [13], is shown in Fig.10. All devices show a strongly resonant response even at the highest current due to the limited photon density achieved at thermal roll-over, which limits the resonance frequency and therefore the damping. This, together with the relatively large capacitance associated with the single oxide-aperture limits the modulation bandwidth to ~10 GHz at 25°C and ~6 GHz at 85°C. The impact of bonding interface thickness (gain-resonance offset) on HC-VCSEL dynamics is reflected in the strength of the damping of the modulation response at thermal roll-over (where the highest photon density is established) and by the rate at which the resonance frequency increases with current (which is quantified by the *D*-factor). Therefore, devices B-D have the most damped response at the highest current while also having a lower *D*-factor than device A (from 4.8 to 3.0 GHz/mA$^{1/2}$ for device A-D at 25°C). This is because of the differential gain being lower on the long-wavelength side of the gain peak.

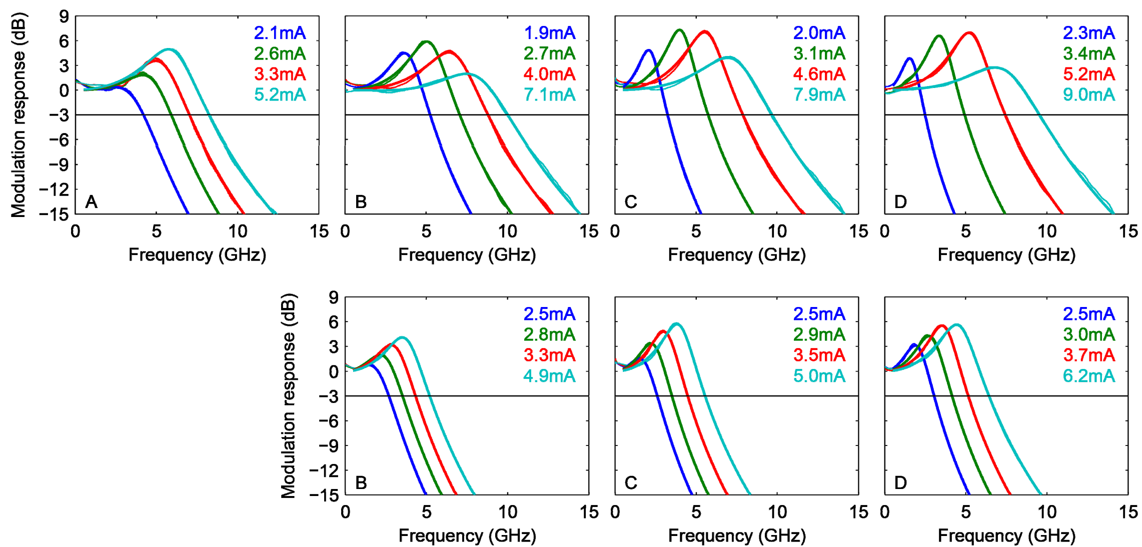

Figure 10. Small signal modulation response for devices A-D at 25°C (upper) and C-D at 85°C (lower).

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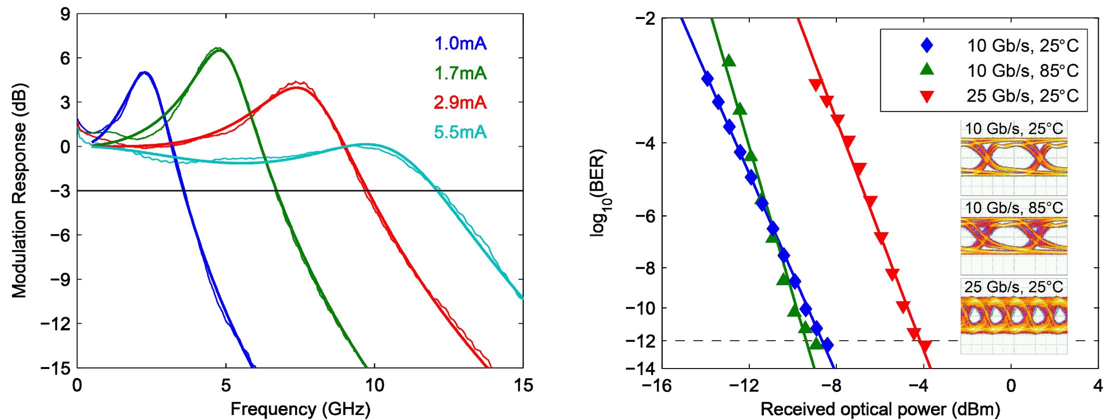

Figure 11. Small signal modulation response at 25°C for a HC-VCSEL with a 5 µm oxide aperture diameter and an emission wavelength of 859 nm (similar to device C). BER vs. received optical power for the same device at bit-rates up to 25 Gbit/s at 25°C and 10 Gbit/s at 85°C. Insets show received optical eyes.

For large-signal modulation and data transmission experiments we chose a HC-VCSEL with a smaller aperture diameter of 5 µm and a resonance wavelength of 859 nm. This device has a threshold current of 0.5 mA and a more damped response due to the higher photon density. Fig.11 shows the small-signal modulation response, with a maximum modulation bandwidth of 12 GHz at 25°C (9 GHz at 85°C), and results from transmission experiments. Maximum data rates of 25 and 10 Gbit/s were reached at 25 and 85°C, respectively.

5. SUMMARY AND DISCUSSION

We have established a heterogeneous integration technique for short-wavelength HC-VCSELs on Si where an epitaxial GaAs-based half-VCSEL structure is attached to a dielectric DBR on Si by adhesive bonding. HC-VCSELs at 850 nm with sub-mA threshold current, >2 mW output power, and 25 Gbit/s modulation speed were demonstrated. We have also shown that the thickness of the bonding interface can be used to optimize a certain performance parameter (e.g. threshold current, output power, or modulation speed) at a given temperature or to minimize the variation of performance over temperature. The performance of the HC-VCSELs in terms of output power and speed is limited by the high thermal impedance caused by the high thermal resistance of the dielectric DBR. Integrated metallic heat spreaders [14] or thermal shunts [15] may reduce the thermal impedance.

With an intra-cavity waveguide with a diffraction grating, light can be tapped of to the in-plane waveguide. Together with a high reflectance top DBR this may enable a low current, high-efficiency and small footprint HVCL for silicon photonics integration. Short-wavelength light sources on a silicon-nitride waveguide platform on Si will enable fully integrated silicon photonic circuits for applications in life science, bio-photonics, and short-reach optical interconnects.

6. ACKNOWLEDGEMENT

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