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PLAT4M: Progressing Silicon Photonics in Europe

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Abstract: Photonic integration is an appealing technology for emerging applications in communications, medical diagnostics and sensing. Silicon Photonics presents a highly attractive solution for large-scale photonic integration, principally because it is based on well-established CMOS-fabrication technologies. However, Silicon photonics can be difficult and expensive to implement, as it requires complex device design, fabrication and packaging capabilities. Photonic Libraries And Technology for Manufacturing (PLAT4M) is a major European project that brings together the key capabilities required to develop solutions for a range of Silicon photonic-based applications. This paper will present an overview of the PLAT4M project. It will present, in detail, a key application demonstrator (Coherent Beam Combiner), highlighting the ability of the project team to develop an integrated Silicon Photonic sub-system, from design, through to device fabrication, packaging and final test. The paper also highlights the need to consider additional capabilities besides device fabrication, such as packaging, which are critical to achieving fully operational sub-systems.

Keywords: PLATM; Si photonics; coherent beam combining; Si PIC; SOI; photonic packaging; waveguide coupling

1. Introduction

The PLAT4M (*Photonic Libraries And Technology for Manufacturing*) project focuses on bringing the existing silicon photonics research platform to a level that enables transition to industry, suitable for different application fields and levels of production volume. The PLAT4M consortium includes 15 European R&D institutes and CMOS companies, key industrial and research organizations in design and packaging, as well as end users in different application fields to build the complete supply chain. Silicon has been employed for many years in CMOS integrated circuits for mass-production applications and there is the same expectation for silicon photonic technologies. Upgrading existing photonic platforms to become compatible with industrialization is mandatory at this point. It requires the establishment of design and process flows by taking into account design robustness, process variability and integration constraints. The PLAT4M partners bring a critical combination of expertise to the challenge of building a complete supply chain for commercializing silicon photonics in Europe.

The PLAT4M consortium is developing mature technologies and tools by building a coherent design flow, demonstrating manufacturability of elementary devices and process integration and developing a packaging toolkit. The project is validating the complete supply chain through application-driven test vehicles representing various application fields, such as telecom and datacom, gas sensing, LiDAR, Laser Doppler Vibrometry (LDV) and coherent beam combining. PLAT4M also focuses on preparing the next-generation platform by establishing a roadmap for performance evolution and assessing scalability to high-volume production. The supply chain is based on technology platforms of LETI (France), IMEC (Belgium) and STMicroelectronics (France and Italy), all of which is supported by a unified design environment.

In the following we present, in detail, the workflow of the silicon photonic chip for the coherent beam combining application which is a key application driver in the PLAT4M project. We present each critical stage of the development chain: motivation for the application, photonic chip design and fabrication, photonic packaging, test and characterisation.

Coherent beam combining (CBC) of fibre lasers provides an attractive mean of reaching high output laser power by scaling up the available energy while keeping fibre intrinsic advantages of compactness, reliability, efficiency, and beam quality. In CBC architectures, the power of a master oscillator (MO) is divided into N fibres that are amplified individually. The N amplified output beams are then combined coherently in order to produce ideally an optical beam with a brightness increased by N with respect to the individual beams. Moreover, this laser architecture provides a synthetic aperture with phase front control ability which permits output beam steering and atmospheric phase perturbation compensation.

The coherent addition means that the optical phases of all the channels are locked, either in a passive way [1,2] or, using active phase lock loops (PLLs) [3–5]. This last approach, we chose for this work, is commonly preferred when a large number of fibres are considered (typically above 10 to 20). Then, as many PLLs as the number of fibres have to be implemented, which underlines the need for collective technologies and methods. First prerequisite for a PLL is to measure the phase perturbation between the propagation channels. This can be done using various techniques [3–5], among which we chose an interferometric approach, which has the advantages of being collective and scalable to potentially very high number of fibres (up to hundreds) [5].

An important part of the system is the fibre channel preparation, *i.e.*, the splitting of the incident master oscillator into N channels, and the addition of one phase modulator per channel, required to feed back the system and close the PLLs. For this particular purpose, Silicon Photonics technology can bring unique advantages for these splitting and phase modulation functionalities. When a potentially very large number of channels is envisaged, volume and cost considerations become critical, and an integrated solution, carrying these functionalities on a single or few chips, is mandatory for an economically viable system. Our demonstrator aims at validating the integration of Silicon photonic functions for channel splitting and phase modulators arrays in a passive CBC experiment.

2. Si Photonic IC

2.1. Design

For real system applications with Coherent Beam Combining, high optical power levels are required at the output channels of the silicon Photonic Integrated Circuit (PIC). Therefore, it is important that the total insertion loss of the PIC is as low as possible. The first aim is to increase the overall power efficiency, but it is equally important to limit the amount of total optical power required at the input of the chip. It is well known that, in silicon, the optical power that can be efficiently guided in a submicron wire waveguide is limited by two-photon absorption and subsequently free carrier absorption. At 50 mW one has to account for 3 dB/cm additional loss due to these non-linear processes. Such a power level is easily reached at the input in front of the splitter when several milliwatts of power are required at the output channels. Another crucial part in the CBC design is the

phase shifter. To ensure coherent beam combining the phase shifters should be able to induce a 2π phase shift. Additionally, in order to keep the Strehl ratio degradation of the combined beam below 10%, the phase resolution should be at least $\pi/10$ and any possible spurious amplitude modulation associated with the phase modulation process should be below 1 dB [6]. Next, we will describe the design that can meet all the aforementioned requirements.

To couple light from the PM fibres in and out the silicon PIC, high efficiency grating couplers [7] are used. Higher efficiency is obtained in these grating couplers by adding and patterning a poly-silicon overlay on top of the standard crystalline silicon layer. By doing so, the directionality of the grating coupler can be enhanced, resulting in higher efficiency. The input grating coupler is followed by a 1×16 splitter. The optical waveguide that interconnects the grating coupler with the splitter is kept as short as possible to avoid excessive losses due to non-linear (NL) processes. The splitter itself is implemented as a 4-stage tree of 1×2 MMIs. MMIs are known to be very robust against process variations, having low insertion loss and high channel uniformity. A disadvantage of the tree architecture is the high power in the first branch of the tree, which is the sum of the power in all the output channels, typically 20/30 dBm. However, for a full system demonstration as shown here, this approach was selected as being the most reliable. The output channels of the splitter are connected to the phase modulators. Because carrier based silicon phase modulators inherently induce strong spurious amplitude modulation, this type of modulator cannot be used. Fortunately, because the required speed for this application is only in the kHz range, thermo-optic phase shifters offer a good alternative, as they have low insertion loss and low spurious amplitude modulation.

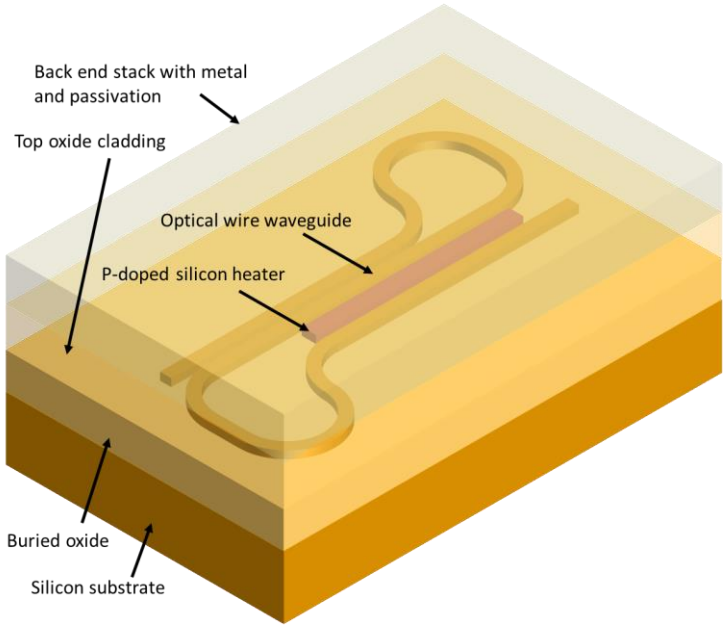

Figure 1. Schematic representation of the thermo-optic phase shifter implementation, where the optical waveguide is wrapped around a doped silicon line.

The thermo-optic phase shifters are implemented as p-doped silicon lines in the same layer as the optical waveguides. The fact that these heaters are in-plane with the optical waveguides offers an advantage over also often used metal heaters that are positioned above the optical waveguide. The reason is that in the case of in-plane heaters the optical waveguide can be wrapped around the heater, which gives an efficiency improvement of at least a factor of 2 without compromising for speed [8]. Figure 1 shows a schematic representation of the phase shifter that has been implemented in the CBC design. The optical waveguide passes by the heater as close as possible and is then routed back to pass by the other side of the heater after which it is again routed towards the direction of

the output waveguide. The heater width and spacing with respect to the optical waveguide are determined from optical and thermal simulations. From a thermal point of view, it is desirable to put the heater as close as possible to the waveguide to enhance the efficiency. However, a directional coupler is formed by the optical waveguide and the silicon line heater, which limits the minimum spacing because of possible undesired coupling. To minimize the coupling, the width of the heater can be modified to avoid phase matching between the optical modes that can exist in the optical waveguide and the silicon heater line. According to our simulations a heater width of 1.2 μm is a good choice and this allows placing the heater at a distance of 600 nm from the optical waveguide without causing significant undesired coupling when the heater has a length of 200 μm.

The outputs of the thermo-optic phase shifters are connected to the high efficiency grating couplers which are arranged in an array with 127 μm pitch for interfacing with a fibre array. In order to comply with packaging requirements, shunt waveguides with grating couplers have been added around the input- and output grating couplers to enable an active alignment approach. Furthermore, optical in- and outputs are placed at the left and right side of the chip, while all electrical bondpads for electrical contacting were routed to the top of the chip for wire bonding. Because of the size of fibre array heads, the distance between the grating couplers and electrical bondpads should be large enough such that the fibre array heads do not block the electrical bondpads. Note that the size of the design is mainly determined by these packaging constraints. It is therefore important to already be aware of these constraints in the design phase of the chip, as in worst case a whole new design cycle can be required which is a significant cost.

As handling high optical powers is crucial for practical CBC systems, a new integrated grating coupler splitter has been developed in parallel with the full demonstrator [9]. This integrated grating coupler splitter consists of a star coupler that has a curved grating in its slab region. The incoming light from the fibre is then "defocused" by this curved grating into the slab of the star coupler. As the light is now never confined in a single mode waveguide, optical intensities are lower and as a result non-linear effects can be avoided. This device is capable of handling input powers up to 1 W and will be implemented in the next generation designs.

2.2. Fabrication

The devices were fabricated in IMEC's silicon photonics full platform (ISIPP25G) [10] on 200 mm SOI wafers with 220 nm silicon on a 2 μm buried oxide. First, the passive waveguide layer is processed using three etch steps: a complete 220 nm etch, a partial 70 nm etch and a partial 160 nm etch. In our design we used the deep etch for the waveguides and the doped silicon heaters while the 70 nm etch was used to lower the refractive index contrast in the lateral direction in the MMI and to define the first part of the high efficiency grating couplers. These structures are then oxide-clad and planarized, and on top of 70 nm partial etch for the grating couplers an additional 160 nm of poly-silicon is deposited. This layer is then patterned to define the high-efficiency gratings. Next, the dopants for the heaters are implanted and activated. Local silicidation is applied for contacting and after oxide cladding deposition contact holes are etched and filled with Tungsten. Finally, a standard Cu-damascene back-end and passivation is added. A microscope image of the fabricated demonstrator circuit is shown in Figure 2.

3. Photonic Packaging

The photonic chip is housed onto a custom test board that allows us to connect the 16 heaters to a DC connector. A 10 kΩ thermistor is placed in good thermal contact with the IC. The printed circuit board (PCB) presents thermal vias on the PIC footprint, and a thermoelectric cooler is mounted underneath the PCB for temperature control of the device. The test-unit is assembled on top of an optical breadboard that acts also as heat-sink for the thermoelectric cooler (TEC).

The cross-section of single mode Si photonics waveguides @ 1550 nm is 220 nm × 450 nm. Diffracting grating couplers [7] are used for optical coupling between waveguides and single-mode

fibres. For Coherent Beam Combining, it is necessary to use polarization maintaining (PM) fibres to connect to the Silicon waveguides. The 1D grating couplers implemented on this demonstrator support only transverse-electric (TE) polarization of light. The fibre stress rod orientation shown in Figure 3a allows only the TE mode to reach the grating couplers. Active alignment is required for optical coupling between single-mode fibres and PIC [11]. We use two extra grating couplers or "optical shunts" in addition to those on the input signal channels, Figure 3b. These shunts are necessary for accurate fibre alignment and they avoid the need to use the signal channels during the alignment process. The active alignment process involves maximizing the signal coupled into the shunt waveguide when the fibre array is scanning in a near contact position to the Si-PIC surface.

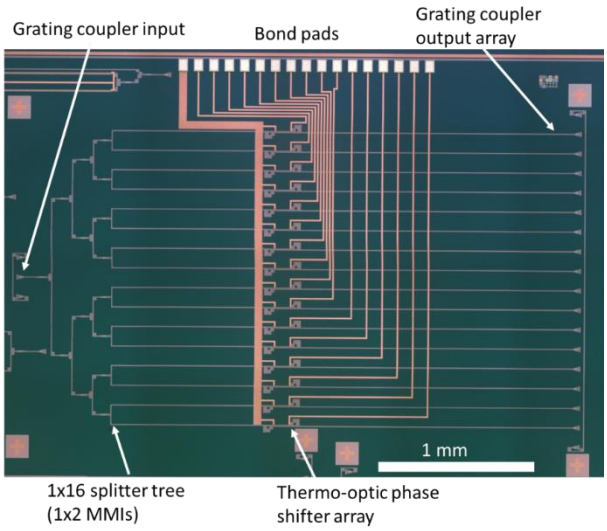

Figure 2. Microscope image of the demonstrator circuit after finalizing the silicon Photonic Integrated Circuit (PIC) fabrication process.

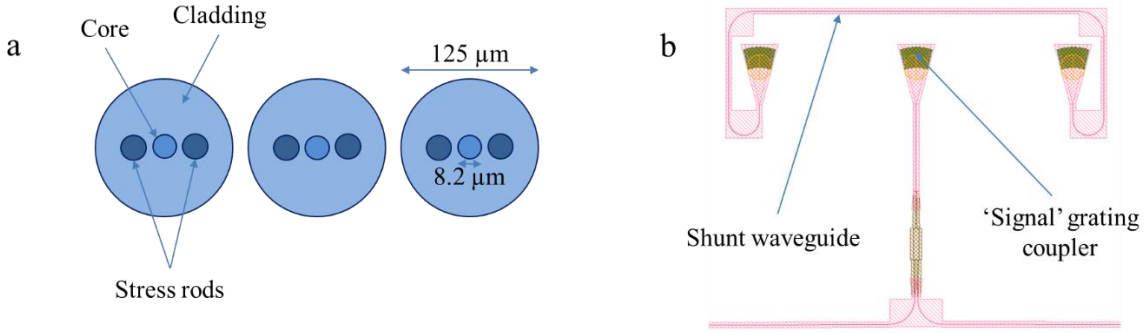

Figure 3. (**a**) Polarization maintaining fibre array with stress rods oriented to deliver transverse-electric (TE) mode on the grating couplers; (**b**) Shunt waveguide connecting two dummy grating couplers for active fibre coupling process.

Grating couplers designed for this application require light incident at 10° off-vertical and the channel pitch is 127 µm, corresponding to standard fibre arrays. When the fibre array is positioned on the maximum coupling efficiency point through the shunt waveguide, a thin layer of low-shrinkage UV cure epoxy is used to bond the fibre block onto the PIC surface, see Figure 4a. The epoxy refractive index (n) is approximately 1.5, which is close to the refractive indices of the fibre and the SiO_2 cover layer on top of the grating coupler. Figure 4b shows the 3D model of the fibre connection to the PIC. Two different fibre arrays have been used for the input and the 16 outputs. On both sides, two grating couplers shorted by a waveguide enable the active alignment of the fibres.

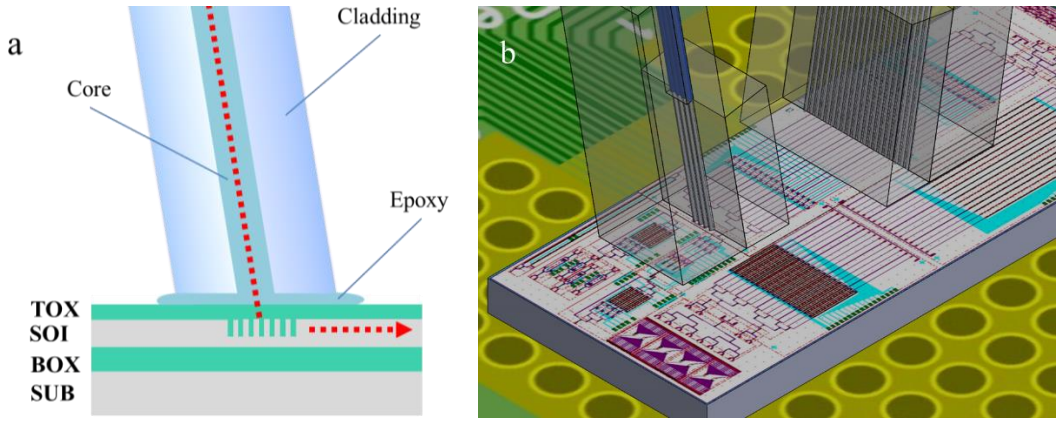

Figure 4. (**a**) Fibre connection to the grating coupler. The fibre block is polished at 10° and a thin layer of "optical" epoxy is used to bond the fibre onto the photonic chip; (**b**) 3D model of the fibre connection to the PIC. The PIC presents one input and 16 outputs. On both input and output side two additional grating couplers have been added to support the active fibre alignment.

Figure 5 shows a completed prototype, note the two posts supporting the bulky fibre bundle to avoid unnecessary stress on the joint between fibre array and PIC. It should be noted that it is possible to use a planar fibre array for a more compact overall assembly [11]. However, this initial CBC prototype used the vertical fibre design. As mentioned previously, this prototype includes 16 channels, which is still far from the hundreds or more potentially required for extremely high power CBC sources. The main challenge for scaling up this channel count is on the packaging side. With the current fibre coupling approach, the chip area increases linearly with the number of channels, with huge impact on the cost. However, 2D fibre arrays should be a valuable implementation in the future, to scale up to tens of channels on a chip with moderate dimensions.

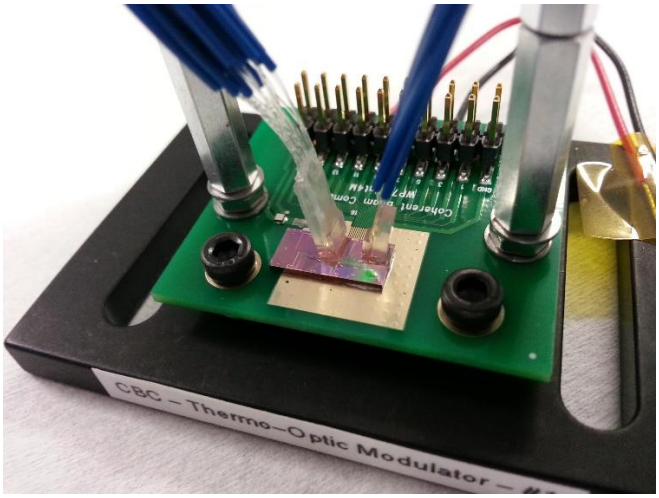

Figure 5. Photo of the coherent beam combining (CBC) prototype. The Si-PIC is housed onto a custom printed circuit board (PCB) and two fibre arrays are aligned and attached on top of the Photonic Integrated Circuit (PIC) using ultraviolet cure epoxy.

Although the chip fabrication process is ready for large scale production, the packaging process is based on active alignment and not yet suitable for high volume manufacturing. This lack on the packaging side will be soon addressed by industry using vision based optical coupling techniques.

Figure 6a shows the wavelength response across the shunt waveguide for the four demonstrators prepared. It is peaking at 1535 nm. At 1550 nm, the CBC operation wavelength, the insertion loss

for each grating coupler is 4 dB with less than 1 dB fluctuation, see Figure 6b. It represents also the insertion loss of the device in each channel (excluding the 1:16 splitter block). The grating couplers are designed to peak at 1550 nm with a "fibre-air-chip" interface when flat-end fibres at 10° off-vertical are used for optical coupling. This interface is not present in the packaged device because index matching epoxy is used to bond the fibres onto the chip. As a result there is not refraction at the silicon oxide interface and the beam shines the grating coupler with a different angle resulting in a shift of the peak wavelength.

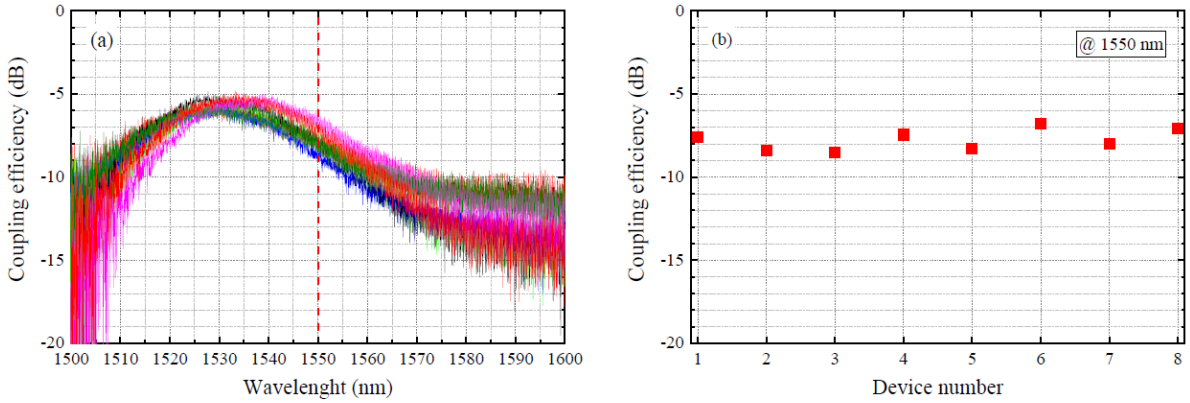

Figure 6. (**a**) Grating coupler wavelength response on the eight measured samples. The coupling efficiency peaks at 1535 nm and is still acceptable at 1550 nm; (**b**) Coupling efficiency at 1550 nm of the eight tested structures. The insertion loss on each grating coupler is of about 4 dB and the uniformity is better than 1 dB.

We also investigated the alignment tolerance of our grating couplers using standard single-mode fibres (SMF-28), see Figure 7. The coupling efficiency through the shunt waveguide was recorded while the fibre array was swept over the grating coupler with a 200 nm step. The alignment tolerances results are relatively relaxed: about 1 dB of additional losses over a planar misalignment of $\pm$ 2.5 µm, which is in good agreement with values reported in literature [12]. Figure 7a shows the 2D map of the grating coupler alignment tolerances over an area 15 µm $\times$ 15 µm. Figure 7b shows the grating coupler efficiency recorded moving the fibre along two orthogonal axes on the grating plane.

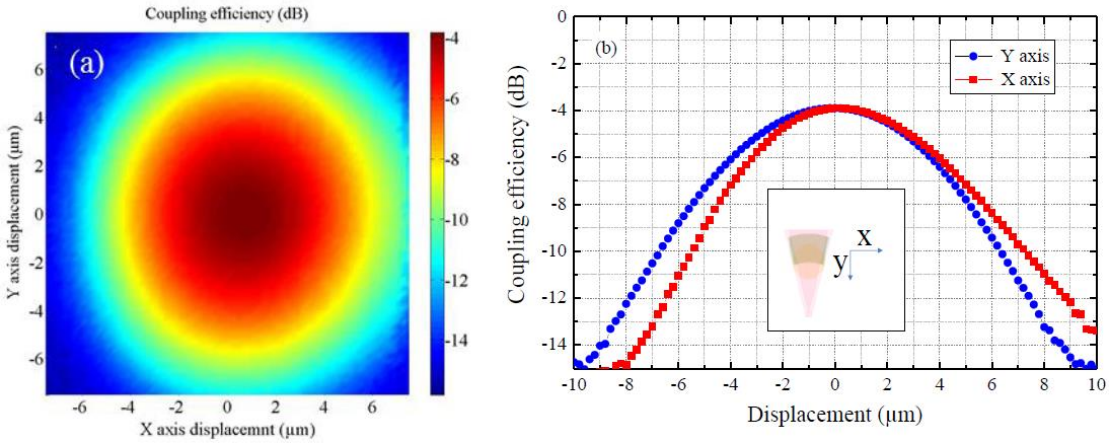

Figure 7. (**a**) Grating coupler alignment tolerance measurement; (**b**) X and Y scan of the fibre on the grating coupler plane showing about 1 dB of extra insertion losses with a fibre displacement of $\pm$ 2.5 µm.

4. Experimental Setup

As described in Figure 8, the principle of this measurement is to retrieve the optical phase distribution from the spatial position of the fringe sets resulting from the interference of each individual beam with a common reference plane wave. This collective phase measurement is operated at 1 kHz refresh rate, which gives the PLL loop frequency.

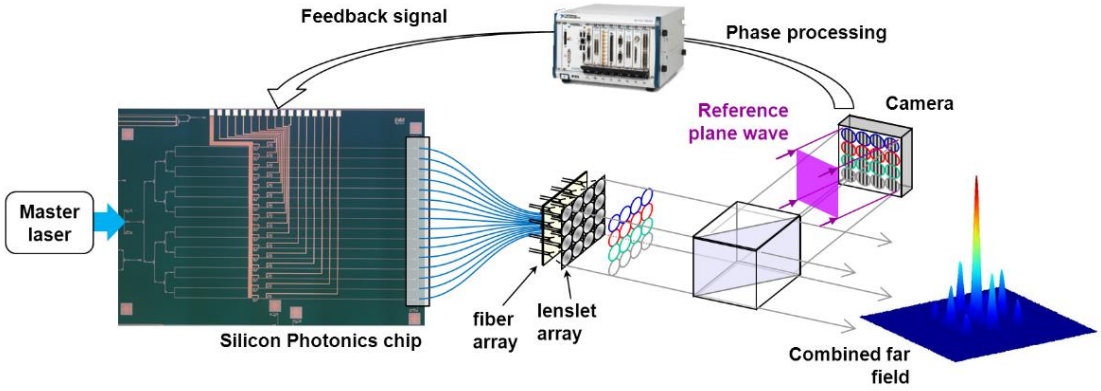

Figure 8. Schematic of the CBC experimental setup with active phase locking.

In our CBC system, a 1.55 μm CW master oscillator directly feeds the Silicon chip through a PM fibre glued onto the input grating coupler. The power of the master oscillator is split on chip into 16 channels, each of which includes a thermal phase modulator. The outputs of the 16 waveguides are collectively out-coupled from the chip using a PM optical fibre array aligned and glued onto the PIC's output grating couplers array. At the other end of fibre array, the 16 fibre outputs are arranged in a 4 by 4 squared lattice, and collimated by a microlens array to form 16 collimated and parallel beamlets. Details on the fibre array laser head can be found in [13]. The laser intensity at each of the 16 fibres output is first measured and normalized to the energy delivered by the master laser.

5. Results and Discussion

The fibre-to-fibre transmission measurement is shown in Figure 9a. The overall insertion loss homogeneity is about 1 dB, and the insertion loss of the device is 7 dB per channel, excluding the 1:16 ratio of the splitter tree. The phase responses of the PIC's modulators are collectively measured using our CBC interferometric set up, by applying square shaped voltage waveforms at 1 kHz frequency to the modulators. Therefore, we make sure that the thermal modulator technology is suitable with our chosen 1 kHz loop frequency for the PLLs. As shown in Figure 9b, the phase responses of all the 16 channels are very homogeneous, with a slope efficiency of 0.285 rad/mW. Therefore, a 2π phase shift is achieved for 22 mW of electrical driving power.

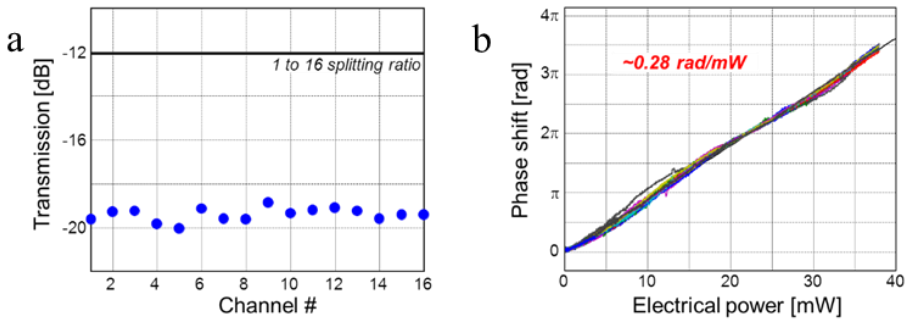

Figure 9. (**a**) Fibre-to-fibre transmission of the 16 channels; (**b**) Phase modulation response for the 16 channels (superposed colored lines).

Finally, the successful coherent combination is evidenced by recording the far field of the 16 parallel and collimated output beams. As shown in Figure 10, when the PLLs are off, the far field pattern is a fluctuating speckle-like profile resulting from the interference of the 16 beams with random phase distribution. When the PLLs are on, the phases of all the 16 channels are locked together and form an overall plane phase front for the composite output pupil of the system. This result in the far field pattern is shown in Figure 10 (right), with a bright and stable central lobe. The intensity lost here in the satellite lobes is just a result of the filling factor of the individual beams in the collimating microlenses plane. The temporal stability of the system is also illustrated in the plot below, with the energy encircled in the main central lobe plotted against time. The measured channel-to-channel residual phase error in closed loop configuration is below $\lambda/120$.

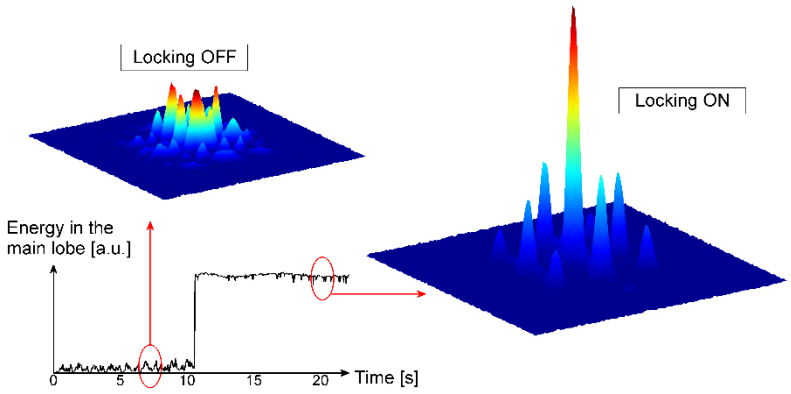

Figure 10. Experimental far field pattern of the 16 combined beams, when PLLs are off (**upper left**), and when PLLs are on (**right**). The plot shows the temporal evolution of the energy encircled in the main central lobe of the combined beam.

The optical power incident on the chip here was 10 dBm, meaning approximately −9 dBm at each fibre output. This is still too low for a real system application where fibre amplifiers have to operate in saturation regime. The next generation of devices will be able to handle one to two orders of magnitude higher input power.

6. Conclusions

The growing interest in Silicon photonics is mainly driven by its ability to satisfy demands in large markets, particularly for datacoms, medical diagnostics and sensing applications. Device fabrication based on CMOS wafer-scale processes can meet this demand. However, device fabrication is only one element of the supply chain necessary to produce fully working sub-systems. In this paper, we have shown how the PLAT4M project is addressing this technological supply chain challenge, by bringing together a range of capabilities from around Europe, from Si-PIC design, through to device fabrication, packaging and final test. We reported the demonstration of this full supply chain through one of the applications developed in PLAT4M, a Si-PIC Coherent Beam Combiner. It is however worthwhile mentioning that the PLAT4M supply chain is also used in the project for the development of other applications, namely laser Doppler vibrometry, gas sensing and a Datacom transceiver compatible with the 100GBase-LR4 standard. A key feature of this collaboration is the need for each partner to understand and to account for other elements in the supply chain. For example, device designers need to account for packaging when preparing chip layout, ensuring factors such as grating coupler pitch and shunt waveguides are included to ease the fibre alignment process. The PLAT4M project highlights the need for a consortium-driven approach to integrated photonics, where all elements of the technology supply chain work together to achieve a single objective.

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Conflicts of Interest: The authors declare no conflict of interest.

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