On-chip Transmitter and Receiver Front-ends for Ultra-Broadband Wired and Optical-fiber Communications

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Abstract: Increasing line rates beyond 56Gb/s is a big challenge for transceiver front-ends. We discuss recent developments towards 100Gb/s copper, +56Gb/s multi-channel single-mode VCSEL links and segmented MZM drivers for advanced modulation.
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1. Introduction

High-speed interface speeds need to scale up to follow the increasing demand of data intensive applications such as cloud services, high-performance computing, video traffic, storage, 5G etc. Datacenters have become the hot spots of the internet where various interconnect challenges reside from chip-to-chip, chip-to-module, board-to-board, rack-to-rack, etc. There is no single best solution among electrical and optical technologies due to the different technological constraint in terms of distance, footprint, power consumption, cost etc. Research is approaching this need for capacity from different angles, with technological improvements on photonic and electronic devices and/or by applying more complex modulation and signal processing. In this paper, we highlight a number of our recent developments on the most critical building blocks of very high speed transceivers targeting various applications at 56Gb/s and higher.

2. 100Gb/s interconnects

Without doubt, electrical signaling is the most straightforward way of communication between electronic devices. The capacity of copper interconnects is often underestimated. Alternative printed circuit board (PCB) and connector technologies are being developed such as cable backplanes or direct-mate orthogonal connectors, constantly extending the reach over copper. For sure, copper interconnections on PCB and copper cables suffer from conductor and dielectric losses, which increase dramatically with frequency. However, depending on the distance and desired bit rate, the low-pass filtering introduced by the copper channel can be effectively compensated by equalizer circuits [1]. As such, copper will remain more cost effective for short links as long as sufficient signal-to-noise ratio (SNR) is available. Currently distances on the order of 50cm for Megtron 6 backplanes at 56Gb/s and on the order of 1-3m for twinax cables up to 100Gb/s are feasible [2]. Moreover, partial response modulation schemes, such as duobinary, can actually partly use the channel's low pass characteristic. In such scheme the channel loss is used to shape the signal with well known intersymbol interference to increase the bandwidth efficiency.

Fig. 1 (a) shows the basic architecture and working principle of our duobinary transmitter (Tx) and receiver (Rx) chip set. The Tx consists of a 4:1 multiplexer (MUX) connected to a 6-tap feed-forward equalizer (FFE) with an approximate delay of 10ps between the taps. Together with the channel, the FFE creates an equivalent channel that transforms the NRZ output of the MUX into a duobinary signal at the Rx input. The Rx chip includes a duobinary front-end connected to a 1:4 demultiplexer (DEMUX). 100Gbit/s operation is shown in Fig. 1 (b) and (c) with good horizontal and vertical eye openings, and a BER below 10^{-12} was shown for a 25 cm differential link between the test boards (20cm coax + 5cm RO4350 PCB). The BER performance and the maximum achievable loss budget will now be evaluated for 100Gb/s backplane and cable interconnects. This is the fastest reported electrical duobinary transmission experiment to date. The Tx and Rx chips are fabricated in 130 nm SiGe BiCMOS technology and mounted directly onto test PCBs using thermosonic flip-chip bonding. The power consumption is around 20mW/Gb/s for Tx and Rx together, and a new version of the Rx chip is under development including a 100Gb/s CDR and reduced power consumption aiming at 10mW/Gb/s for a 100Gb/s transceiver. Experimenting with fiber-optic front-ends to evaluate 3-level duobinary signaling for active optical cabling beyond 56Gb/s is planned for the near future. So far 3-level duobinary received little attention in standardization bodies, but our full implementation of the high-speed signal path shows that 100Gb/s duobinary is an elegant solution, not too complex, but offering high performance and good power efficiency with mature IC technology.
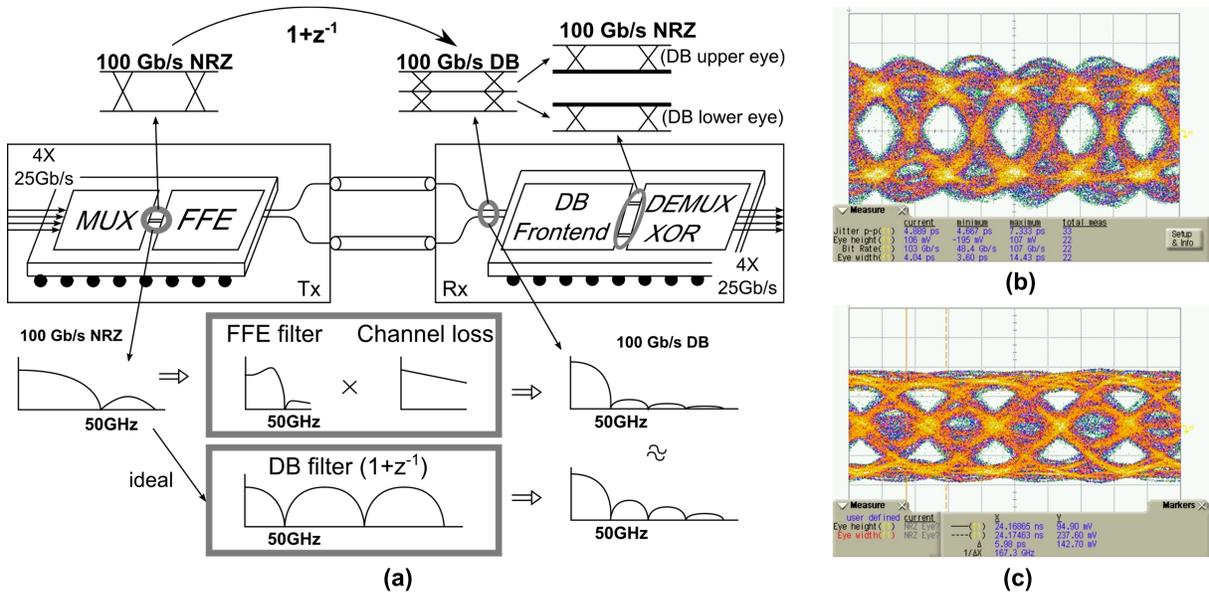
Fig. 1 (a) 100Gb/s duobinary Tx/Rx functionality and working principle (b) 100Gb/s NRZ eye diagram, 50mV/division (c) 100Gb/s duobinary eye diagram, 100mV/div

3. Short-reach single-mode interconnects

As the IEEE 802.3bs Task Force is adopting PAM-4 as a next modulation scheme for 400 Gigabit Ethernet (GbE) single-mode fiber (SMF) links, there is a strong need to develop 50Gb/s (and 100Gb/s) PAM-4 optoelectronic transmitters and receivers. The PAM-4 format is also considered within the Optical Internetworking Forum (OIF) for the upcoming CEI-56G specification. These high data rates require a transition from multi-mode fiber to SMF for the specified 400GbE distances beyond 500m, while still maintaining low power consumption for the link. Single-mode Vertical Cavity Surface Emitting Lasers (VCSELs) at 1310nm or 1550nm are very promising cost-effective emitters for these applications. State-of-the-art single-mode VCSELs are showing bias-dependent bandwidths up to 18 GHz [3]. However, custom drivers with FFE are needed to compensate the non-linear modulation response of the VCSEL for PAM-4 modulation. Today, the fastest VCSEL drivers are designed for multi-mode common-cathode VCSEL arrays at 850nm [4]. Single-mode VCSEL arrays on the other hand are fabricated in common-anode arrays and require higher drive currents. To this end, we have designed a two-channel VCSEL driver IC, compatible with TUM's and Vertilas' single-mode common-anode VCSELs featuring a 4-tap FFE topology. Fig. 2 (a) shows the die micrograph and (b) shows the electrical output at 64Gb/s, measured with a 50Ω GSG probe.
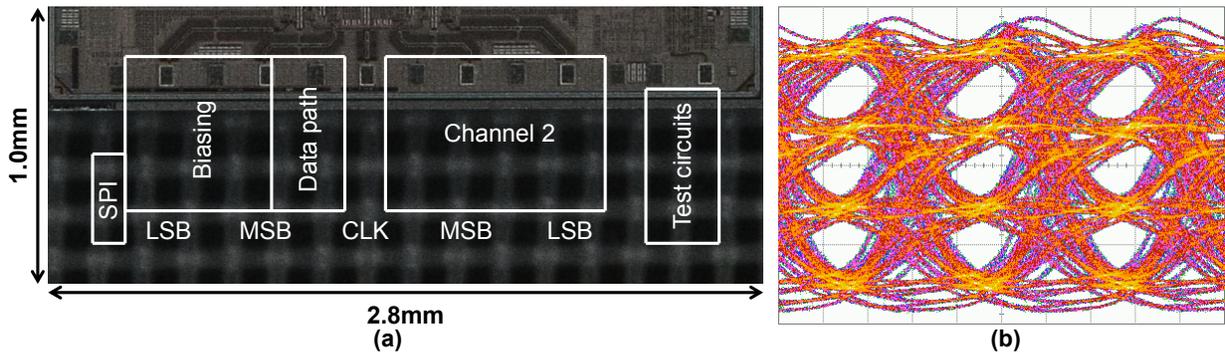

Fig. 2 (a) +56Gb/s PAM-4 VCSEL driver IC (b) electrical drive signal at 64Gb/s (10ps/div, 77mV/div)

Single-ended inputs are used for the clock, the most significant bit (MSB) and the least significant bit (LSB) signals to ease the interfacing and board design. The full-rate clock signal synchronizes the MSB/LSB signals, as PAM-4 signals are sensitive to timing mismatches. The same clock is used to create the FFE delays. Tunable delay cells and an additional flip-flop relax the setup and hold time requirements. The back termination resistor is derived as a compromise between power consumption and the bandwidth enhancement of the electro-optic response. To our

knowledge, this is the first +56Gb/s PAM-4 driver IC for long-wavelength VCSEL arrays. The integration and testing with single-mode VCSELs is being prepared at the time of writing.

PAM-4 links require a linear receiver. Our linear transimpedance amplier (TIA) array consists of two identical channels, which are mirrored in the layout as shown in Fig. 3(a). The data path contains a TIA core, linear main amplifiers and a 50Ω output buffer. To ensure linear operation for PAM-4, an automatic gain control (AGC) block monitors and adjusts the differential output voltage. A logarithmic amplifier is used for this purpose as this allows the dynamic behavior of the AGC to be independent of the signal level. The AGC output is digitized and fed back to the on-chip channel controller.
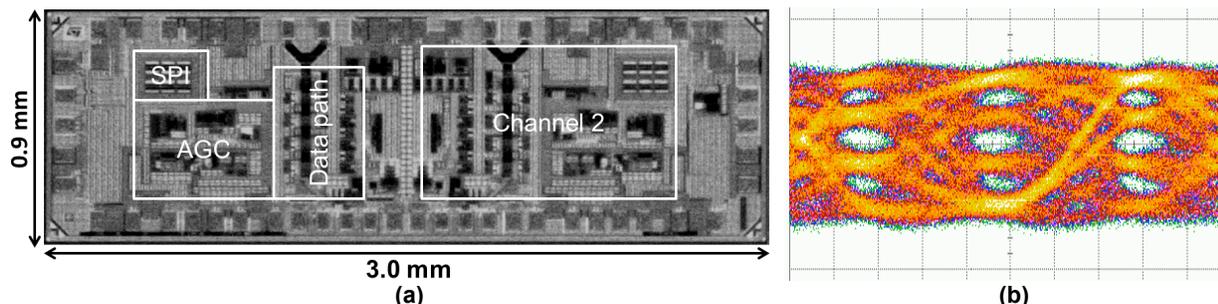

Fig. 3 (a) +56Gb/s PAM-4 TIA IC (b) receiver PAM-4 eye diagram at 64Gb/s (10ps/div, 50mV/div)

The linear TIA array has been wire-bonded to a photodiode array and the receiver was evaluated at 25, 28 and 32 Gbaud. As shown in Fig. 3 (b), the measured output eye diagram is noisy for weak signals, but still quite open at 32 Gbaud (64 Gb/s). The clear separation of the symbol levels implies sufficient reception performance, which was confirmed by the BER lying well below the FEC limit [5]. In addition, this linear TIA array has been integrated with a single-polarization silicon photonic coherent receiver. Operation below the FEC limit for both QPSK and 16-QAM at 28 Gbaud was obtained [6]. Besides short-reach multi-level and long-reach coherent applications, linear TIAs are also very critical components for future radio-over-fiber communication links, for which the TIA dynamic range, linearity and power consumption need to be optimized, for integration in remote antenna units.

3. Segmented Mach–Zehnder modulator driver electronics

Instead of generating a multilevel signal electrically and applying such electrical multilevel signal through a linear driver to a linear emitter, it is also possible to generate optical multilevel signals with a segmented Mach–Zehnder modulator (MZM) [7]. In a segmented MZM, the electrode is split in different pieces, which can be individually driven. Turning on/off the various segments, it is possible to create a multitude of optical levels, while the multi-segment driver should simply turn on or off the segments. As such, an optical digital-to-analog converter (DAC) is realized. Segmented MZMs are now mainly considered as a power efficient solution (no electrical DAC and no linear driver needed) for advanced modulation in coherent transport networks, however, this is actually also a promising technique for the generation of spectrally efficient radio over fiber signals.

4. Conclusions

This paper presented our recent developments towards 100Gb/s copper, +56Gb/s multi-channel single-mode VCSEL links and segmented MZM drivers for advanced coherent or radio over fiber modulation.

5. Acknowledgement

6. References

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