Dynamic properties of silicon-integrated short-wavelength hybrid-cavity VCSEL

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ABSTRACT

We present a vertical-cavity surface-emitting laser (VCSEL) where a GaAs-based "half-VCSEL" is attached to a dielectric distributed Bragg reflector on silicon using ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding, creating a hybrid cavity where the optical field extends over both the GaAs- and the Si-based parts of the cavity. A VCSEL with an oxide aperture diameter of 5 μm and a threshold current of 0.4 mA provides 0.6 mW output power at 845 nm. The VCSEL exhibits a modulation bandwidth of 11 GHz and can transmit data up to 20 Gbps.

Keywords: High-speed modulation, large signal modulation, optical interconnects, semiconductor lasers, silicon photonics, vertical-cavity surface-emitting laser (VCSEL).

1. INTRODUCTION

Silicon photonics (SiP) has attracted significant attention over the last years as a platform for photonic integrated circuits (PICs), with applications in e.g. optical communication and sensing. Due to silicon's lack of efficient light generation, integration of light sources based on materials with high radiative efficiency is needed for SiP to develop its full potential. For this purpose, heterogeneous integration of direct bandgap III-V material is a most promising approach[1].

For applications requiring wavelengths in the visible and very near-infrared, such as life sciences and short reach optical interconnects, the SiP-PICs use silicon nitride (SiN) waveguides due to their transparency at these wavelengths[2]. This also enables the use of GaAs-based optoelectronics, such as the GaAs-based vertical-cavity surface-emitting lasers (VCSELs). GaAs-based VCSELs have reached power efficiencies exceeding 60%[3] and are the most energy-efficient high-speed light sources available today with modulation bandwidths up to 30 GHz[4], data rates above 70 Gb/s[5], and energy dissipation below 100 fJ/bit at data rates up to 50 Gb/s[4,6].

A hybrid vertical cavity can be created by heterogeneous integration of a "half-VCSEL" on a Si-based reflector[7,8]. With the optical field extending over both the III-V- and the Si-based parts of the cavity, some of the light can be tapped off to an in-plane waveguide. This can, for instance, be accomplished using an intra-cavity SiN waveguide with a weak diffraction grating[9] (Figure 1). The dielectric distributed Bragg reflector (DBR) can be replaced by a high-contrast grating (HCG) connected to the in-plane SiN waveguide[8,10,11]. The use of an HCG as bottom reflector also allows for setting the wavelength of individual VCSELs by the grating parameters[12,13]. Together with an integrated wavelength multiplexer, this would enable the fabrication of a fully integrated transmitter for wavelength division multiplexed (WDM) interconnects[14].

As a first step towards heterogeneous integration of GaAs-based VCSELs on a SiN waveguide platform we here present a surface-emitting hybrid-cavity VCSEL where a GaAs-based "half-VCSEL" has been attached to a Si-based dielectric DBR using ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding[15]. This allows us to develop and evaluate the integration concept and to investigate the impact of high thermal impedance Si-based reflectors, such as dielectric DBRs and HCGs, on the static and dynamic VCSEL performance.
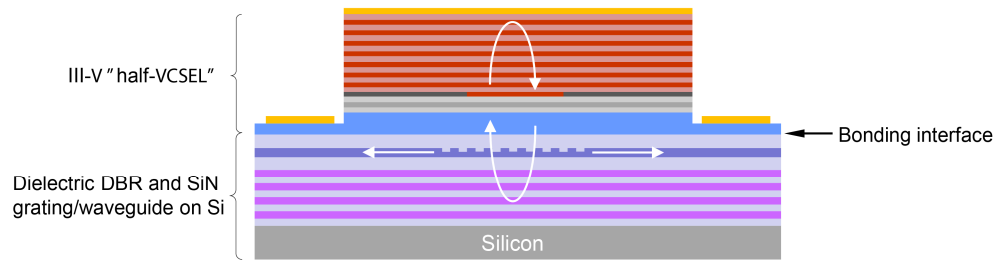
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Figure 1. Schematic cross-section of a hybrid-cavity VCSEL with an intra-cavity diffraction grating to tap off optical power into an in-plane SiN waveguide.

The paper is organized as follows. Section 2 covers the integration concept and the VCSEL design, whereas the fabrication technique is described in Section 3. The static and dynamic characteristics are presented in Section 4 and data transmission experiments are presented in Section 5. Finally, the paper is summarized in Section 6.

2. INTEGRATION AND VCSEL DESIGN

The Si-integrated short-wavelength hybrid-cavity VCSEL is formed by attaching a GaAs-based "half-VCSEL" epitaxial structure to a Si-based reflector using ultra-thin DVS-BCB adhesive bonding. The design is schematically illustrated in Figure 2(a) and the refractive index profile together with the simulated optical intensity along the optical axis is shown in Figure 2(b). Here, the bottom reflector is a 20 pair SiO_2/Ta_2O_5 dielectric DBR on a Si substrate.
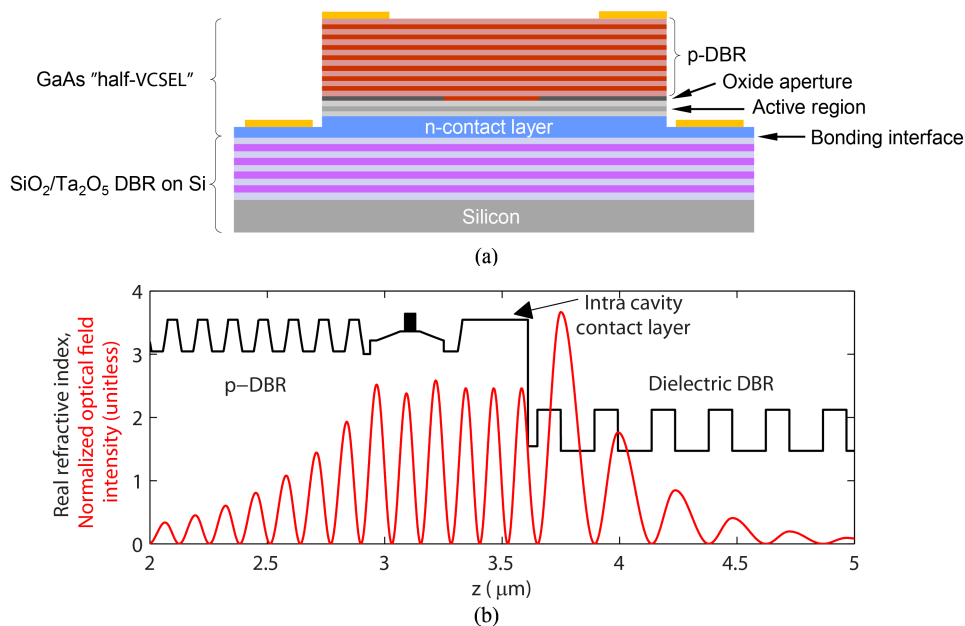

Figure 2. (a) Schematic cross-section of the hybrid-cavity VCSEL. (b) Refractive index profile and simulated optical intensity along the optical axis of the VCSEL.

The GaAs-based "half-VCSEL" epitaxial structure was grown on a GaAs substrate by MOCVD at IQE Europe Ltd. The design is presented in detail elsewhere[16]. In short, the design comprises a 23 pair p-doped AlGaAs-based DBR containing a 30 nm thick $Al_{0.98}Ga_{0.02}As$ layer to enable the formation of an oxide aperture, an active region with five InGaAs quantum wells (QWs), and an n-doped AlGaAs intra-cavity contact and current spreading layer. The photoluminescence (PL) peak from the QWs is at 840 nm.

3. FABRICATION

The fabrication process flow (which is described in detail elsewhere[16]) is illustrated in Figure 3. The GaAs-based "half-VCSEL" epitaxial structure was attached to the dielectric DBR using ultra-thin DVS-BCB adhesive bonding. The bonding process comprises spin-coating of diluted DVS-BCB onto the dielectric DBR on Si, followed by a partial cure. The GaAs die was placed on top of the dielectric DBR, with the epitaxial structure facing the dielectric DBR. The BCB was fully cured while the two substrates were clamped together. The resulting BCB bonding layer is 40 nm thick. The bonding was followed by removal of the GaAs substrate. The first part of the substrate was removed by mechanical thinning. The rest of the substrate was removed using selective wet etching. The resulting resonance wavelength of the cavity was measured at 843 nm. With the PL peak at 840 nm the PL-to-resonance detuning is only 3 nm.

The bonding and substrate removal was followed by standard processing for oxide-confined VCSELs. Ti/Pt/Au *p*-contact rings were deposited, followed by dry etching of circular mesas using inductively coupled plasma reactive ion etching with $SiCl_4$ chemistry. The *in-situ* etch depth was monitored using a laser interferometer endpoint system to accurately stop within the thin intra-cavity contact layer and expose the $Al_{0.98}Ga_{0.02}As$ for oxidation. The mesa surface was protected during the oxidation by a thin layer of Si_xN_y deposited by plasma-enhanced chemical vapor deposition. Before the apertures were formed in a wet oxidation furnace, the Si_xN_y was removed on the mesa side walls. Subsequently, Ni/Ge/Au *n*-contacts were deposited and annealed in an inert N_2 atmosphere. Finally, the VCSELs were planarized with a thick BCB layer to enable deposition of ground-signal-ground (GSG) Ti/Au bondpads. A fully processed VCSEL is shown in Figure 4. Figure 4(a) shows scanning electron microscope (SEM) images of a focused ion beam (FIB) cross-section with the oxide aperture visible, and Figure 4(b) shows a microscope top image of a VCSEL.
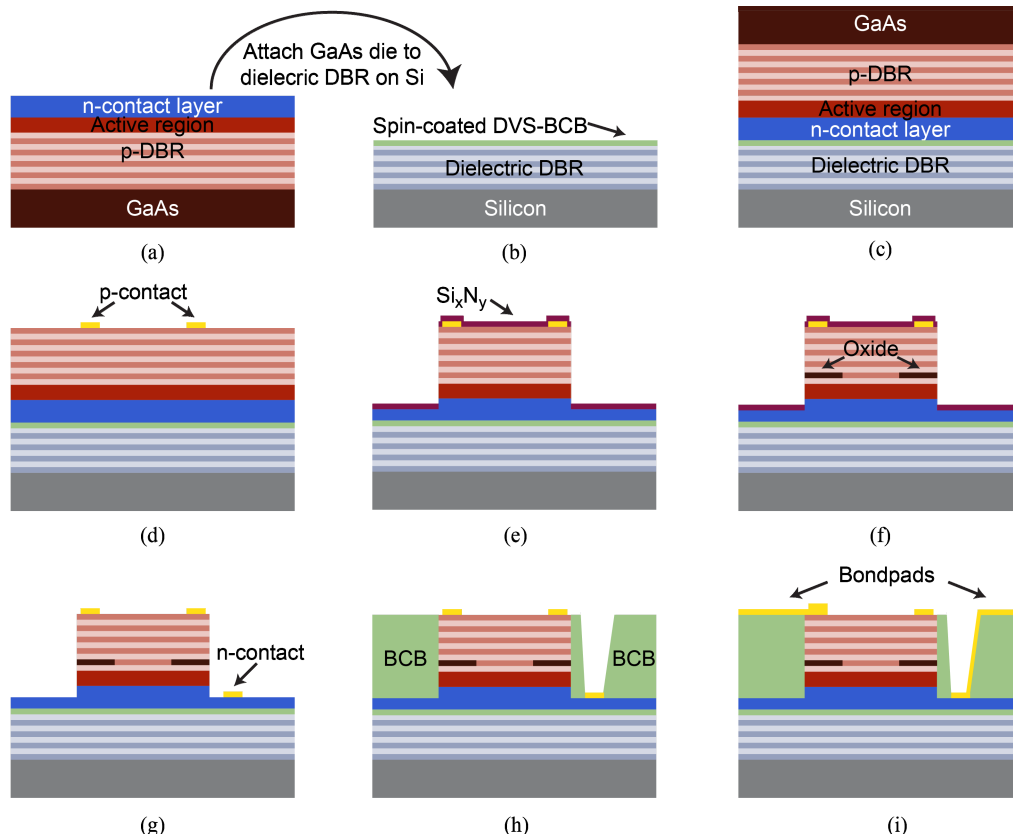

Figure 3. Fabrication process flow for the Si-integrated hybrid-cavity VCSEL: the GaAs-based "half-VCSEL" epitaxial structure (a) is attached to the dielectric DBR on Si, spin-coated with DVS-BCB (b–c). The GaAs substrate is removed, followed by *p*-contact deposition (d). After mesa etching and Si_xN_y deposition/opening (e), an oxide aperture is formed (f), the Si_xN_y is removed, and the *n*-contact is deposited (g). Finally, the structure is planarized with BCB (h) to allow for deposition of bondpads (i).
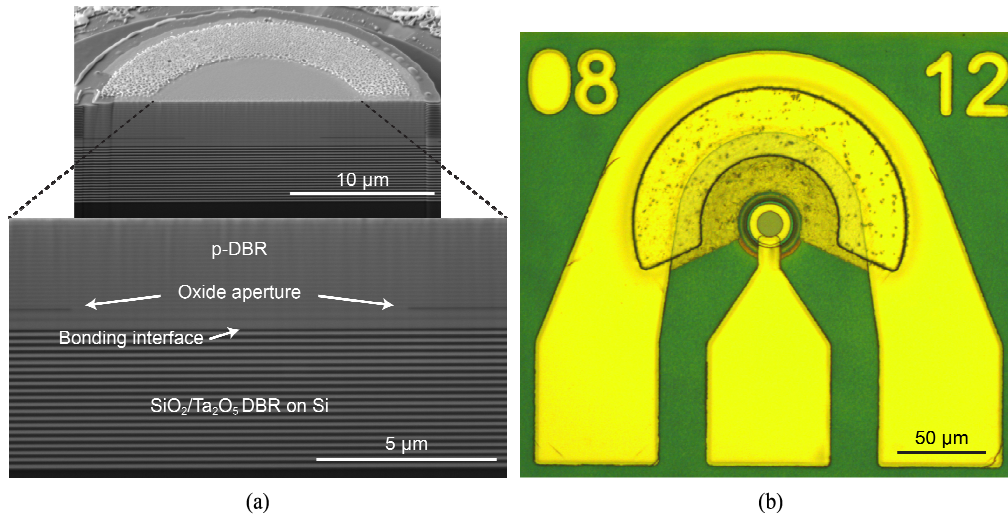
Figure 4. Fully processed VCSEL shown by (a) SEM images of a FIB cross-section and (b) an optical microscope image of the VCSEL surface.

The top *p*-contact layer has a thickness of $\lambda/2$, producing an anti-phase reflection at the surface to facilitate post process tuning of the photon lifetime[17]. This thickness was adjusted to $\lambda/4$ by low power Ar ion milling (longer photon lifetime) to achieve sufficient damping of the modulation response under large signal modulation and data transmission[18].

4. STATIC AND DYNAMIC CHARACTERISTICS

All measurements were performed with the VCSELs on a temperature-controlled heat-sink held at 25°C. The continuous wave light-current-voltage characteristics of VCSELs with oxide aperture diameters of 3, 5, and 7 µm, measured using a free-space large area silicon photodetector, are shown in Figure 5. The emission spectrum for the 5 µm aperture VCSEL, biased at 3.5 mA, which shows lasing with multiple transverse modes around 845 nm, is included as an inset to Figure 5. The 5 µm oxide aperture VCSEL has a low threshold of 0.38 mA and a differential resistance of 73 Ω at thermal rollover. The slope efficiency is 0.25 W/A and the maximum output power is 0.60 mW[19].
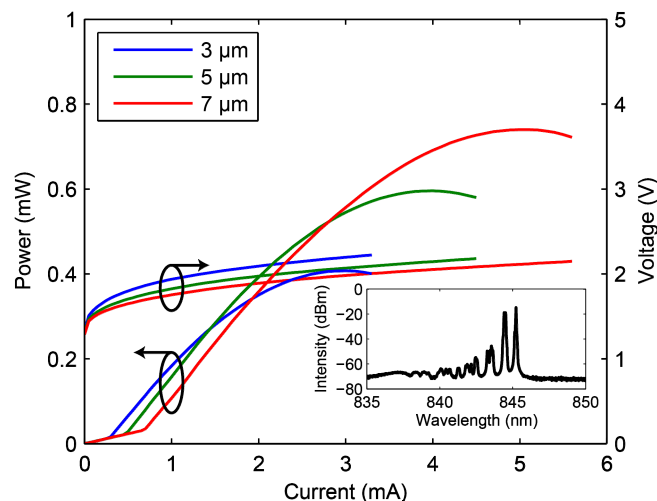

Figure 5. Measured light-current-voltage characteristics for hybrid-cavity VCSELs with oxide aperture diameters of 3−7 µm. Inset: Spectrum for a 5 µm aperture VCSEL biased at 3.5 mA.
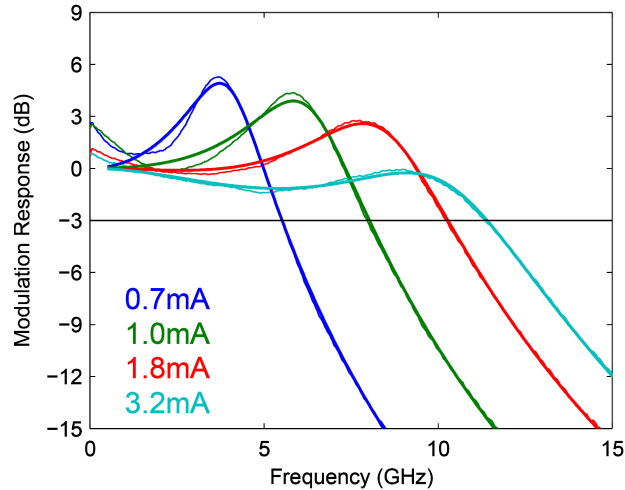
Figure 6. Small signal modulation response for a 5 μm oxide aperture diameter hybrid-cavity VCSEL at indicated bias currents.

As can be seen in Figure 5, the VCSELs suffer from an early onset of thermal rollover. We attribute this to the limited heat transport through the dielectric DBR due to its high thermal impedance. To investigate the thermal impact of the dielectric DBR, the thermal impedance was measured to 10.7 K/mW[19] for the 5 μm oxide aperture diameter VCSEL, by tracking the redshift of the fundamental optical mode with dissipated power and stage temperature. The thermal impedance is ~3 times higher than for conventional GaAs-based oxide-confined VCSELs[20].

The PL-to-resonance detuning of only 3 nm is another contributor to the early rollover. The small detuning results in minimum threshold current far below room temperature (–16°C)[16]. This can be mitigated by increasing the BCB bonding layer to 60–80 nm to redshift the resonace wavelength.

Higher maximum output powers of up to 1.6 mW (9 μm oxide aperture diameter VCSEL) and slope efficiencies of 0.5 W/A were reached with a lower reflectance top DBR (reduced photon lifetime), simultaneously also causing a higher threshold current[16]. However, this reduces the damping of the modulation response, which causes excessive ringing under large signal modulation and link performance degradation.

The small signal modulation response of the 5 μm VCSEL at four bias currents is shown in Figure 6. The maximum 3 dB modulation bandwidth is 11 GHz (at 3.2 mA bias current). K- and D-factors of 0.2 ns and 7.2 GHz/mA$^{1/2}$, respectively, were extracted from the measured small signal response[19]. The bandwidth is mainly limited by thermal effects and parasitics, due to the high thermal impedance of the dielectric DBR and the high capacitance across the single oxide layer, respectively.

5. LARGE SIGNAL MODULATION AND DATA TRANSMISSION

Error-free (defined as bit error rate [BER] < 10^{-12}) data transmission was possible up to 20 Gbps by direct modulation of the 5 μm oxide aperture diameter hybrid-cavity VCSEL, biased at 3.5 mA[19]. The limiting photoreceiver has a bandwidth of 30 GHz and the applied pseudo random bit sequences (PRBSs) voltage signal (0.4 V_{pp}) had a pattern length of $2^7 - 1$. The BER measurements at 10, 15, and 20 Gbps, with the corresponding eye diagrams of the received signal, are shown in Figure 7.

The bias current of 3.5 mA is close to thermal rollover of the 5 μm oxide aperture diameter VCSEL, which is needed to achieve sufficient damping of the modulation response. However, there is still overshoot and ringing in the optical signal, which translates into timing jitter in the limiting photoreceiver[18].
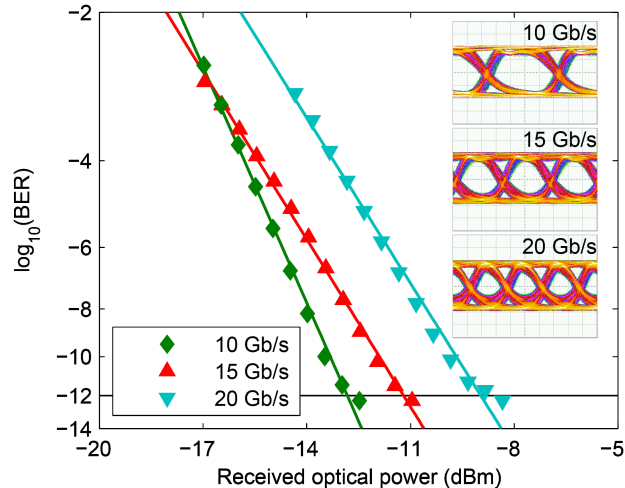
Figure 7. BER measurements at 10, 15, and 20 Gbps with a 5 μm oxide aperture diameter hybrid-cavity VCSEL, biased with 3.5 mA, with the corresponding eye diagrams as inset. Scales: 100 mV/div and 20 ps/div.

6. SUMMARY

We have presented a heterogeneously integrated short-wavelength hybrid-cavity VCSEL on a Si substrate. A 5 μm oxide aperture diameter hybrid-cavity VCSEL with a sub-milliampere threshold current has a small signal modulation bandwidth of 11 GHz and is capable of error-free data transmission at data rates up to 20 Gbps, in spite of the high thermal impedance and the large capacitance.

ACKNOWLEDGMENTS

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