DVS-BCB ADHESIVE BONDING FOR SILICON PHOTONICS

S. Keyvaninia[1,2] , M. Muneeb[1,2] , S. Stanković[1,2], S. Ghosh[1,2], M. Tassaert[1,2], D. Van Thourhout[1,2], G. Roelkens[1,2]
[1]Photonics Research Group, INTEC, Ghent University-IMEC, Sint-Pietersnieuwstraat 41, B-9000 Ghent. [2]Center for Nano- and Biophotonics (NB-Photonics), Ghent, Belgium

Abstract
A new process for bonding of III-V dies to processed silicon-on-insulator waveguide circuits using divinylsiloxane-bis-benzocyclobutene (DVS-BCB) was developed using a commercial wafer bonder. High-quality bonding, with ultra-thin bonding layers (< 50 nm) is demonstrated, which is suitable for the fabrication of heterogeneously integrated photonic devices, specifically hybrid III-V/Si lasers and photodetectors.

Introduction
Silicon photonics, based on the silicon-on-insulator (SOI) material platform, is emerging as an important platform for the realization of high-speed optical transceivers. Moreover, standard complementary metal oxide semiconductor (CMOS) processing infrastructure can be used to process these optical components [1]. This allows high-yield fabrication and a reduction of the component cost through economies of scale. However, the fabrication of efficient light sources in silicon photonics is challenging due to silicon's indirect bandgap. In order to create photonic integrated circuits comprising both opto-electronic and passive optical components, the heterogeneous integration of passive silicon-on-insulator waveguide circuits and active InP/InGaAsP components has been proposed [2-3], for applications in the telecommunication wavelength range.
Semiconductor wafer bonding allows the integration of high-quality III-V epitaxial layers on top of the silicon platform by transferring the III-V layer stack from its original growth substrate to the SOI wafer. Full wafer bonding, multiple die-to-wafer bonding or single die bonding can be envisaged, depending on the application. In all cases, an unprocessed III-V semiconductor epitaxial layer stack is transferred, which reduces the time required to complete the integration process compared to a flip-chip process, as no stringent alignment accuracy is needed because of the absence of structures on the dies or wafers. After removal of the growth substrate, the optoelectronic components can be fabricated in the bonded epitaxial layer. DVS-BCB is a good candidate for hybrid bonding because of its excellent physical properties such as low dielectric constant, low moisture absorption, low curing temperature, high degree of planarization, low level of ionic contaminants, high optical clarity, good thermal stability, excellent chemical resistance, and good compatibility with various metallization systems [4].
In this paper we describe a new adhesive wafer bonding process scheme that involves partial curing of the DVS-BCB prior to bonding and attaching the III-V substrate at room temperature prior to curing in a vacuum atmosphere. This 'cold bonding' method significantly simplifies the bonding preparation for machine-based bonding both for die and wafer-scale bonding. This approach shows high yield for ultra-thin bonding thicknesses below 50 nm, as well as good uniformity of the DVS-BCB layer thickness after wafer bonding over the full wafer area. This process was applied to achieve ultra-thin DVS-BCB bonding layers for the fabrication of several photonic devices, such as III-V/SOI lasers and optical isolators.

DVS-BCB wafer bonding processes
The bonding process was developed for a wafer level epitaxial layer transfer; however, as will be shown later, it can also be applied to multiple die-to-wafer bonding and single-

die bonding. A MicroTec ELAN CB6L wafer bonder was used for bonding experiments. Commercial DVS-BCB solutions are limited in available spin-coated layer thicknesses down to 1µm (for Cyclotene®™ 3022-35 from Dow Chemical). Since this work deals with bonding layer thicknesses that are an order of magnitude smaller, mesitylene is added to Cyclotene 3022-35 to reduce the spin-coated layer thickness substantially.
The processing procedure is schematically illustrated in Figure. 1. The bonding process starts with the cleaning of the SOI substrate and III-V dies. The SOI cleaning is performed by immersing the substrate for 15 minutes into a Standard Clean 1 (SC-1) solution, comprising aqueous ammonia (NH4OH), hydrogen peroxide (H2O2) and deionized (DI) water in volume ratios of 1:1:5, respectively, which is heated to 70 °C. After this, the DVS-BCB:mesitylene solution is spin-coated onto the SOI substrate. The SOI substrate is then baked for 10 min at 150 °C, to let mesitylene evaporate, after which the substrate is slowly cooled down to room temperature. Finally, the SOI is mounted on a carrier wafer made of Pyrex glass (1200 um thick, 100 mm diameter). Meanwhile, prior to bonding, a sacricifial InP/InGaAs sacrificial layer pair on the III-V wafer/die is removed by selective wet etching using HCl:H2O and H2SO4:H2O2:H2O in volume ratios of 4:1 and 1:1:18 respectively. This procedure removes particles and contaminants from the III-V die surface. The III-V die is then rinsed with DI water, dried and mounted on the SOI die. Since in the presented method the dies are contacted at room temperature, individual dies can easily be pick-and-placed onto the silicon target wafer. They can be aligned manually with an accuracy of 500µm without any extra tools or can be placed more accurately using a flip-chip machine. After that, the SOI substrate on its carrier wafer is mounted on the transport fixture and is loaded into the processing chamber of the wafer bonding tool. The chamber is pumped-down (target pressure 10-3 mbar) and heated to 150°C with a ramp of 15 °C/min for 10 min, while applying pressure on the III-V/SOI stack.

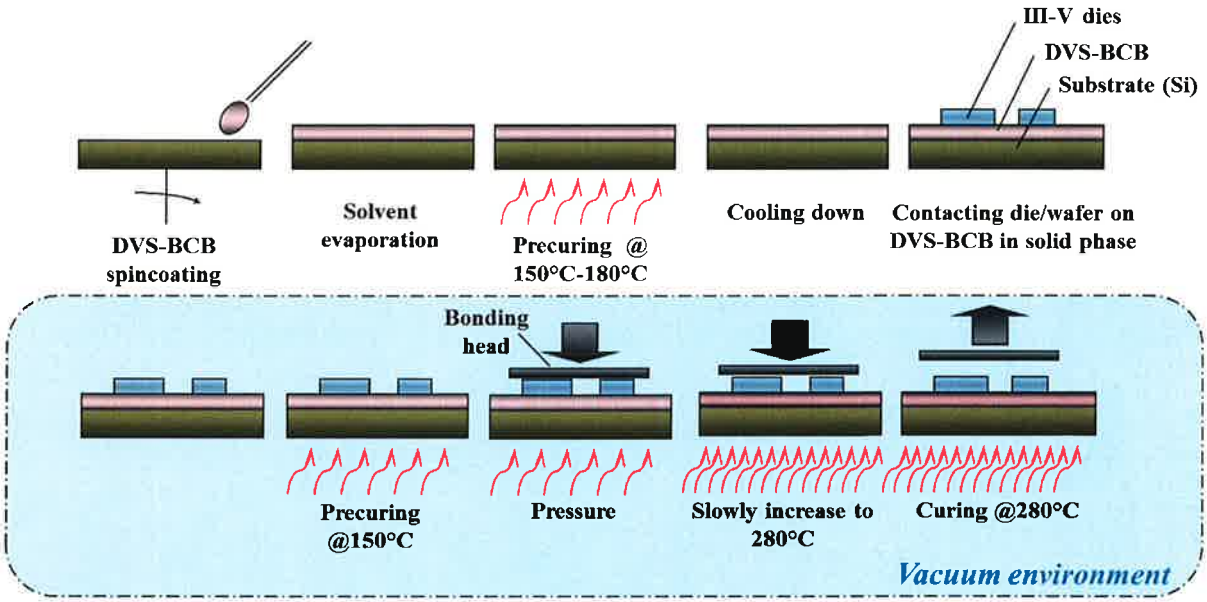


Figure 1: Developed bonding process, referred to as 'cold bonding'.

The actual bonding pressure (the applied force per area of the III-V die) is kept in the range of 200 to 400 KPa. After keeping the pressure on the dies for 10 min at 150 °C, temperature is increased up to 280 °C, with a ramp of 1.5 °C/min. Upon reaching 280 °C, the dies are kept at this temperature for 60 min in a nitrogen atmosphere. After the curing, the bonded samples are cooled down (at 6-10 °C/min) and unloaded from the processing chamber. The InP substrate of the III-V die is then removed by a selective wet etching using HCl, leaving a thin III-V film with the functional layers bonded to the SOI die, ready for further processing. An alternative method has been reported earlier by our group [5], in which adhesive die-to-wafer bonding was demonstrated in a commercial

wafer bonder. In this method spacers are used to keep the die and substrate separate prior to loading the stack in the bonding tool. In this new method no carrier is required to load the top wafer/die into the machine and no vacuum or heating is required prior to contacting the wafers in the bonding chamber. This makes the process more straight forward. Moreover, with the previous recipe, it was not possible to perform multiple die-to-wafer bonding for dies with different thickness. Using this new method we demonstrate that multiple-die bonding with different die thickness is feasible [6].

Bonding Experiments

The bonding recipe was originally developed for ultra-thin DVS-BCB bonding layers, suitable for the fabrication of photonic devices, specifically hybrid III-V/Si lasers. Several bonding experiments were performed to evaluate the bonding quality and the DVS-BCB thickness uniformity after wafer bonding. The experimental results on wafer-to-wafer, die-to-wafer and multiple die-to-wafer bonding are presented in Figures 2 (a-h). A uniform DVS-BCB thickness for different points distributed over the bonded surface is obtained, with an average bonding layer thickness of 29nm, varying by +/- 3 nm over 2 inch wafer bonding area [6].

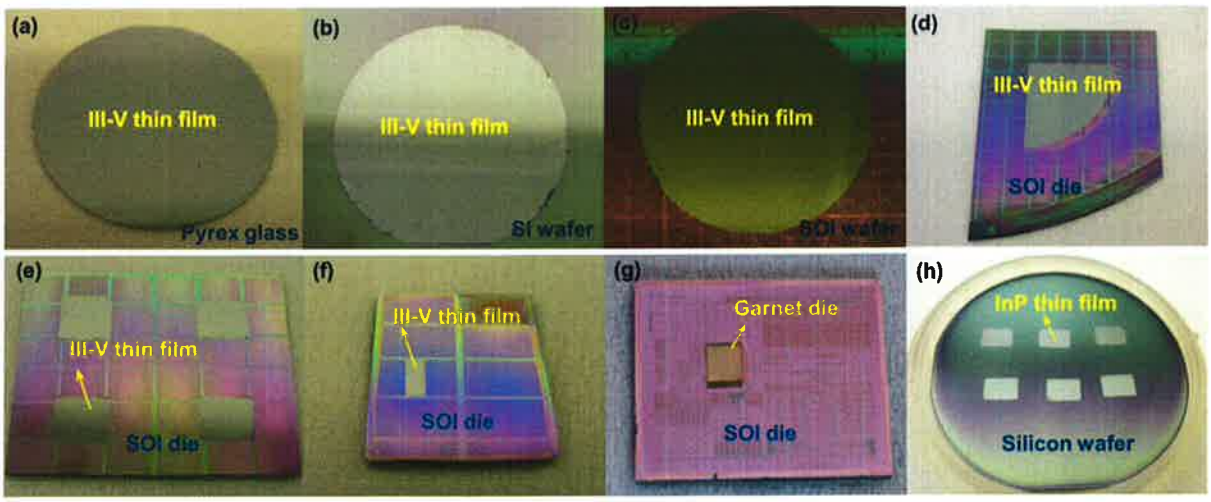


Figure 2: A full wafer 300nm InP membrane bonded on a Pyrex glass wafer (a), a 100 mm silicon wafer (b) and a quasi-planarized SOI wafer (c) epitaxial quarter III-V wafer bonded on quasi-planarized SOI (d) after substrate removal; four epitaxial 0.3 cm^2 III-V dies bonded (e) 1.3 mm by 4 mm die transferred on a quasi-planarized SOI after the substrate removal process; (f) 0.04 cm^2 garnet (magneto-optic material) bonded on SOI [7] (g) 6 InP-membranes (with an individual die area of 0.2 cm^2) bonded on a 50 mm silicon wafer [8].

Commercial silicon and CMOS production is carried out on wafer diameters of 200 mm and above, while III-V substrates used in photonics applications have typical diameters of less than 100 mm, indicating that wafer-to-wafer bonding will often not be the preferred approach. Moreover, bonding of large III-V areas would result in a waste of material in chip areas were the transferred material is not needed. Therefore, a cost-effective approach in heterogeneous integration requires III-V material or other optical materials to be bonded in small areas of the SOI photonic wafer. We focus on a multiple die-to-wafer bonding process where III-V dies would be bonded to a SOI die or a full SOI wafer. Since the presented method uses contacting of the dies at room temperature, individual dies can easily be pick-and-placed onto a silicon target wafer. They can be aligned with an accuracy of 500µm without any extra tools or can be placed more accurately using a flip-chip machine. The results are shown in Figures. 2 (e-f).

While in the previous experiments nominally identical III-V dies were used, in particular situations there is a need for bonding different types of III-V dies on a single SOI die or wafer (e.g. a die containing laser epitaxy and a die containing photodetector epitaxy). This typically results in dies of different height and size to be bonded, which is difficult to achieve using the classical bonding recipe. Here we show that by applying the new bonding recipe, in combination with a graphite foil between the dies and the bonding head, four-die bonding using two different epitaxial layer stacks (with about 50 µm difference in substrate thickness) can be achieved. The graphite foil is used to compensate for these thickness variations in order to distribute the pressure evenly over all dies during the bonding, as is illustrated in Figure 3.

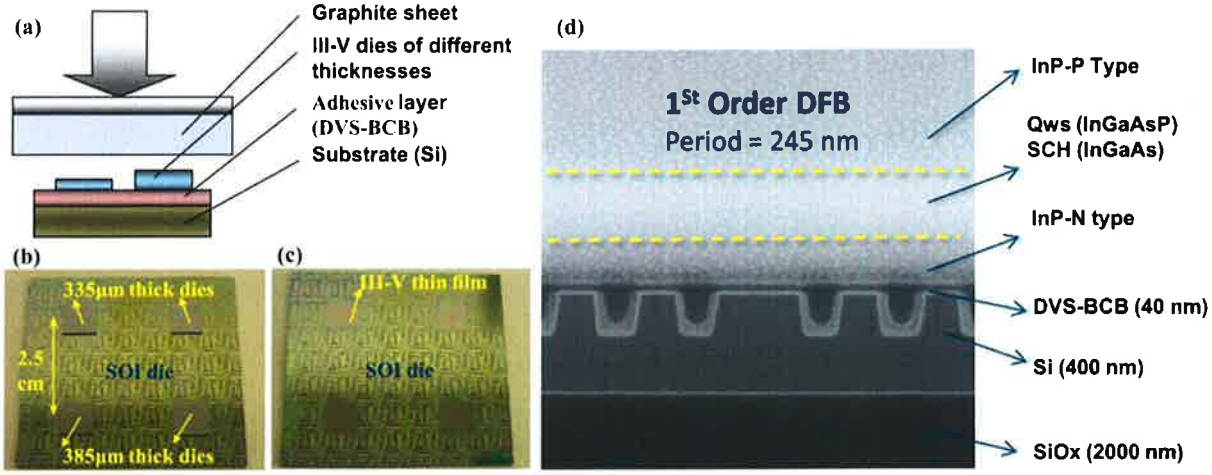


Figure 3: Four-die bonding on planarized SOI with different substrate thickness, using a graphite foil to compensate for die-thickness variations: (a) schematic; (b) before substrate removal; (c) after substrate removal; (d) SEM image of the longitudinal cross section of the λ/4 shift region in the center of the grating for the hybrid DFB laser, while the thickness of the DVS–BCB bonding layer is ~40 nm [3].

Conclusions an Acknowledgements

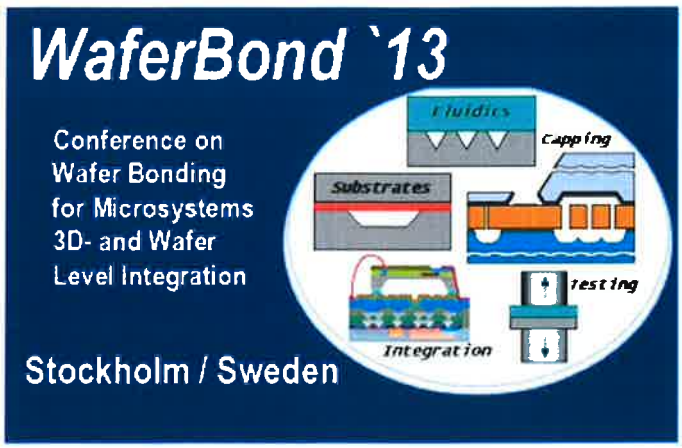
This work is supported by EU-funded project Photonics Electronics functional Integration on CMOS (HELIOS). The authors thank Guang-Hua Duan and Francois Lelarge (III-V lab, Paris) for delivering the III-V epitaxial material used in developing this process.

References

[1] W. Bogaerts, et al., "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," *J. Lightwave Technol.* 23, pp. 401-412 (2005).
[2] G. Roelkens, et al., "III-V/silicon photonics for on-chip and intera-chip optical interconnects," *Laser & Photonics reviews* **4**, pp. 751-779 (2010).
[3] S. Keyvaninia, et al., "Heterogeneously integrated III-V/silicon distributed feedback lasers," *Optics Letters*, in press.
[4] F. Niklaus., et al., "Adhesive wafer bonding," J. Appl. Phys. 99, 031101 (2006).
[5] S. Stanković, et al., "Die-to-die adhesive bonding for evanescently-coupled photonic devices," Electrochem. Solid-State Lett. **14**, pp. 326–329 (2011).
[6] S. keyvaninia, et al.,"Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate", *Optical Materials Express*, Vol. 3, Issue 1, pp. 35-46 (2013)
[7] S. Ghosh, et al., 'Adhesively bonded Ce:YIG/SOI integrated optical circulator, *Optics Letters,* 38(6), pp.965-967 (2013)
[8] J. Pello, et al., "High-efficiency ultra-small polarization converter in InP membrane," *Optics Letters,* 37, pp. 3711-3713 (2012).

Stockholm (Sweden), 5th-6th December 2013

WaferBond 13



KTH VETENSKAP OCH KONST

ROYAL INSTITUTE OF TECHNOLOGY

Program

Registration

Conference Location & Hotels

Late Posters

Contact

...will be organized by

KTH Royal Institute of Technology Stockholm.

You are invited to present your latest results in wafer bonding technologies and their application in microsystems technologies, to learn about how to use wafer bonding in complex technologies, get news about wafer bonding equipment as well as about testing of wafer bonded interfaces and finally meet your colleagues working in this field for fruitful discussion.

Practical Information

Partners:

MEMS JOURNAL

Micronews

Sponsors:

EVG

AML

Soitec

MSYS

silex MICROSYSTEMS

Program WaferBond '13

Conference on Wafer Bonding for Microsystems and Wafer Level Integration

Partners:

MEMS JOURNAL

Micronews

Sponsors:

EVG

NIL

3altec

MSYS

silex

SOSS Microtec

FAB

PRIMOCELER
CHALLENGE US

Wednesday 2013-12-04 Pre-Evening-Reception

17:15		ABBA Museum / Melody Hotel, Stockholm

Thursday 2013-12-05 1st Day WaferBond '13

09:00	R. Knechtel	Technical Chair
09:05	F. Niklaus	Local Chair KTH Stockholm
09:20	H. Baumgart	Old Dominion University
Session 1 Fundamentals and New Approaches I		Chairs: H. Malmcas, N. Roxhed
09:40	L. Capello	SOITEC
10:00	A. Mano	Waseda Univ.Japan
10:15	C. Rauer	CEA, LETI, Minatec
10:30		Break
Session 2 Characterisation of Bonded Wafers I		Chairs: M. Petzold, M. Tilli
10:50	S. Brand	Fraunhofer IWM Halle
11:05	P. Sievilä	Univ. Helsinki
11:20	L. Capello, A. Castex	SOITEC
11:35	P. Emery	MENAPIC
11:50	D. Radisson	CEA, LETI, Minatec
12:05		Lunch Break
13:00	Poster Flash Session	Chair: R. Knechtel
Session 3 Low Temperature Wafer Bonding I		Chairs: L. di Cioccio, J. Frömel
14:00	T. Ebefors	Silex
14:20	A.Malko	Chalmers Univ.
14:35	T. Matsumae	Univ. Tokyo
14:50	F. Forsberg	KTH Stockholm
15:05		Break
Session 4 3D Integration		Chairs: M. Wiemer, S. Keyvaninia
15:30	P. Enquist	Ziptronix
15:50	P. Anantha, C.S. Tan	Nanyang Univ.
16:05	K. Hagiwara	NHK Tokyo
16:20	J. Burgraf	EV Group
16:45	K. Szostak	AML
17:05		Bus Departure
17:30		Social Event - Vasa-Museum & Dinner
22:00		

Friday 2013-12-06 2nd Day WaferBond '13

Session 5 Wafer Bonding for MEMS and Special Processes		Chairs: F. Niklaus, R. Knechtel
09:00	M. Tilli	Okmetic
09:20	J. Frömel	Fraunhofer ENAS Chemnitz
09:40	D. Borowsky	Robert-Bosch GmbH
09:55	Lan Peng	IMEC
10:10	T. Suni	VTT
10:25	K. Zoschke	Fraunhofer IZM Berlin
10:40		Break
Session 6 Temporary and Adhesive Wafer Bonding		Chairs: T. Mayer, L. Capello
11:00	S. Keyvaninia	Ghent University
11:20	M. Gabriel	Suss MT
11:35	K. H. Gatty	KTH Stockholm
11:50	A. Jourdain	IMEC
12:05	P. Montmeat	CEA, LETI, Minatec
12:20		Lunch Break
Session 7 Fundamentals and New Approaches II		Chairs: H. Menzel, H. Baumgart
13:10	B. Imbert	CEA, LETI, Minatec
13:30	K. Schjølberg-Henriksen	Sintef Oslo
13:45	E. Navaro	Soitec
14:00	X. Zhang	Chinese Academy
14:15	A. de Pablos-Martin	Fraunhofer IWM Halle
14:30		Break
Session 3 Low Temperature Wafer Bonding II		Chairs: T. Suga, P. Enquist
15:00	T. Shimatsu	Tohoku Univ.
15:15	J. Bräuer	Fraunhofer ENAS Chemnitz
15:30	M. Eichler	Fraunhofer IST Braunschweig
15:45	R. Knechtel	Closing Remarks
16:00		Lab Tour KTH Stockholm

Posters

P1	B. Rebhahn	EV Group
P2	M. Petzold, F. Naumann	Fraunhofer IWM Halle
P3	S. Maus, U. Hansen	MSG Lithoglas GmbH
P4	N. Malik	Sintef Oslo
P5	C. Kaden, S. Langa	Fraunhfer IPMS
P6	A. Lapadatu	Sensonor
P7	M. Goorsky	University of California
P8	F. Saharil	KTH
P9	W.-S. Wang	Fraunhofer ENAS Chemnitz
P10	F. Fournel, E.Beche	CEA, LETI, Minatec
P11	B. Imbert, P. Gondcharton	CEA, LETI, Minatec
P12	T. Rogers	AML
P13	G. Klakowski	Fraunhofer IOF Jena
P14	S. Guenschmann	TU Ilmenau Germany
P15	H. Kon	Tohoku Univ. Japan
P16	M. Goorsky	University of California
P17	S. Dempwolf	X-FAB
P18	M. Schima	Fraunhofer IZM

P1	Analytical methods used for low temperature Cu-Cu wafer bonding process evaluation
P2	Life-time modelling of low temperature Si fusion bonded interfaces with TSV used for 3D MEMS device integration
P3	Anodic Bonding using Evaporated Borosilicate Glass Thin-Films
P4	OPTIMIZATION OF AL-AL THERMOCOMPRESSION BONDING
P5	Wafer level vacuum packaging of micro-mirrors with buried signal lines
P6	Wafer level vacuum encapsulation for uncooled microbolometers
P7	3-d materials integration: Epitaxial transformations and other metallurgical interactions ay metal-bonded interfaces
P8	Dry adhesive bonding of porous alumina membranes to microstructured silicon wafers using the OSTE(+) dual-cure polymer
P9	Application of Nanoporous Gold for Substrate Bonding at Low Temperture
P10	Direct wafer bonding of amorphous or densified atomic layer deposited alumina thin films.
P11	KINETICS IN LOW TEMPERATURE DIRECT COPPER-COPPER BONDING
P12	Wafer bonding with large differential temperature pre-bonding treatment
P13	Direct Bonding of high index coated Fused Silica for optical applications
P14	Silicon-Ceramic-Silicon-Wafercompound fabricated by using nanostructured Siliconsurfaces and a ceramic with adapted thermal expansion coefficient
P15	Room Temperature Bonding of Wafers and Polished Metals using Thin Au Films for Enhancing the Heat Dissipation Efficiency
P16	The role of relative surface orientation on the electrical conductivity of S-terminated III-V bonded heterostructures
P17	Advanced Glass Frit Wafer Bonding
P18	Recent Results and Developments in Temporary Wafer Bonding and Debonding on 300mm Leading Edge Tools