Effect of mask grid on SOI arrayed waveguide grating performance

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***Abstract*—We studied the impact of the lithography mask grid on the performance of silicon AWGs, and show a dramatic improvement in crosstalk of 5dB when going from a 5nm to a 1nm grid.**

I. Introduction

Arrayed waveguide gratings (AWGs) are one of the commonly used devices for wavelength multiplexing [1]. However, in silicon, AWGs have always lagged in performance compared to the other techniques, such as silica [2] and InP [3]. While silicon AWGs can be much smaller because of the high refractive index contrast, the same high index contrast gives rise to phase errors and other parasitics which contribute to the overall crosstalk of the device. In general, silicon AWGs achieve crosstalk levels of -20dB, with the best devices showing -25dB crosstalk [4]–[6].

II. Phase Errors

The key contributor to crosstalk in silicon AWGs is the phase errors that are accumulated along the delay lines. When the distributed light in the waveguides recombines in the free propagation region (FPR), phase errors will translate in ripples in the optical phase front. These ripples will induce sidelobes and overall crosstalk in the image at the output waveguides, resulting in optical power coupled to the wrong outputs. We can distinguish these phase errors in the delay lines into two categories: deterministic and stochastic errors. In the latter category we find sidewall roughness and line-width/thickness variations as key causes. Using wider waveguides in the delay sections can alleviate the impact of theses effects [4]–[7]. For the deterministic errors, we studied the effect of mask discretization on the performance of the AWG.

As the common design of our AWGs uses rectangular waveguide layouts [4]–[6] where the bend sections are generally identical between the delay lines, we first looked at the effect of the mask grid on the straight delay sections of the AWG. The effect is illustrated in Fig. 2. The path for the delay line is calculated along 3 sides of a rectangle (taking into account the length of the bends). During that calculation, the coordinates of the sides are calculated to high precision. However, during subsequent tape-out to a GDSII mask file, the coordinates are snapped to a fixed grid. In practice, we used a 5nm grid, which means the length deviations in each arm could be $\pm$15nm, which translates in phase errors of $\pm\pi/19$. By going to a 1nm grid, these variations drop to $\pm$3nm, or

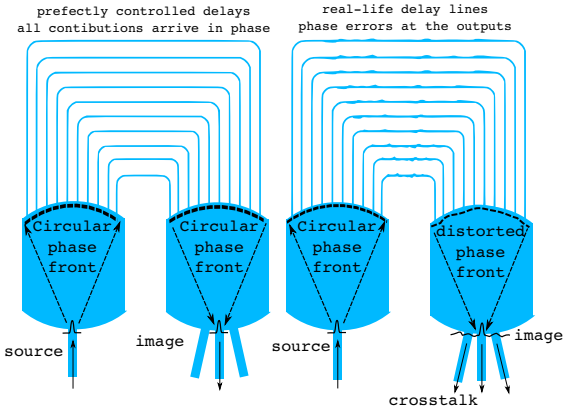

Fig. 1. Schematic diagram of the AWG with ideal delay lines and with phase error affected delay lines.

phase errors of $\pm\pi/96$. While the grid snapping in our mask design is fairly random (a rounding error depending on the calculated delay length), it is a deterministic process: two identically designed AWGs will experience the same phase error contributions from grid snapping.

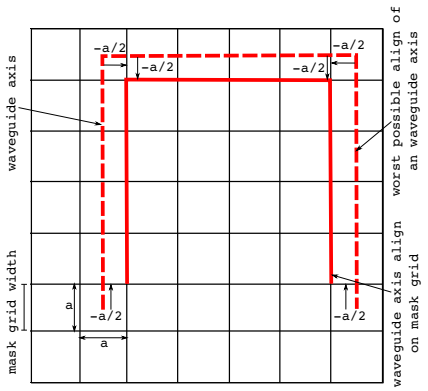

Fig. 2. The length deviation of a waveguides due to the grid snapping.

We studied the effect of phase errors through simulation and experimentally, by designing and simulating a set of identical AWGs on both a 1nm and a 5nm grid, and fabricated them side-by-side.

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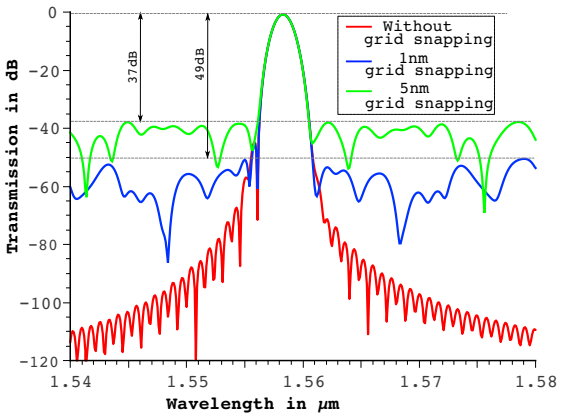

Fig. 3. Simulated transmission spectrum of 16 × 400GHz AWG (8th channel) for 1nm, 5nm and without grid snapping.

TABLE I
COMPARISON OF MEASURED AWG INSERTION LOSS (IL, CENTER CHANNEL AND OUTER CHANNEL) AND CROSSTALK LEVEL BETWEEN 1NM AND 5NM MASK GRID DISCRETIZATION.

Channels	**Spacing** [GHz]	**Area** [μm^2]	**IL** [dB]	**XT 5nm** [dB]	**XT 1nm** [dB]	**FSR** [nm]
4	400	468 × 237	-1.8 -2.2	-22	-27	19
8	400	490 × 307	-1.3 -2.7	-21	-26	32
16	400	530 × 435	-1.5 -3.5	-21	-26	54

III. Simulation

The AWGs are simulated by a semi-analytical model [5] integrated with our design software (IPKISS) [8]. As we want to illustrate the effect on the crosstalk due to the phase errors introduced by the grid snapping we didn't include any stochastic phase error due sidewall roughness.

Fig. 3 shows the simulated spectral response of the 8th channel of a 16 × 400GHz AWG without grid snapping, and for 1nm and 5nm snapping. The simulation indicates, as expected, that the insertion loss will not be affected while the crosstalk floor will increase with increasing grid snapping. In the simulation we can see that the crosstalk is improved by 12dB as we change the grid from 5nm to 1nm.

IV. Experiment

We also fabricated a set of identical AWG designs, but with a different mask discretization. Fig. 4 shows the measured spectral response of a 16 × 400GHz AWG using 5nm and 1nm grid snapping. We see that the crosstalk is substantially higher compare to the simulated AWGs, because other crosstalk mechanisms are still present. But we do see a significant improvement for the 1nm mask grid: The crosstalk floor drops from -21dB for the 5nm grid to -26dB for the 1nm grid, making this the best published device with such a high channel count. Other AWGs, with different channel counts, show similar improvements, as listed in table I.

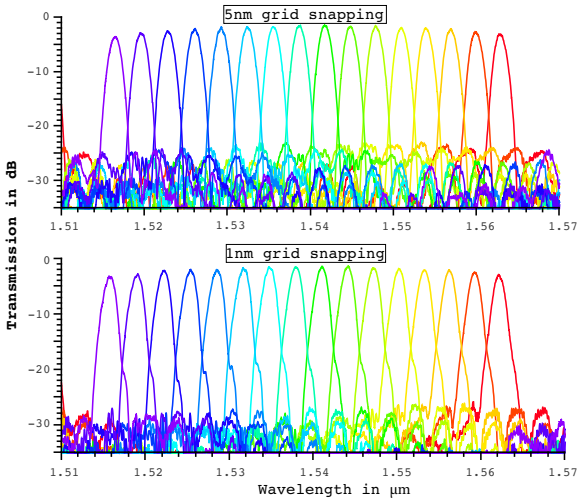

Fig. 4. Experimental transmission spectrum of 16 × 400GHz AWG using 5nm and 1nm grid snapping.

V. Conclusion

We demonstrate a significant improvement in silicon AWGs by going from a 5nm mask discretization to a 1nm mask grid. We see an experimental improvement of 5dB in crosstalk due to snapping-related phase errors. We illustrated this with a 16 × 400GHz AWG with -26dB crosstalk level by reducing the mask grid from 5nm to 1nm.

Acknowledgment

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