Silicon Carrier-Depletion-Based Mach-Zehnder and Ring Modulators with Different Doping Patterns for Telecommunication and Optical Interconnect

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ABSTRACT

In this paper, we review our progress on carrier-depletion-based silicon modulator. The lateral and the interdigitated PN junctions are optimized and then compared systematically. The comparison helps us to choose a proper doping pattern for 40 Gbit/s modulation with MZ structure and travelling wave electrode. Ring modulators with both doping patterns are able to work at 10 Gbit/s with 0.5 V_{pp} driving voltage. We also reduce the size of ring modulator by utilizing an asymmetrical waveguide.

Keywords: modulator, carrier depletion, coplanar waveguide, ring resonator, Mach-Zehnder interferometer.

1. INTRODUCTION

Silicon carrier-depletion-based modulator has proven itself to be the most prevailing solution for optical modulation on silicon, owing to its advantages of high operation speed, CMOS compatibility and fabrication simplicity, which so far cannot be offered simultaneously by other competing modulation techniques on silicon. The potential of high operation speed of carrier-depletion-based modulator can be exploited by using a Mach-Zehnder interferometer incorporated with a travelling wave electrode. Operation speed of up to 50 Gbit/s has been demonstrated with this structure for applications such as high capacity long-haul optical communications [1] [2]. For applications like optical interconnect, the advanced CMOS circuit imposes a strict constraint on the driving voltage and power consumption. Ring resonator therefore is used to enhance the optical modulation with a driving voltage which is compatible with CMOS electronics [3]. The strong temperature dependence of silicon ring modulator can be hurdled by an integrated heater.

In this paper, we review the recent progress at photonics research group of Ghent university-imec on carrier-depletion-based silicon modulator. The two most prevalent doping patterns, *i.e.* the lateral and the interdigitated PN junctions are optimized to enhance the modulation efficiency. After that their performances are compared comprehensively, including modulation efficiency, insertion loss, and depletion capacitance. Based on such specific understanding about the characteristics of each doping pattern, we demonstrate a 40 Gbit/s MZ modulator as well as 10 Gbit/s low driving voltage ring modulators. Also an asymmetrical waveguide is utilized to reduce the radius of ring modulator which is surrounded by doped silicon as the integrated heater.

2. DIODE DESIGN, FABRICATION AND CHARACTERIZATION

A carrier-depletion-based optical modulator implies to embed a PN junction inside a silicon waveguide, and then manipulate the refractive index of the waveguide by reverse biasing the PN junction. Schematic diagrams of the lateral and the interdigitated PN junctions are shown in Figs. 1(a) and 1(b). The width and height of the rib waveguide accommodating the PN junctions are 500 nm and 220 nm respectively. The slab height of 150 nm is chosen in order to enable simple co-integration of the diode modulators with shallowly etched fiber grating couplers. The P-type and the N-type regions which form the PN junction have the same average doping concentration of 1×10^{18}/cm^3. The Ohmic contact regions which reside 1 μm away from two sidewalls of the rib are heavily doped to 1×10^{20}/cm^3.

The modulators were fabricated on a 200-mm SOI wafer with 2 μm buried oxide and 220 nm top c-Si layer. First, the shallow-etched structures like fiber grating couplers and phase shifters were defined by 193 nm lithography and 70 nm silicon dry etching. A second 193 nm lithography step followed by 220 nm silicon dry etching then defined the strip access waveguides. Next, a 10-nm oxide layer was thermally grown to prevent ion channeling during ion implantation. The boron and phosphorus implants were carried out using photoresist as the mask. Local implantation windows were opened in this resist mask using 248 nm lithography. The dopants were subsequently activated by rapid thermal annealing (RTA). The simulated phosphorus and boron distributions

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inside the waveguide after annealing are shown in Figs. 1(c) and 1(d), respectively. Subsequently, silicide ohmic contacts were selectively formed on the highly doped contact regions. This was followed by pre-metal dielectric deposition, contact holes patterning, tungsten filling and chemical mechanical polishing (CMP). Finally, the electrode was formed by a Cu-damascene process.
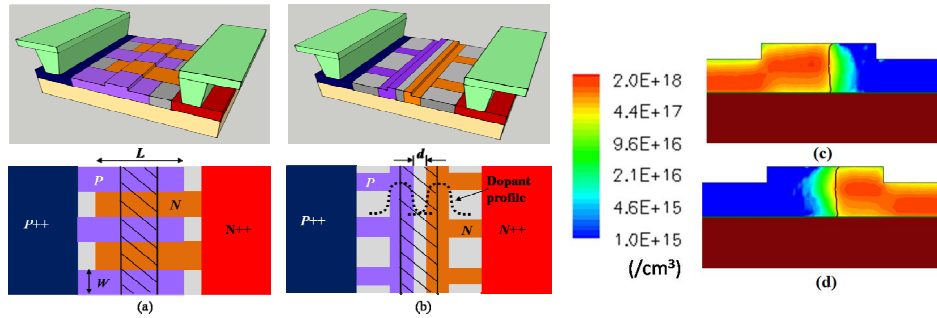

Figure 1. Schematic 3D diagrams and top views of the two doping patterns: (a) interdigitated PN junction; (b) lateral PN junction; (c) simulated phosphorus distribution inside the waveguide; (d) simulated boron distribution inside the waveguide. Shaded areas in top views mark positions of rib waveguides.
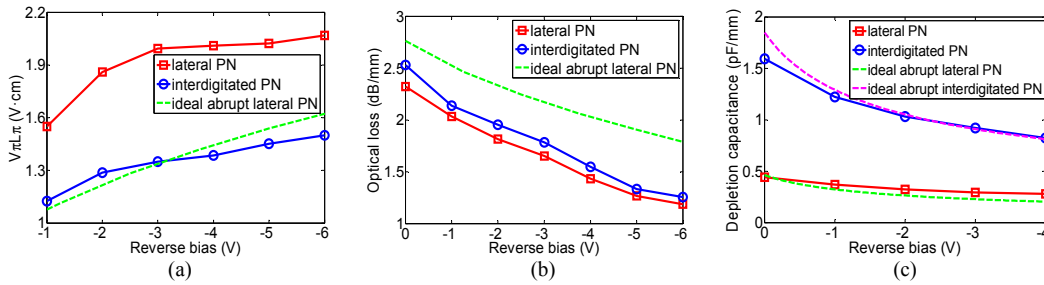

Figure 2. Measured and simulated $V_\pi L_\pi$ (a), propagation loss (b) and depletion capacitance (c) as a function of the reverse bias for the interdigitated and the lateral PN junctions. The doping concentration is $1 \times 10^{18}/cm^3$.

Geometries of interdigitated and lateral PN junctions are optimized in terms of enhancing the modulation efficiency. The modulation efficiency of interdigitated PN junction depends on the width W of interdigitated implantation windows and the overlap length L between two adjacent windows as shown in Fig. 1(a). L determines the overlap between the optical mode and the space charge region of each PN junction, while W determines the PN junction density along the beam propagation direction. Based on a trade-off between modulation efficiency, operation speed and linewidth limitation of 248 nm lithography, W and L were chosen to be 300 nm and 1.6 um respectively. For the lateral PN junction, the gap d between the N and the P implantation windows affects the gradient of the practical net dopant concentration. According to our simulation and measurement result [4][5], a gap of $d = 40$ nm induces the steepest PN junction, and therefore exhibits the highest modulation efficiency. The measured modulation efficiency $V_\pi L_\pi$, the propagation loss, and the depletion capacitance of the optimized lateral and interdigitated PN junctions are presented in Fig. 2 as a function of the reverse bias, the simulated performances of ideal abrupt PN junctions are displayed together as well.

Compared with the lateral PN junction, the capacitance of interdigitated PN junction is a factor 3.6 higher when the reverse bias is 0 V (1.59 nF/mm vs. 0.44 nF/mm). However, the modulation efficiency of the interdigitated PN junction is only 40% higher than that of the lateral diode (1.12 V·cm vs. 1.55 V·cm at -1 V). The reason is that the carrier depletion region of lateral PN junction overlaps better with the center of optical mode where any variation of carrier density can alter the mode refractive index more effectively. On the other hand, the lateral and the interdigitated PN junctions have very similar propagation loss (2. dB/mm vs. 2.5 dB/mm at 0 V). This implies the total insertion loss of the interdigitated PN junction based device is much less than that of the lateral PN junction based device, owing to the 40% improvement of the modulation efficiency and the resultant shorter device length of the former.

3. 40 GBIT/S MZ MODULATOR WITH TRAVELING WAVE ELECTRODE

The lumped electrode based MZ modulator is not suitable if the bit rate increases far beyond 10 Gbit/s due to the limitation of RC constant. To overcome this limitation, a travelling wave electrode is utilized to enable 40 Gbit/s modulation. Figures 3(a) and 3(b) show the microscope image and the schematic cross section of the coplanar waveguide (CPW) used to drive the MZ modulator. The operation speed of a modulator with a travelling wave electrode is determined by 3 factors: the velocity matching between the microwave and the optical carrier, the impedance matching and the low microwave attenuation. To fulfil these requirements, a specific transmission

line calculation is essential for high speed modulation. We develop an analytical equivalent circuit model for the coplanar waveguide in Fig. 3(b) [6]. The model is depicted in Fig. 3(c). Conformal mapping and partial capacitance techniques are employed to calculate each element in this circuit. In contrast to the numeric simulation, the model allows us to do a fast and accurate RF calculation together with a clear physical insight to the propagation behavior of RF signal. Based on the model and the travelling wave modulation theory, we optimize the CPW for maximum 3dB modulation bandwidth. According to the calculation, the width of the central signal metal is set to 6 μm, and the gap between the central metal and two grounds is 3.5 μm.
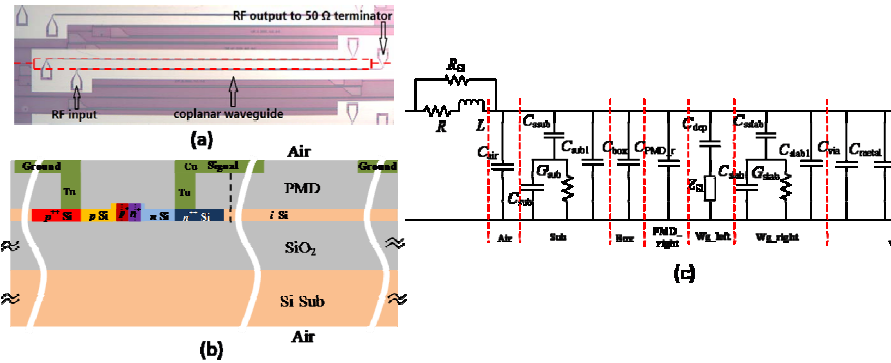

Figure 3. Microscope image (a) and schematic cross section (b) of coplanar waveguide used to drive the carrier-depletion based modulator. (c) an equivalent circuit model of the transmission line shown in (a) and (b).
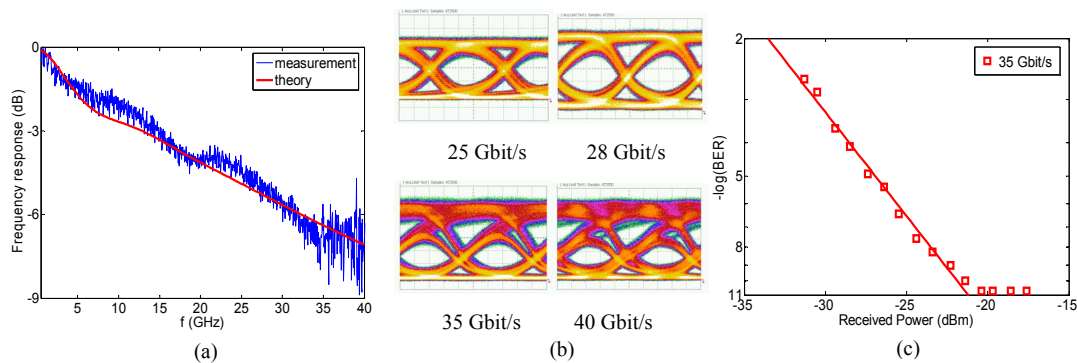

Figure 4. EO frequency response (a), eye diagrams (b), and bit error rate (c) of a 3 mm lateral PN junction which is driven by a CPW. The reverse bias in (a) is -4 V. The peak to peak voltage of the 2^7-1 PRBS signal reaching the input port of CPW is around 5 V_{pp} in (b) and (c). The output port of CPW is terminated with a 50 Ω load for all measurements.

Our calculation indicates that for our MZ modulators whose phase shifters are 3 mm, the microwave attenuation emerges as the major speed limitation factor. As aforementioned in section 2, the capacitance of interdigitated PN junction is 3.6 times as high as that of the lateral PN junction. This will induces a large shunt admittance between the signal electrode and the ground, which therefore increases the axial current running along the electrode as well as the conductor loss. For example, the RF propagation losses of the lateral PN junction and the interdigitated PN junction embedded CPWs at 15 Gbit/s are calculated to be 2.6 dB/mm and 5.4 dB/mm respectively. As such, the lateral PN junction is superior to the interdigitated PN junction for modulation speed beyond 10 Gbit/s. This is confirmed by our measurement result: a lateral PN junction of 3 mm driven by the optimized CPW supports a bit rate of up to 40 Gbit/s; in contrast the operation speed of a 3 mm interdigitated PN junction with the same CPW is far below 25 Gbit/s, which is the bottom limit of our measurement system.

The dynamic measurement results of the 3 mm lateral PN junction with CPW are shown in Fig. 4. Figure 4(a) shows the measured EO frequency response agrees quite well with the prediction of the equivalent circuit model. The measured 3 dB optical modulation bandwidth is 15 GHz at -4 V. Error free operation is realized at 35 Gbit/s in Fig. 4(c). The extinction ratio at this bit rate is 11.3 dB.

4. 10 GBIT/S LOW-VOLTAGE LOW-LOSS RING MODULATORS

Key requirements for the modulator in optical interconnects are high extinction ratio, low insertion loss, high modulation speed and low energy per bit. A ring modulator whose spectrum is sensitive to any small variation of refractive index is applicable for this job. Both doping patterns shown in Fig. 1 are embedded into a ring of 40 μm radius. Measured transmission spectra of the lateral and the interdigitated PN junctions based rings are shown in Figs. 5(a) and 5(b) with different biases. The experimental quality factors Q at 0 V were 15400 and

18700 for the lateral and the interdigitated diodes respectively. Figure 5(c) shows the resonance wavelength shift of the two diodes versus the applied bias, where the modulation efficiencies are 22 pm/V and 30 pm/V for the lateral and the interdigitated PN junctions, respectively. It can be deduced that with a static voltage swing from 0.5 V to -0.5 V, the maximum DC extinction ratios are 18.5 dB and 29 dB for the lateral and the interdigitated PN junctions based modulators, while the corresponding insertion losses are 7.9 dB and 4.8 dB respectively.
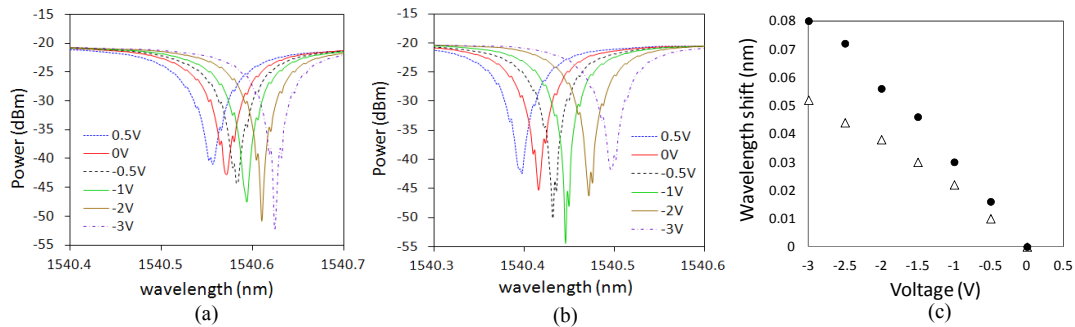

Figure 5. Measured transmitted power versus wavelength of the lateral (a) and the interdigitated (b) PN junctions based ring modulators with different applied biases. (c) resonance wavelength shift as a function of reverse bias for both lateral and interdigitated diodes.
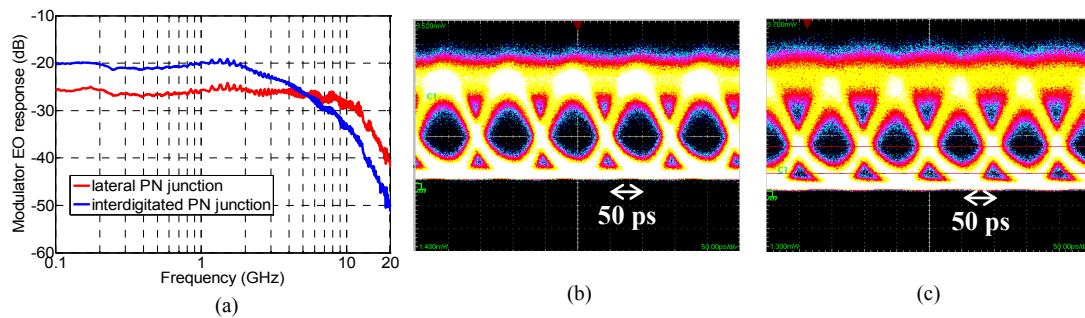

Figure 6. Dynamic measurement result of the ring modulators with lateral and interdigitated PN junctions: (a) EO frequency response at 0V reverse bias. (b) Eye diagram of the lateral PN junction based ring modulator. (b) Eye diagram of the interdigitated PN junction based ring modulator. Peak to Peak voltage of the 10 Gbit/s PRBS signal $(2^{15}-1)$ is 0.5 V_{pp}.

Figure 6(a) shows the frequency responses of the ring modulators. The electrical 3 dB bandwidth of the lateral PN junction based ring is 11 GHz, which is limited by both RC constant and photon life time. In contrast the 3.8 GHz bandwidth of the interdigitated PN junction based ring is mainly limited by its RC constant, owing to its large capacitance. The high Q values of both rings enable them to operate with a 0.5 V_{pp} PRBS driving signal at 10 Gbit/s as shown in Figs. 6(b) and 6(c). Because of a superposition between the input and the reflected RF signals, the practical voltage swing applied on the PN junctions would be 1 time higher (1 V). The extinction ratios are 9.1 dB and 9.7 dB in Figs. 6(b) and 6(c) respectively.

5. COMPACT RING MODULATORS WITH INTEGRATED HEATER

The ring modulator benefits from reducing its bending radius, since the depletion capacitance is proportional to the radius. A small capacitance is always desirable for obtaining high modulation bandwidth and low power consumption. However, due to the 70 nm etching depth as aforementioned in section 2 and the consequent weak lateral confinement to the optical field, the ring modulators in section 4 have a radius of 40 µm so as to avoid too much bending loss. One way to cut the radius without increasing the bending loss is to increase the etching depth of the ring. However, introducing a new etching depth requires additional lithography and etching steps. In order to implement a compact ring modulator with 70 nm etching depth, we have designed and fabricated a ring based on an asymmetrical waveguide as shown in Fig. 7(a). The outer side of the ring is completely etched in order to enable a small bending radius, while the inner side is etched by 70 nm to allow electrical paths from the P and N regions to corresponding contacts. The particular doping pattern in Fig .7(a) allows both P+ and N+ contacts to locate at the same side of the waveguide. Another benefit of this structure is that the integrated heater can be implemented by doped silicon or silicide surrounding the ring, without adding any additional steps in the processing flow.
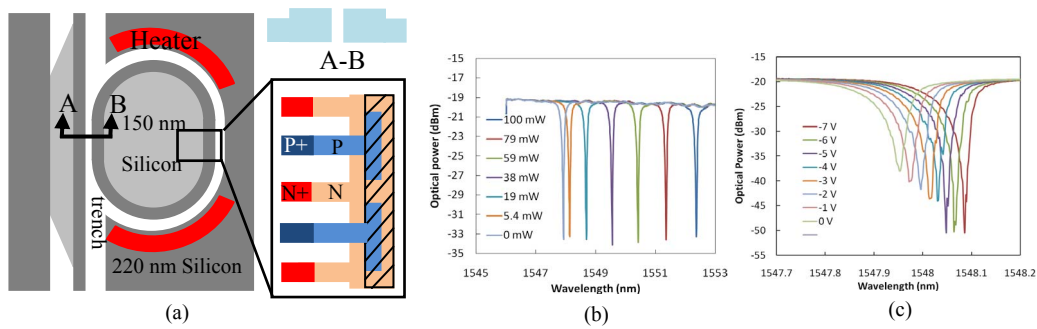
Figure 7: (a) schematic top view of the asymmetrical waveguide based ring modulator with integrated heater; (b) transmission spectra with different heater powers; (c) transmission spectra with different reverse biases

A radius of 10 μm is implemented in this study, while the straight section length of the racetrack ring is 11 μm. Figures 7(b) and 7(c) show the spectra of this ring modulator for different heater powers and reverse biases respectively. The Q value and FSR of this ring are 13600 and 7.3 nm respectively. It can be deduced from Figs. 7(b) and 7(c) that the modulation efficiency is 21 pm/V, which is comparable with that of the lateral PN junction based ring modulator; on the other hand, the tuning efficiency of the heater is 42 pm/mW. In Fig. 8 we carry out the eye diagram measurement at different wavelengths by changing the heater power. We can see that there is no notable degradation of the modulation quality while the operation wavelength is tuned within a range more than a half of FSR.
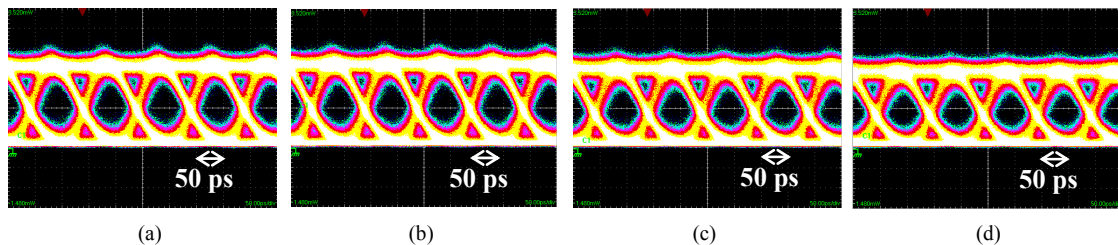

Figure 8. Eye diagrams of asymmetrical waveguide based ring modulator with different heater power. The heater power, extinction ratio, operation wavelength and quality factor of the eye are: (a) 0 mW, 10.08 dB, 1548.134 nm and 7.37; (b) 39.4 mW, 10.01 dB, 1549.825 nm and 7.16; (c) 59.5 mW,10.05 dB, 1550.751 nm and 7.01; (d) 100 mW,9.87 dB, 1552.715 nm and 6.77. The V_{pp} of the 10 Gbit/s PRBS signal (2^{31}-1) is 2 V. A DC voltage of -2.5 V is applied to make sure the diode is always reverse biased during the modulation.

6. CONCLUSIONS

Silicon carrier-depletion-based modulators have been demonstrated for different applications by choosing proper doping pattern, waveguide configuration and electrode, including 40 Gbit/s MZ modulator suitable for optical telecommunication, ring modulators of 0.5 V_{pp} driving voltage for optical interconnect. A 10Gbit/s compact ring modulator based on an asymmetrical waveguide with integrated heater is demonstrated as well.

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