CMOS-compatible Tungsten Heaters for Silicon Photonic Waveguides

A. Masood[1], M. Pantouvaki[2], D. Goossens[2], G. Lepage[2], P. Verheyen[2], D. Van Thourhout[1], P. Absil[2], W. Bogaerts[1]

[1] Photonics Research Group (INTEC), Ghent University - imec, Department of Information Technology, Center for Nano and Biophotonics (NB Photonics), Sint-Pietersnieuwstraat 41, B-9000 Ghent, Belgium

[2]imec vzw, Kapeldreef 75, B-3001 Leuven, Belgium

Email: Adil.Masood@intec.UGent.be

***Abstract* –We present a Tungsten thermo-optic tuner on SOI, using standard CMOS back-end fabrication processes. Tuning efficiency of 35.2mW/FSR was achieved on ring resonators with 10%-90% heating time of 2.8µs.**

Keywords – Silicon photonics, thermo-optic tuning, CMOS, Integration

I. Introduction

Recent advances in silicon and silicon compatible photonics, passive as well as active, have stimulated prospects of high density integration of photonic and electronic components [1]. Manufacturing of silicon photonics on the same platform as complementary metal-oxide-semiconductor (CMOS) electronics provides a route to high-volume markets [2][3].

Silicon's high thermo-optic coefficient ($1.86 \times 10^{-4}K^{-1}$) makes silicon photonic extremely sensitive to temperature variations [4]. While this is a liability when it comes to robustness against external changes, this high thermal sensitivity can also be exploited to tune wavelength selective filters for WDM [5]. Integrated heaters based on Joule's heating are widely used for this purpose. Different components are used as heating elements in thermo-optical tuning like thin film metal lines, metal-silicides and ion-implanted silicon lines [6][7][8].

For a truly CMOS compatible scheme for heaters, at least following criteria should be met: (a) Heater fabrication should not impact, or demand changes, in photonics front-end (waveguide based components) fabrication so that photonics stays optimized; (b) Fabrication processes should be as similar as possible to CMOS back-end (contact via, metal interconnects etc.) processing, so that development cost is minimized; and (c) Fabricated heaters should allow successive processing of CMOS standard back-end metallization so that integration and packaging feasibility remains high.

In this paper, we present a fabrication scheme and characterization results for CMOS compatible tungsten heaters that meet the above defined criteria.

II. Material & Design

To ensure the highest degree of compatibility with CMOS, the choice of material to be used as heater was reduced to conductive materials used in CMOS devices. Since tungsten is typically used for contacts, and it has suitable electrical and thermal characteristics, we implemented the heaters in this material. As a test vehicle for the tungsten heaters we chose ring elongated resonators, as they are compact and easy to characterize. The heaters were co-fabricated with carrier depletion modulators [9], which included tungsten contacts as well as copper metal interconnects (metal 1). The fabrication of the heaters was included in the processing flow after metallization of the tungsten contacts and before deposition of the stack for metal 1. This allows flexibility to insert or remove heater fabrication module between tungsten contacts and metal 1 (Figure 1).

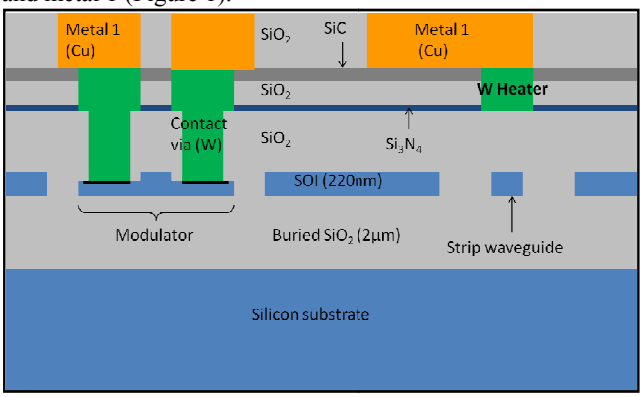

Figure 1: Device stack showing W contact via for modulators and W heater

The choice of the dielectric on top of the photonic structures was made on the basis of optical performance. Waveguides with different silica glass cladding were measured and a low-loss silica glass was chosen, after verifying that the standard dielectric etch processes remain the same [10].

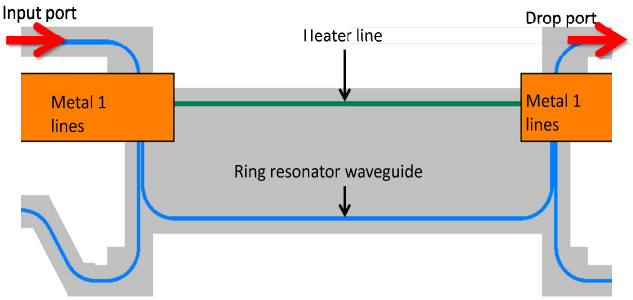

Figure 2: Design layout of heater on top of micro-ring

Device design was kept simple to facilitate benchmarking (Figure 2). Racetrack type micro-rings with free spectral range (FSR) of ~3.5nm were used as optical devices. The heater lines were 600nm wide and 420nm thick. They were positioned directly on top of one of its longer sides as a straight metal line.

The tungsten heater line was contacted at both ends by Cu metal lines which led to probing pads.

III. FABRICATION

Complete fabrication took place at the 200mm CMOS pilot line of imec (Leuven, Belgium). The photonic 'front-end' was fabricated on 200mm Silicon-on-Insulator (SOI) wafers (220nm crystalline silicon on top of 2µm buried oxide and substrate).

A. Front-end and contact modules

Standard processing modules from imec's Silicon-Photonics Platform (iSiPP), which include 193nm lithography and inductive coupled plasma reactive ion etch, were used for fabricating waveguide and grating couplers [11]. Ion implants and Nickel-silicidation (NiSi) were based on standard CMOS modules. After the front-end, a blanket layer of SiO_2 was deposited using chemical vapor deposition method. Dielectric planarization was done using a timed chemical-mechanical polishing (CMP). Holes for contact were etched by capacitively coupled plasma reactive ion etch (CCP-RIE) stopping on the NiSi (Figure 3a) and filled using standard CMOS Ti/TiN/W contact metallization processes. The excessive W, Ti and TiN were planarized using metal CMP (Figure 3b).

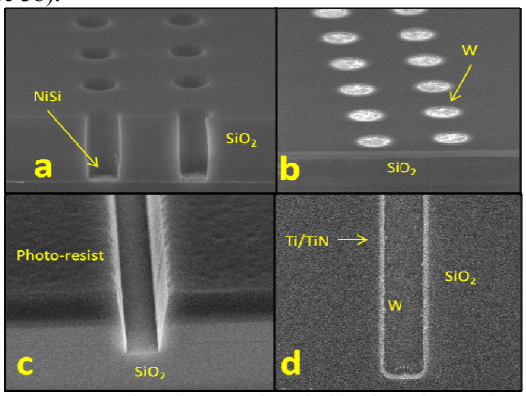

Figure 3: (a) Cross-section of contact via etched in SiO2; (b) Top-down view of W filled/polished contact via; (c) Cross-section of etched heater trenches in SiO2 (with photo-resist); (d) Top-down view of W filled heater lines.

B. Heater module

For heater fabrication, a stack of Si_3N_4, SiO_2 and SiC was deposited. The purpose of Si_3N_4 is to act as an etch stop for heater etch while the SiC acts as a CMP stop for the heaters. Similar to the contact via module, 248nm lithography is performed to pattern heater layer, followed by CCP-RIE etch in two steps: to etch SiC, and then to etch SiO_2, which stops by opening Si_3N_4 (Figure 3c). For heater metallization, similar processes as for the contact module were used. CMP removed excess W and planarized the top surface, making it ready for back-end metallization (Figure 3d).

C. Back-end Metallization

Typical CMOS uses many layers of Copper (Cu) or Aluminum (Al) based metallization [12]. In our case, we required only a single metal layer, which was formed using standard Cu damascene processes for 130nm CMOS technology. After the metallization, we applied a thin layer of SiC as a passivation layer to prevent Cu oxidation.

IV. CHARACTERIZATION

The tungsten heaters were characterized in voltage-driven mode. Light was coupled in using vertical grating based fiber couplers through a tunable laser. The drop port output was connected to an optical power-meter. The voltage was increased in steps of 0.5V and the wavelength was swept for each step in the range 1465nm – 1565nm. The output spectrum corresponded to the drop port spectrum of a micro-ring resonator with peaks at different wavelengths separated by the FSR of the ring. Upon application of voltage on the heaters, the peak wavelengths showed a shift towards longer wavelengths the peak wavelength shift as percentage of FSR for different powers is shown in Figure 4.

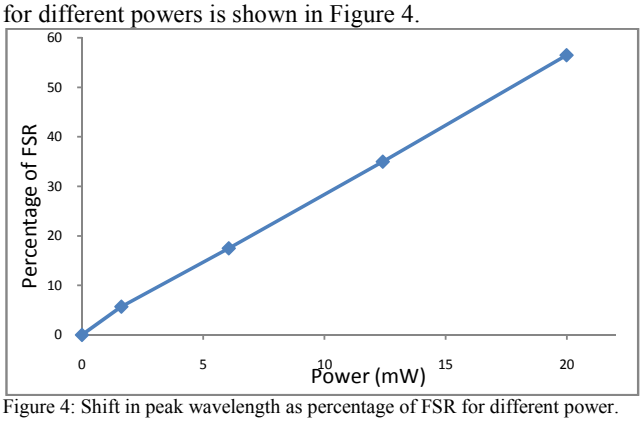

Figure 4: Shift in peak wavelength as percentage of FSR for different power.

The linearity in the graph is expected as the temperature rises linearly due to Joule heating. 100% of the FSR shift (corresponding to a phase shift of 2π) is achieved for 35.2mW. Compared to other similar heater approaches (metal line on top of waveguide), this efficiency corresponds to the state-of-the-art [6][13][14][15]. However, similar heater has been demonstrated with as low efficiency as 2.4mW per FSR shift using isolation trenches etched around waveguide for enhanced heat confinement [16].

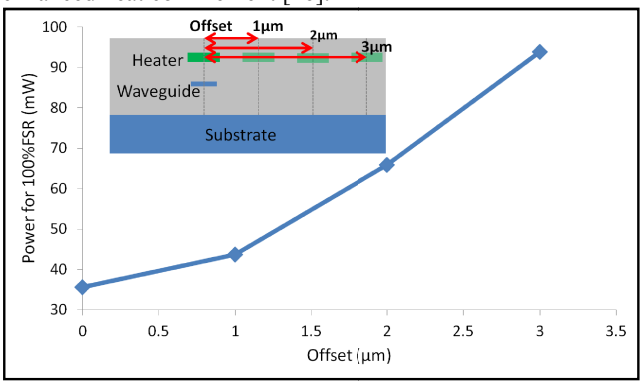

Figure 5: Power corresponding to 100% FSR shift for heater offset from waveguide.

Figure 5 shows change in power needed for 100% FSR shift with offset of heater position in relation to waveguide. Power requirement increases rapidly as heater moves away from heater.

For devices requiring rapid phase tuning, heating and cooling time of waveguide is important. This switching speed can be measured by comparing optical response of the filters with change in electrical power. The optical wavelength was tuned to a resonance peak (maximum output) when no voltage was applied. 1V DC application shifted the peak wavelength to roughly 50% of FSR, showing maximum drop in optical power from drop port.

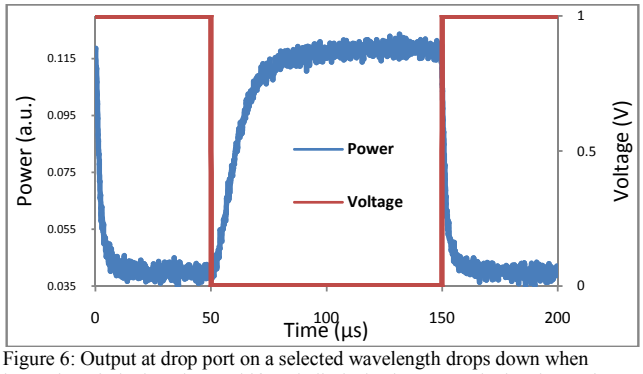

Figure 6: Output at drop port on a selected wavelength drops down when heater is switched on due to shift and climbs back to normal when heater is switched off.

The heater was connected to a function generator supplying block-wave voltages across the heater with duration of 100µs for 0V and 50µs for 1V. This resulted in a drop and rise in the optical output as shown in Figure 7. From recorded graphs, the heating time for 10%-90% was estimated to be 2.8µs and the cooling time was estimated to be 30.2µs.

V. CONCLUSIONS

We have demonstrated the implementation of tungsten heaters for thermo-optic tuning of silicon waveguides for the first time. The integration of tungsten heaters was fully compatible with CMOS processing. This approach demonstrates that standard off-the-shelf CMOS processes can be used to perform highly compatible large volume production of thermal phase tuners on SOI based WDM filters. The efficiency can be further improved by further optimizing thickness and choice of overlay stack by investigating other CMOS compatible dielectrics or by implementing trench isolation to enhance heat confinement.

ACKNOWLEDGMENT

Authors would like to acknowledge imec's 200mm p-line for the processing and towards Karel Van Acoleyen for his help in setting up characterization of devices.

REFERENCES

[1]. M. Lipson, "Silicon photonics: the optical spice rack", *Electronics Letters*, Volume: 45, Issue: 12, pp. 576 – 578 , 2009.

[2]. P. Dumon, W. Bogaerts, R. Baets, J – M Fedeli, L. Fulbert, "Towards foundry approach for silicon photonics: silicon photonics platform ePIXfab", *Electronics Letters*, Volume: 45, Issue: 12, pp. 581 – 582, 2009.

[3]. L. Tsybeskov, D.J. Lockwood, M. Ichikawa, "Silicon Photonics: CMOS Going Optical", *Proceedings of the IEEE*, Volume: 97, Issue: 7, pp. 1161 – 1165, July 2009.

[4]. G. Cocorullo, "Thermo-optical modulation at 1.5mu in silicon etalon", *Electronics Letters*, Volume: 28, Issue: 1, pp. 83 – 85, January, 1992.

[5]. W. Bogaerts, S.K. Selvaraja, P. Dumon, J. Brouckaert, K. De Vos, D. Van Thourhout, R. Baets, "Silicon-on-Insulator Spectral Filters Fabricated With CMOS Technology", *IEEE Journal of Selected Topics in Quantum Electronics*, Volume: 16, Issue: 1, pp. 33 – 44, January-February, 2010.

[6]. F. Gan, T. Barwicz, M. A. Popovic, M. S. Dahlem, C. W. Holzwarth, P. T. Rakich, H. I. Smith, E. P. Ippen, and F. X. Kartner, "Maximizing the thermo-optic tuning range of silicon photonic structures," *Photonics in Switching* (2007), pp. 67 – 68, 2007.

[7]. J. V. Campenhout, W. M. J. Green, S. Assefa, Y. A. Vlasov, " Integrated NiSi waveguide heaters for CMOS-compatible silicon thermo-optic devices" *Optics Letters*, Volume: 35, Issue: 7, pp. 1013 – 1015, 2010

[8]. J. Song, Q. Fang, T. Liow, H. Cai, M. Yu, G. Lo, and D. Kwong, "High Efficiency Optical Switches with Heater-on-Slab (HoS) Structures", *Optical Fiber Communication Conference* (2011), pp. 1 -3, March 2011.

[9]. H. Yu, et al, "Doping Geometries for 40G Carrier-Depletion-Based Silicon Optical Modulators", *Optical Fiber Communication Conference (OFC)*, Los Angeles, United States, March 4, 2012.

[10]. A. Masood, W. Bogaerts, J. Van Olmen, J. Van Aelst, D. Van Thourhout, D. Sabuncuolu Tezcan, "Photonics-CMOS 3D integration: copper through-silicon-via approach", *Proceedings of the 2009 Annual Symposium of the IEEE Photonics Benelux Chapter*, Belgium, p.165-168, 2009

[11]. S. K. Selvaraja, P. Jaenen, W. Bogaerts, D. Van Thourhout, P. Dumon, R. Baets, "Fabrication of Photonic Wire and Crystal Circuits in Silicon-on-Insulator Using 193-nm Optical Lithography", *Journal of Lightwave Technology*, Volume: 27, Issue: 18, pp. 4076-4083, 2009.

[12]. M. Quirk, J. Serda, *Semiconductor Manufacturing Technology*, Prentice-Hall, 2001.

[13]. M. Geng, L. Jia, L. Zhang, L. Yang, P. Chen, T. Wang, and Y. Liu, "Four-channel reconfigurable optical add- drop multiplexer based on photonic wire waveguide", *Optics Express*, Volume: 17, Issue: 7, pp. 5502–5516, 2009.

[14]. P. Dong, W. Qian, H. Liang, R. Shafiiha, N.-N. Feng, D. Feng, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low power and compact reconfigurable multiplexing devices based on silicon microring resonators", *Optics Express*, Volume: 18, Issue: 10, pp. 9852 – 9858, 2010

[15]. M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, and R. W. Young, "Adiabatic Resonant Microrings (ARMs) with directly integrated thermal microphotonics," *Proceedings of Conference on Quantum electronics and Laser Science Conference* CLEO/QELS 2009, pp. 1 – 2, 2009

[16]. Dong, Po; Qian, Wei; Liang, Hong; Shafiiha, Roshanak; Feng, Dazeng; Li, Guoliang; Cunningham, John E; Krishnamoorthy, Ashok V; Asghari, Mehdi, "Thermally tunable silicon racetrack resonators with ultralow tuning power", *Optics Express*, Volume 18, Issue 19, pp. 20298 – 20304, 2010