The BOOM Project: Towards 160 Gb/s Packet Switching Using SOI Photonic Integrated Circuits and Hybrid Integrated Optical Flip-Flops

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***Abstract*—We present a 160 Gb/s optical packet switching architecture that performs label detection and packet wavelength conversion using photonic components integrated on silicon-on-insulator (SOI) waveguide boards. For label detection, we report the fabrication of a 4-channel tunable, second-order microring resonator demultiplexer using the SOI nanowire waveguide platform. For all-optical wavelength conversion we report the integration and packaging of a cascaded SOI delay interferometer (DI) structure using SOI rib waveguides. Both components were assembled with an optical flip-flop to enable 160 Gb/s optical packet switching. The power penalty after the wavelength conversion process was $\sim$4.5 dB with error performance well above the FEC limit. This work is part of the European ICT-BOOM project which aims at building a Tb/s photonic router using hybrid and heterogeneous integration on SOI substrates. The preliminary results reported here is the initial step before the final project demonstrator.**

***Index Terms*—All-optical signal processing, all-optical wavelength converter (AOWC), all-optical wavelength routing, hybrid photonic integration, microring resonator, optical flip-flop, optical packet switching, silicon-on-insulator (SOI).**

I. Introduction

THE growing demand for bandwidth hungry internet applications is stressing the available capacity and performance of optical core networks [1]. Network operators are responding with the expansion of their electronic infrastructure and the deployment of new transmission and switching equipment. However, size, power consumption, heat-dissipation and inter-connectivity of the increasing number of racks of equipment raise concerns for the configuration and practical operation of modern central offices [2]. Looking ahead, future optical packet routers that can offer a high degree of capacity inside compact, cost-effective, and energy-efficient photonic structures are being researched worldwide [3]. The tool for the realization of miniaturized photonic system architectures is the dense functional photonic integration using either InP or silicon waveguide substrates [4], [5].

Monolithic InP integration has been dominant in the fabrication of photonic integrated circuits (PICs) for signal processing such as all-optical wavelength converters (AOWCs) and multi-port optical switches [6], [7]. With the continuous progress of photonic integration, the assembly of the InP chips with passive silicon or silica waveguide circuits has become feasible, realizing even more demanding functionalities such as optical packet synchronization and buffering [8]. Now the new trend is to bring both InP and silicon components on the same integration platform in order to address loss-coupling issues and obtain functional PICs with optimum yield management and InP utilization. In this context new power-efficient component designs [9] and new optical routing components based on the hybrid silicon photonic platform [4] are now being attempted combining both the processing speed of InP and the cost-effective silicon fabrication.

The European BOOM project attempts the development of a photonic routing platform relying on hybrid silicon-on-insulator (SOI) integrated PICs to implement all the routing functionalities; label detection, control signal generation, wavelength conversion (WC) and wavelength switching. Packet synchronization can be implemented using optical buffers based on delay lines [10] or micro-resonator assisted components [11]. Hybridization is performed through flip-chip bonding and heterogeneous wafer scale integration techniques which enable the realization of components such as ultra-fast all-optical wavelength converters, electroabsorption-modulated lasers (EMLs), WDM photo-detectors and microring resonator (MRR) based cross-connects on silicon substrates. At the moment these devices are in the process of development but the first packaged SOI structures have been designed, fabricated and are available for the first system-level, proof-of-concept tests at speeds exceeding 100 Gb/s.

In this paper we present an optical circuit that can perform 160 Gb/s packet switching employing a second-order SOI

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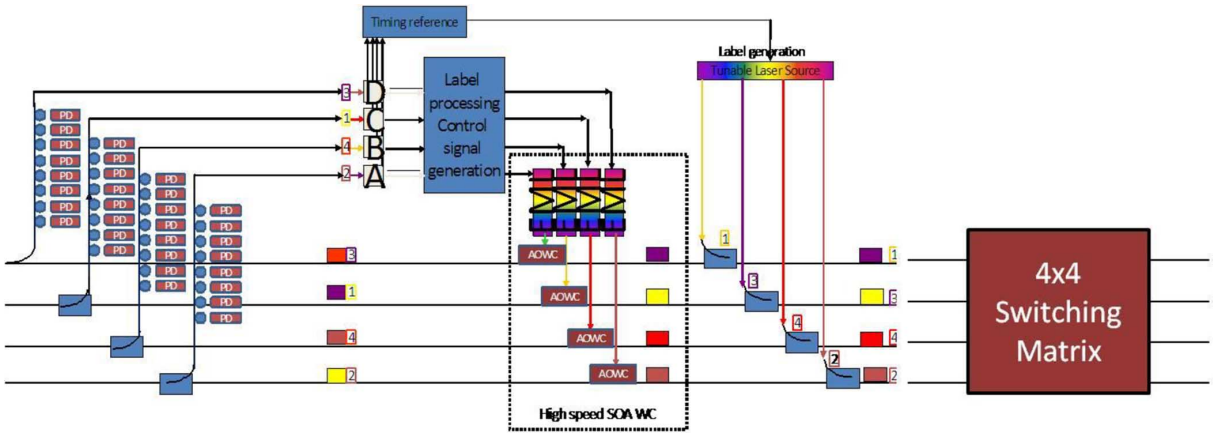

Fig. 1. BOOM routing architecture.

nanowire microring resonator for label extraction, and a SOI delay interferometer (DI) chip for high-speed wavelength conversion. We demonstrate CMOS-compatible fabrication of a fully tunable 4-channel microring resonator demultiplexer for label extraction and the fabrication of the SOI-DI on a 4 μm SOI rib substrate. We present the packaging and pigtailing of the SOI-DI chip using the generic Optocap bathtub package which has configurable end-wall options, covering multi-fiber as well as electrical supply requirements. On the system-level, all-optical routing is assisted using a hybrid integrated optical flip-flop (OFF) for control signal generation. The optical components were assembled to realize 160 Gb/s optical packet switching with 4.5 dB power penalty and error performance well above the FEC limit.

II. BOOM Photonic Routing Concept

Fig. 1 depicts the BOOM photonic routing architecture with synchronized labeled packets entering at different wavelengths. Payloads have an on-off-keying packet format and carry data rates up to 160 Gb/s. Labels on the other hand are NRZ optical pulses with duration of a few nanoseconds. The switching process starts with packets arriving at the node at predefined time-slots and three sub-systems are employed for routing the packets. The first performs label detection through ultra-dense wavelength division (UDWDM) demultiplexers that filter out the optical labels. The UDWDM demultiplexer comprises compact MRR and arrays of integrated detectors fabricated on silicon-on-insulator through die-to wafer bonding techniques. The generated electrical signals are subsequently delivered for further electronic processing. The electronic processor—which can be typically a FPGA—generates the control signal that gates the all-optical wavelength conversion subsystem. The latter includes EMLs and high-speed AOWCs flip-chip integrated on the same SOI platform. The EMLs have the DFB and electro-absorption (EAM) section and by gating the EAM, E/O conversion of the control signal is accomplished. The optical control signals are subsequently used to feed the integrated hybrid wavelength converters changing the wavelengths of the incoming data packets and assisting the wavelength routing process. The ultra-fast AOWCs consist of InP semiconductor optical amplifiers (SOAs) and a pair of cascaded SOI DIs. The SOAs serve for cross gain and phase modulation while the cascaded interferometers for chirp filtering and polarity inversion respectively. This type of wavelength conversion has been demonstrated with discrete element components for data rates beyond 160 Gb/s [12]. The wavelength routing process is performed with a 4×4 wavelength-based cross connect with 2-D grids of SOI MRRs [13], [14]. According to the wavelength of the labels, a different group of photodetector, EML and wavelength converter is enabled changing the color of the initial packet streams. The wavelength converted packets enter the 4×4 switching matrix and are routed to specific outputs according to their new wavelength color. The 4×4 switching matrix can be fabricated using waveguide substrates reported with waveguide loss as low as 0.7 dB/m minimizing the matrix loss [22]. Packet routing configurability can be performed using the integrated heating elements on top of the ring-based switching matrix. The whole routing system can support 160 Gb/s line rates with power consumption mainly determined by the wavelength conversion stages. Table I outlines the BOOM silicon technology compared to current state-of-the-art.

TABLE I
BOOM Technology/State-of-the-Art

Specs \ Structure	*AOWC*	*EML on SOI*	*SOI DWDM*
Bit rate (Gb/s)	160/40	10/-	10/-
Footprint (mm2)	100/870	µm range/-	µm range /-
Power consump. (W)	2.5/12	0.3/-	mW range/-

III. All-Optical Routing

The BOOM wavelength-routing silicon platform requires a list of hybrid components for its assembly and evaluation. Most of these elements are under the final fabrication stage and optimization. Given however the availability of a variety of passive structures which can be easily interconnected with commercial active elements, it would be possible to design a slightly modified routing architecture, relying on all-optical signal processing of labels and data packets. Fig. 2 shows the all-optical circuit that performs packet switching with MRRs, all-optical flip/flops and ultra-fast wavelength converters. The process

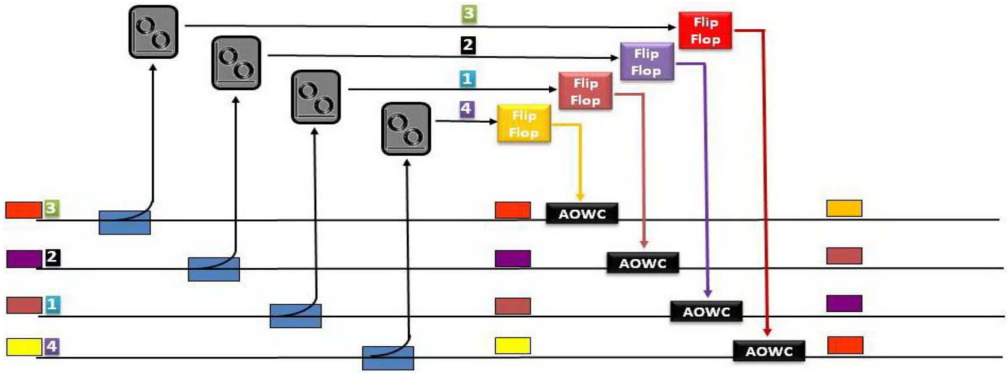

Fig. 2. All-optical routing concept.

starts with synchronized labeled data packets entering at different wavelengths and forwarded to three sequential subsystem units. The first undertakes the label detection and extraction operation using second-order SOI MRRs with very sharp-narrow filter responses and integrated heating elements for wavelength fine-tuning. The second unit receives the extracted headers and gates by means of optical triggering hybrid optical flip-flops. Here the flip-flops rely on coupled, SOA-MZI structures whose ON-OFF state is determined by the header set-reset pulses. Alternatively these flip-flops can also be implemented using the SOI nanowire platform [15]. According to the time-difference of set and reset pulses, continuous wave packets are generated at the outputs of the flip/flops with duration comparable to the data packet lengths. These signals are used subsequently as feed to high-speed AOWCs for wavelength conversion and routing. The wavelength conversion system comprises a commercially available SOA with 18 ps 90%–10% recovery time and a SOI packaged motherboard with two concatenated delay interferometers. The SOA is utilized for cross -gain and -phase modulation while the cascaded interferometers for chirp filtering and polarity inversion. Heating elements have also been incorporated in the SOI board for wavelength fine-tuning. The present AOWC configuration has been attempted in the past with chips on alignment station but never with a compact module. Currently, a pigtailed and packaged passive device has been developed in the BOOM project with good optical properties such as low insertion loss and high extinction ratio filter characteristics. The reconfigurable properties can be retrieved from Fig. 2, where packets enter the system at specific λ s and according to the labels they carry, different flip-flops are enabled generating CWs for subsequent wavelength conversion. Provided that the SOA has a 40 nm gain profile and in this spectrum the packaged module has a periodic tunable filter comb, λ-conversion is feasible with parallel AOWC configuration.

IV. Devices

A. Packaged SOI Double DI for All-Optical Wavelength Conversion

The fabrication of high-performance PICs on silicon requires an optical board technology capable to offer low waveguide losses, high fiber-to-waveguide coupling efficiency and optimum on-chip coupling. For optical signal processing devices,

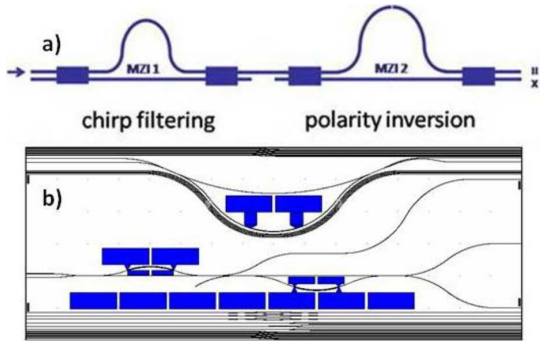

Fig. 3. (a) MZI cascaded structure for chirp filtering and polarity inversion. (b) SOI passive structure mask design.

this is ensured through efficient photonic pigtailing and packaging approaches based on sub-micron stepper motors. The BOOM project relies on the 4 μm SOI PLC technology for the fabrication of ultra-fast all-optical wavelength converters. The technology offers insertion losses <0.5 dB/coupling facet, low waveguide losses ($\sim$0.1 dB/cm) and excellent mode matching between 4 μm waveguides and commercially available lensed fibers. Single mode rib waveguides are used for guiding the light. A typical single-mode rib waveguide features a rib height (h) of 2 μm, a rib width (W) of 3.2 μm and a silicon height (H) above the buried oxide (BOX) of 4 μm. The BOOM ultra-fast AOWC concept is based on the chirp filtering technique. The scheme requires a single SOA, and two cascaded DIs as depicted in Fig. 3(a). The SOA is used for the non-linear processes: it induces chirp in the converted probe signal due to the refractive index modulation caused by a pulsed pump signal. The first SOI-DI filter is slightly detuned with respect to the probe wavelength and by filtering the blue (fast) chirp the acceleration of the effective recovery time of the system is achieved. The second SOI-DI filter is employed to restore the polarity of the optical pulses. Given the periodicity appeared on this comb-like filter structure, a high-speed optical packet injected in this AOWC can be converted on any of the CW wavelengths that coincide at a specific peak of the periodic response. Fig. 3(b) illustrates the mask design of the SOI passive structure.

Within BOOM project a SOI structure with concatenated DIs has been recently fabricated and packaged. The packaging procedure required a bathtub package with application specific end

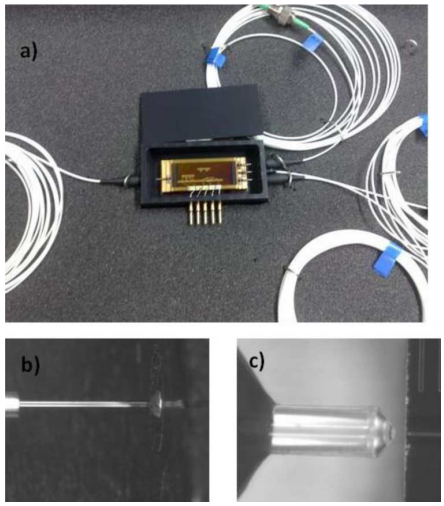

Fig. 4. (a) Packaged device. (b) Fiber through side wall. (c) Lensed fiber aligned and glued.

blanks, covering single and multiple fibre feedthroughs as well as electrical interconnects. In the present design a 1-in 3-out package with electrical option has been utilized. In terms of pigtailing, the most significant challenge of 4 μm waveguide SOI technology is spot-size. Typical mode diameters are around 4μm. Lateral tapering reduces coupling loss to standard SMF to approximately 3 dB. To achieve lower insertion loss, the use of fiber tapers is required. Although this may reduce insertion loss to $<$1 dB, the small spot-size poses challenges in terms of alignment and drift due to quickly decreasing overlap integral off the center point. A 1 dB penalty has already observed for a 0.5 μm misalignment in X-direction. Taking into account that a misalignment will usually have an X- as well as a Y-component, it becomes obvious that the fiber alignment and fixation needs to achieve a precision well below a micron. This can only be done in an active manner.

This is carried out by manipulating the fiber pigtail using sub-micron stepper motors. The fiber, pre-sealed into an external metal tube, is positioned using direct feedback from the illuminated waveguide and, when optimized, is fixed in position using a laser spot welding system. A minimum experimental check of packaged passive devices requires confirmation of correct passive functionality and low insertion loss penalty due to pigtailing. A central issue for the packaging is also the power penalty due to the pigtailing process. Submicron precision can be achieved by active alignment procedures, but fixation of the fiber, shrinkage of adhesive during the curing process and thermal drift usually lead to the preference of welding processes. Fig. 4(a) shows an open view of the packaged passive device with the 1-in 3-out configuration plus electrical contacts. Fig. 4(b) illustrates a microscope analysis image of the input fiber penetrating the side wall while Fig. 4(c) depicts the lensed fiber aligned to the SOI waveguide facet and glued in a permanent position.

For the optical characterization of the packaged passive device, a spectrally flat light source emitting amplified spontaneous emission (ASE) was utilized for capturing the individual DI responses. The polarization state was preserved utilizing a polarizer with over than 30 dB polarization extinction ratio.

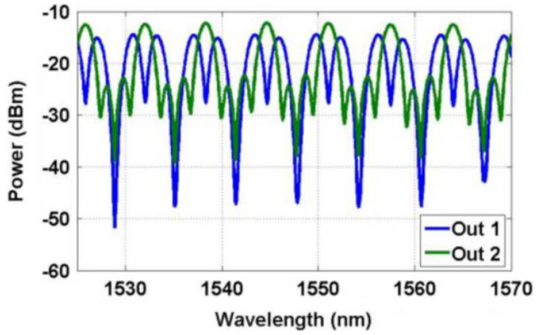

Fig. 5. Chip transfer functions at the output of the second MZI.

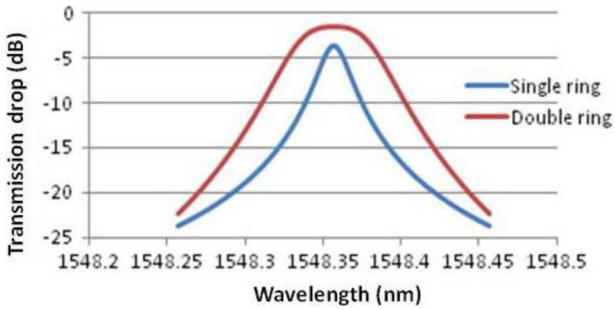

Fig. 6. Comparison of single- and second-order MRR transfer function.

The light was injected into the chip and the spectral responses were acquired by an optical spectrum analyzer (OSA) with a resolution of 10 pm. Then, electrical current was applied to the heating elements in order to extract tuning characteristics of the delay interferometers. With 300 mW electrical power, wavelength shift of 1.5 nm has been obtained. Fig. 5 shows the transfer function of the cascaded filter structures having FSR of 6 nm and 3 nm, respectively. The maximum extinction ratio was 35 dB and it was observed when overlapping the DI spectral dips. The overall chip insertion loss after using a DFB laser as seed has been measured to 8 dB.

B. Microring Resonators for Label Extraction

In BOOM project, MRR demultiplexers are used for optical label extraction and detection. Due to the low crosstalk requirements achieved with first-order MRRs, the solution of second–order ring resonators has been investigated. These devices consist of two coupled rings resulting to more narrow transmission spectrum with a higher roll-off or higher output power at the drop port. To illustrate the superior filter characteristics of the second order ring structures, simulations have been performed for single- and second-order rings regarding crosstalk and drop loss for ring radius of 19 μm. The transmission at the drop port of the double ring is calculated, with 3 dB/cm waveguide loss giving a crosstalk of around 20 dB. Fig. 6 shows that a double ring has a higher roll-off, larger flat band and high out-of-band rejection ratio than a single-ring structure due to the different bandwidth/insertion loss trade off [16].

Fig. 7 shows the different MRR demux structures that have been designed. The MRR structures have been fabricated starting from a SOI wafer and using the 193 nm DUV based

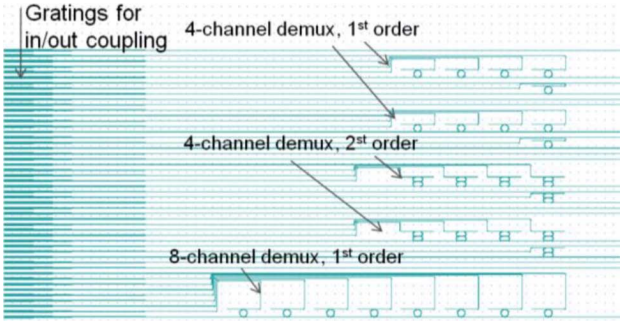

Fig. 7. Mask design.

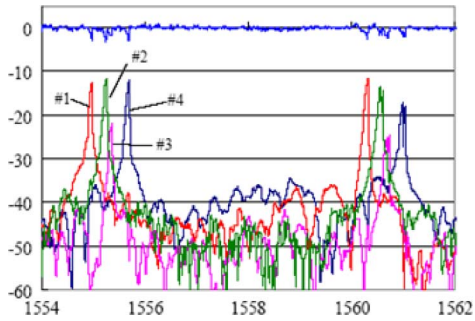

Fig. 8. Through and drop ports of 4-channel first-order MRR demux [P(dBm)-λ (nm)].

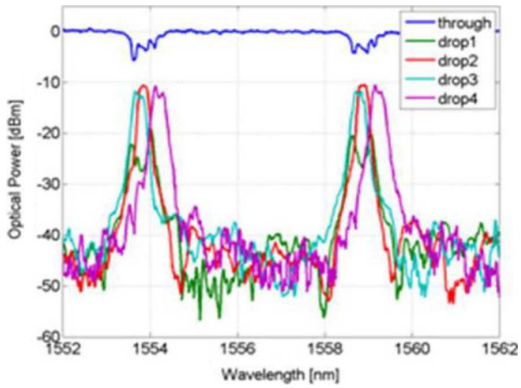

Fig. 9. Through and drop ports of 4-channel second-order MRR demux.

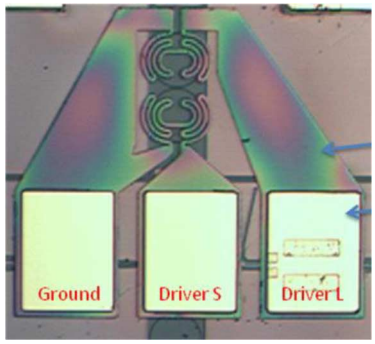

Fig. 10. Heaters for second-order MRR tuning.

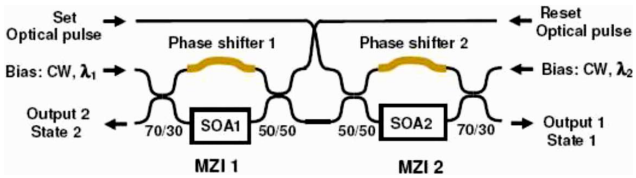

Fig. 11. Flip-flop layout.

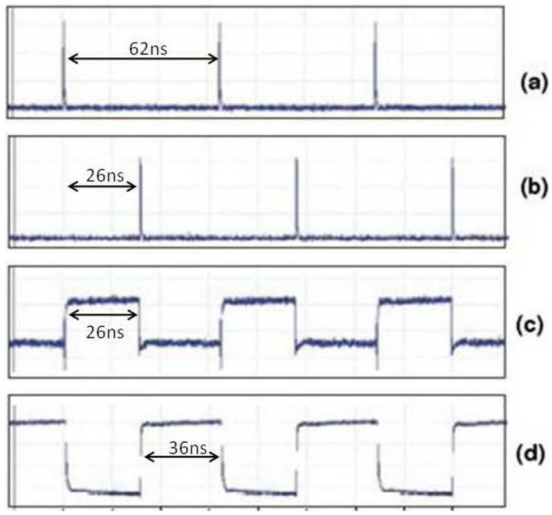

Fig. 12. Flip-flop dynamics. (a) Set pulses. (b) Reset pulses. (c) Output state 1. (d) Output state 2.

process described in [17]. Fig. 8 depicts the measurement results from the 4-channel first-order device. The FSR is about 5.34 nm which agrees well with the designed value (5.5 nm) while the bandwidth of the drop port is equal to 0.04 nm, resulting a Q factor of 40 000. The lower transmission of channel 3 is mainly attributed to fabrication tolerances causing resonance splitting. To overcome the fabrication limitations, one way is to increase the confinement, and therefore employ shallowly etched waveguides, or to decrease the confinement and use TM polarization instead of TE polarization [18].

Second-order MRR demultiplexers have also been optically tested and the results are presented in Fig. 9. Due to fabrication tolerances, the resonance frequencies of both resonators were not always completely aligned, resulting in splitting of the transmission peaks. This filter mismatch was effectively corrected using integrated heating elements for independent wavelength tuning. Titanium (Ti) heaters were employed for heating up the MRR structures and changing the effective refractive index of the light. Thick golden (Au) contact paths were included to guarantee good and robust contacting to the electrical probes while an extra layer of BCB was incorporated between the titanium and gold layer for damaging protection. The left path was used as a common ground whereas the middle and the right path to drive the heaters ($\mathrm{S} = \mathrm{short}, \mathrm{L} = \mathrm{long}$). Fig. 10 shows a close view of second-order MRR heater layout.

C. Hybrid Integrated All-Optical Flip-Flop

A crucial functionality in wavelength routing systems is the generation of new λ s for subsequent wavelength conversion. This can be optically implemented with flip-flops that store the switch control information after set/reset pulse triggering. Different configurations have been demonstrated so far relying on micro-disk lasers, MRRs or nested SOA-MZI structures. With the SOA-MZI setup, a hybrid-integrated packaged flip-flop has

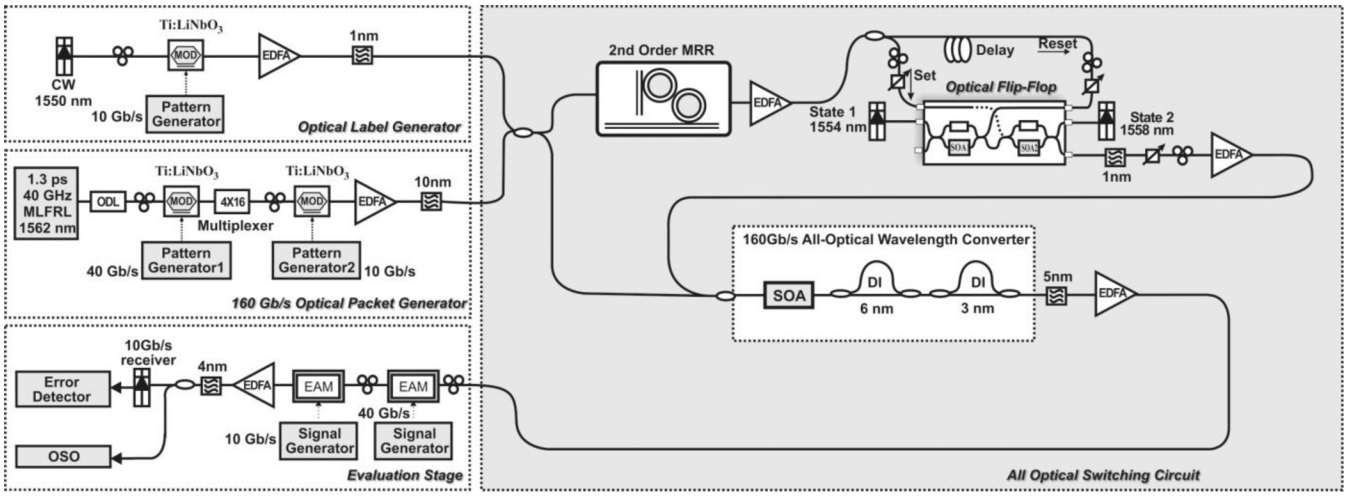

Fig. 13. Experimental setup.

already been fabricated with inherent path length stability and low-loss capability. The device was developed within the framework of IST—project LASAGNE, and it has been extensively studied and tested in [19]. Here we summarize its main operational principles for a better understanding of our preliminary routing concept.

A schematic of the device layout is shown in Fig. 11. It consists of two coupled MZIs with a semiconductor optical amplifier (SOA) in each arm. CWs are injected into the separate MZI inputs bringing the whole system in an optical balance. Depending on the pulse frequency of set and reset pulses, flip/flop states are switched periodically generating complementary CW packet signals at the MZI outputs. The device was designed on a silica-on silicon, passive assembly, hybrid integration platform incorporating buried channel, single-mode silica waveguides. The SOAs were mounted onto separate silicon submounts and flip-chipped into precision recesses milled in the silica on silicon motherboard. The size of the chip was about 45×12 mm^2 and was fully packaged into one complete module including Peltier coolers for both SOAs and thermo-optic silica waveguide phase shifters. Fig. 12 illustrates the dynamic operation of the flip-flop after injecting the set and reset pulses [Fig. 12(a)–(b)] into the coupled MZIs. The temporal responses of the output states are shown in Fig. 12(c)–(d). It can be observed that the generated pulses are complementary but with different extinction ratio. This is attributed to a non-optimal biasing of both flip-flop output states due to non-ideal coupling ratios and to the lack of precise thermal tuning. The produced effects are unequal gain saturation and phase fluctuations. As a consequence only one output state could be exploited featuring a maximum extinction ratio of 11 dB.

V. Experiment

A. Experimental Setup

Fig. 13 depicts the experimental setup. It consists of four main blocks: the 160 Gb/s optical-packets transmitter; the optical label generator; the all-optical switching unit; and the receiver. In the transmitter, optical pulses are generated by a

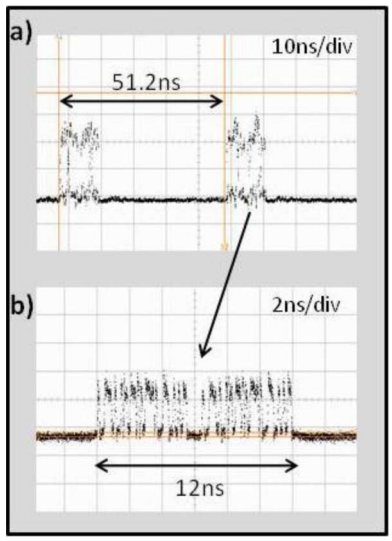

Fig. 14. (a) Packet envelope. (b) Data packet payload.

mode-locked fiber ring laser (MLFRL) at 1562 nm with duration of 1.3 ps and 40 GHz repetition rate, and are encoded with a user pattern from a 40 Gb/s pulse pattern generator (PPG1) to form the optical data sequence based on a $2^7 - 1$ PRBS. The encoded pulses are sent through a fiber interleaver and are time-multiplexed to constitute the 160 Gb/s bit-stream. Subsequently, to form the packets the signal is coupled into an intensity modulator driven by PPG2 which encodes the envelope of the packets. To compensate the rise/fall time of the packet carver ($\sim$20 ps), PPG1 was programmed to generate after time-multiplexing a bit stream with starting/ending zero bits. The periodicity of the packets is of 51.2 ns, whose 12.8 ns correspond to the data payload separated by a guard-band of 38.4 ns. Fig. 14(a) and (b) show the envelope of the packets and the data packets, respectively. As for the optical label generator, a CW light at 1550 nm is modulated by a $LiNbO_3$ modulator producing 5 ns NRZ pulses at 20 Mb/s. Subsequently, the generated labels and the data signal are combined through a DWDM coupler. Two routes follow next. The upper branch couples payload and header into the second–order MRR for label detection and extraction. The MRR features 5 nm FSR,

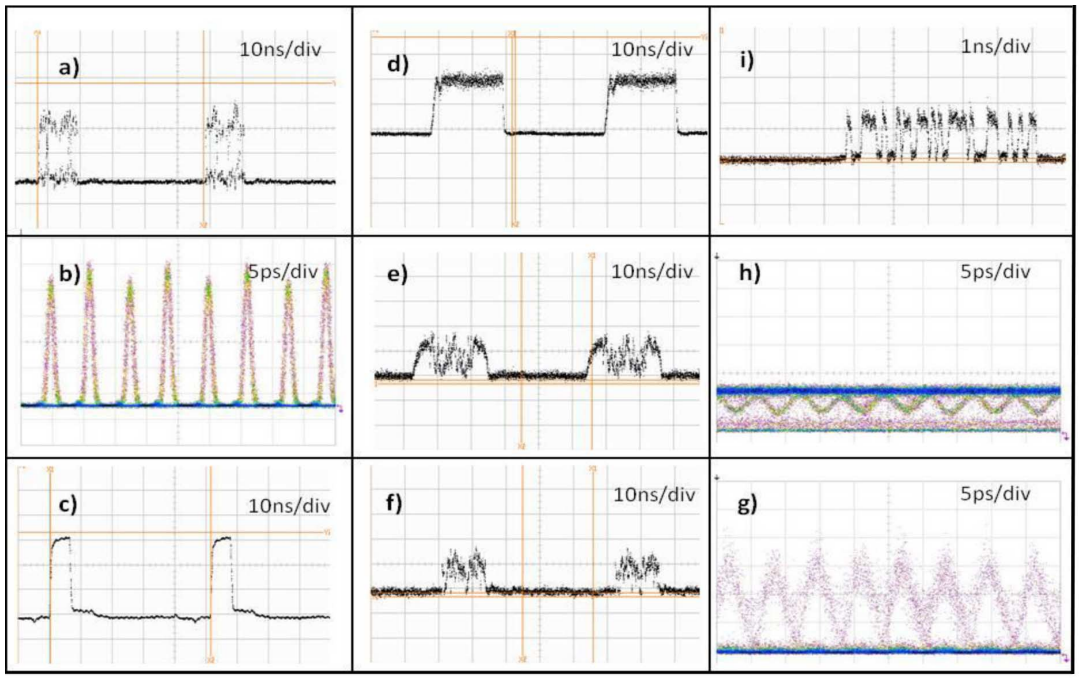

Fig. 15. (a) 160 Gb/s B2B packets. (b) Eye of B2B packets. (c) Optical label. (d) Output of triggered flip-flop. (e) Inverted 160 Gb/s WC packets. (f) Non-inverted WC packets. (g) Eye of non-inverted WC packets. (h) Eye of inverted WC packets. (i) Demultiplexed 160-10 Gb/s WC packet.

3-dB bandwidth of 0.05 nm and wavelength tunability of the label spectral components via the integrated heating elements. The extracted headers are subsequently used for toggling the hybrid integrated flip-flop. The nested MZIs of the flip-flop are biased with two external CWs lasers at 1554 nm and 1558 nm while the set-reset pulses are delayed by 22 ns in order to form a pulse packet, at the output state 2, with rise/fall time of 1.3 ns and duration slightly larger than payload length. The output state 2 of the flip-flop is combined and synchronized with the 160 Gb/s data packet before being coupled together into the AOWC unit. The AOWC is comprised of a commercially available SOA and the recently fabricated and packaged BOOM DI structure. The SOA holds a maximum driving current of 500 mA, a 10–90% gain recovery time of 10 ps, small signal gain of 30 dB and saturation output power of 15 dBm. The packaged device consisted of DI structures with FSR of 6 nm and 3 nm, 8 dB fiber-to-fiber insertion loss, >35 dB extinction ratio and maximum wavelength tunability of 3 nm. The mechanism of wavelength conversion is based on the following basic rules. The incoming payloads interact with the generated flip-flop output into the SOA causing cross-gain XGM and cross-phase XPM modulation. The SOA output is coupled into the photonic integrated circuit. The first DI element converts SPM into amplitude modulation while the second DI element suppresses the carrier to produce a non-inverted version of the wavelength converted signal. The demultiplexing was performed with a set of two-stage electro-absorption modulator (EAM)-based demultiplexer. The first EAM was operated at 40 GHz and the cascaded EAM at 10 GHz. It is worth mentioning that the second-order MRR employed in the setup is not packaged and as such fiber-to-chip and chip-to-fiber coupling had to be performed for label detection and extraction. The light was coupled in and out of the chip through grating couplers with the use of a vertical alignment station. Since the ring structures feature a very narrow bandwidth (0.05 nm), fiber-to-fiber losses were quite high (around 28 dB) requiring very low noise output EDFAs for sufficient amplification. Fig. 14 illustrates the generated B2B packet traffic with 51.2 ns duration and the payload pattern using a 10 Gb/s receiver.

B. Results and Discussion

Fig. 15 illustrates traces and eye-diagrams from the preliminary BOOM routing experiment. Fig. 15(a) shows the 160 Gb/s B2B packet traffic while Fig. 15(b) the respective eye-diagram. The slight amplitude variation observed between the pulses is attributed to the non-optimum equalization in the fiber interleaver. Fig. 15(c) depicts the optical labels generated in head of the data payloads with time-duration around 5 ns for sufficient SOA gain saturation and stable flip-flop operation. Overall spectral efficiency could be further increased using in-band label techniques [20]. The extracted and detected labels were utilized for the flip-flop triggering and the CW packet generation as shown in Fig. 15(d). These envelopes were synchronized with the 160 Gb/s data packets and were injected into the SOA-DI configuration for wavelength conversion. Fig. 15(e) depicts the inverted wavelength conversion operation with data packets placed in the middle of flip-flop outputs for avoiding rise and fall time pattern distortion. Fig. 15(f) illustrates the non-inverted wavelength conversion mode when signal polarity has been restored with carrier suppression. Fig. 15(g) presents the eye-diagram of the non-inverted wavelength converted signal with clear opening area but with noise in the 0-level due to the low extinction ratio of the flip-flop used. The broadening of the pulses at the output of the AOWC is mainly attributed to the narrow 3 dB bandwidth of the delay interferometers. Fig. 15(h)

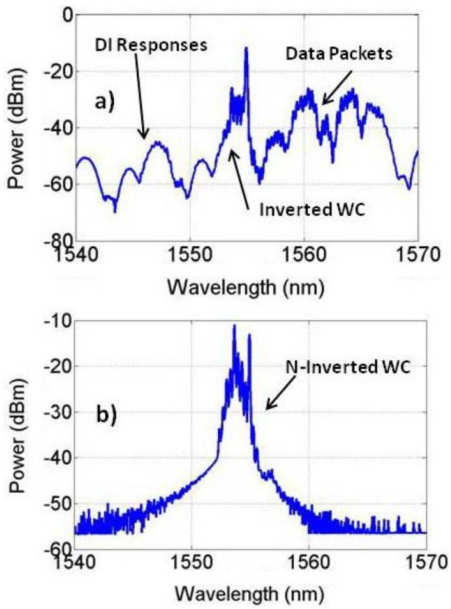

Fig. 16. Spectrums of (a) output of 160 Gb/s WC in inverted operation; (b) output of 160 Gb/s N-Inv. WC.

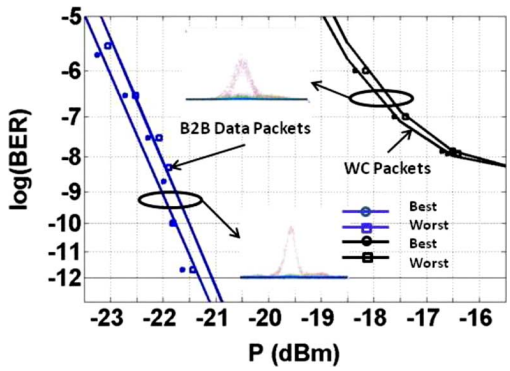

Fig. 17. BER curves of B2B and WC signal.

in turn shows the eye diagram of the inverted wavelength converted signal where effective chirp filtering and SOA acceleration response has been performed. The samples between the two signal levels represent the points acquired by the optical sampling oscilloscope (OSO) due to the rise/fall time of the flip flop. Fig. 15(i) depicts the 10 Gb/s demultiplexed wavelength converted packet. Fig. 16 presents the spectra obtained at the output of the high-speed AOWC. Fig. 16(a) shows the inverted wavelength converted signal, when slight offset filtering is applied, as well as the combined response of the cascaded DI structures. It is observed from this graph that the carrier component is dominant resulting into an inverted version of the wavelength converted signal. In order to obtain a non-inverted version of the signal in question, it is necessary that one of the notches of the DI response coincide with the peak wavelength either by assigning the correct wavelength to the CW packet generator or by thermally tuning the chip response. This is illustrated in Fig. 16(b).

Fig. 17 illustrates the BER curves obtained for the back-to-back (B2B) and wavelength converted packets. In the graph we have plotted the best and worst channels for every case. It is clearly shown that the wavelength converted signal has a power

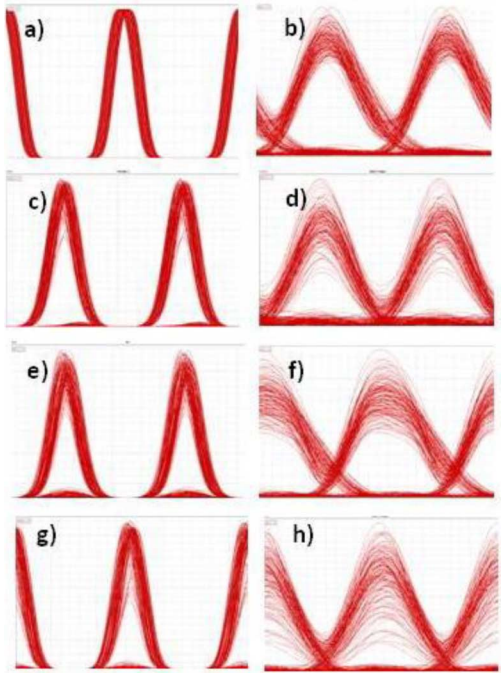

Fig. 18. Signal impairments after sequential WC and regeneration.

penalty of 4.5 dB with respect to the B2B measurements. It is evident an error-floor at 10^{-8}, well above the FEC limit, which is due to the fact that the flip-flop could not be biased perfectly resulting to low extinction at its ports.

This had major effect in the quality of the wavelength converted signal as shown in Fig. 17 (noisy zero level). The imperfect biasing was attributed to the not ideal coupling ratios and lack of precise thermal heating, resulting to unequal gain saturations and phase fluctuations Flip-flop design and fabrication has improved however dramatically through the years, both from energy and operational perspectives, giving the opportunity for optical packet switching at ultra fast data rates [21]. This experimental activity nevertheless, is a truly proof-of-principle concept and it is expected that the replacement of the flip-flops with EMLs in the final BOOM routing platform will improve significantly the system performance.

VI. Performance Over Multiple AOWCs

In a real all-optical network multiple wavelength conversions are required. In order to investigate the signal impairments after cascading wavelength converters we have performed VPI simulations. Fig. 18(a) shows the generated 160 Gb/s back-to-back signal consisting 256 bits of a $2^7 - 1$ PRBS. Fig. 18(b) illustrates the eye diagram after the first all-optical wavelength conversion (AOWC) using the SOA-DI configuration. Due to the pulse broadening at the output of the first AOWC, the induced chirp at the cascaded device is not the sufficient one. To tackle this problem a 3R regenerator is employed in order to generate narrow ($<$2 ps) pulses. The 3R regenerator is a fiber based non-linear-optical loop mirror (NOLM) with 100 m highly non linear fiber. Fig. 18(c) depicts the 160 Gb/s signal after the regenerator while Fig. 18(d) the wavelength converted signal after the second AOWC. Due to the pulse broadening at the output of the second AOWC, a new 3R regenerator is employed.

Fig. 18(e) illustrates the signal after the second 3R regenerator while Fig. 18(f) after the third AOWC. The same process can be performed for one more time as depicted in Fig. 18(g)–(h). It is evident that multiple wavelength conversions using the SOA-DI scheme requires 3R regeneration after each process. The simulations have shown that a 160 Gb/s signal survives after four cascaded wavelength conversions due to the accumulation of amplitude modulation. The AOWC cascading performance can be further increased if an optical hard limiter is employed in order to alleviate the amplitude modulation generated by the AOWC process.

VII. Conclusion

We have demonstrated an all-optical circuit that can perform packet switching at 160 Gb/s using a second-order MRR for label extraction, a hybrid integrated optical flip-flop for control signal generation and a SOI-DI packaged module for ultra-fast packet wavelength conversion. The optical components were assembled to realize 160 Gb/s optical packet switching with 4.5 dB power penalty and error performance well above the FEC limit. The next phase of the BOOM project involves the development of fully hybrid integrated and packaged devices and the assemble of the first 160 Gb/s photonic routing platform.

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