Towards Optical Networks-on-Chip with 200mm hybrid technology

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Abstract—**Integrated components for optical networks-on-chip, including III-V microdisk lasers, photodetectors, and wavelength selective circuits, are all demonstrated using a complementary metal-oxide-semiconductor (CMOS) compatible III-V/silicon-on-insulator integration technology at 200mm wafer scale.**

Keywords—silicon photonics; microdisk lasers and photodetectors; heterogeneous integration; network-on-chip

I. INTRODUCTION

Optical interconnects and more complex optical network-on-chip (ONoC) are likely to replace the current electrical wires for transporting information between processor cores [1]. However such architectures rely on the compliance of all photonic functions - including compact electrically injected laser sources - within silicon. Here we present our recent developments for future electro-photonic integrated circuits. In particular continuous wave operation microdisk lasers, photodetectors, and wavelength selective circuits are demonstrated using a CMOS compatible III-V/silicon technology at 200mm wafer scale.

II. CMOS COMPATIBLE INTEGRATION TECHNOLOGY

The integration scheme makes use of III-V semiconductor materials for both lasers and photodetectors, whereas passive circuits are realized by patterning silicon on insulator (SOI) films. A specific process adapting and modifying the standard III-V material process steps to comply with a CMOS environment is developed, using the so-called above-IC approach schematically represented in Fig.1. In this approach

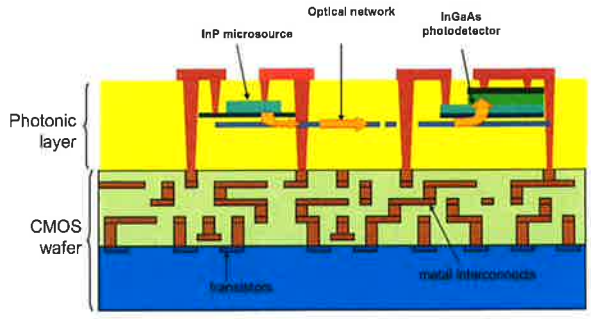

Figure 1. Above-IC silicon photonics and III-V/SOI integration scheme.

the devices are fabricated at the back-end of line (BEOL) levels keeping a temperature budget limited to 350°C – 400°C. To achieve CMOS compatibility, i) die-to-wafer bonding was developed at the 200mm scale, ii) a dry etching chemistry capable of etching the III-V dice while preserving the Si/SiO_2-based surface was investigated and iii) CMOS compatible metals replace standard gold based contacts used in optoelectronics.

The heterogeneous integration of III-V materials and SOI circuits is performed with the die-to-wafer bonding technology, where unpatterned III-V dice are integrated on top of a processed SOI wafer by means of SiO_2/SiO_2 direct bonding. This process under development allowed us to achieve a bonding yield in the order of 80% after complete InP substrate removal. For direct bonding, the thickness of silicon dioxide above the Si waveguide is adjusted to 100 nm. Following the CMP, SOI wafers are cleaned in a RCA solution performed in specific equipment (FSI Magellan). InP hetero-structure is directly covered by a 10 nm thick SiO_2 layer compatible with direct bonding (means a roughness < 0.5 nm RMS) deposited by plasma-enhanced chemical vapor deposition (PECVD). To prevent undesirable out-gassing from the oxide layer during subsequent heat treatments, wafers were annealed at a temperature higher than the subsequent processing temperature after SiO_2 deposition. After annealing, InP wafer is first cleaned in acetone and ethanol, following by DI water rinse and blow-dried in nitrogen. O_2 plasma treatment is then performed in order to active surface by creating a high density of hydroxyl groups (-OH). Wafers are then put in contact at room temperature to perform the bonding. As III-V waveguide are fabricated after bonding, no tight alignment is needed during spontaneous bonding. Finally, the bonded pair is annealed at 200°C for 3 hours. A selective wet etching in $HCl:H_2O$ (3:1) and $H_2SO_4:H_2O_2:H_2O$ (1:1:10) removed InP substrate and InGaAs etch stop layer, respectively. This leaves the epilayer structure of 1µm thick bonded above Si waveguide and ready for processing of the III-V laser structure.

The 100 nm thick bonding oxide layer allowed by the architecture has the advantage of limiting the formation of bonding interface voids. Indeed, the formation of

bonding defects upon annealing depends on the thickness of the interfacial oxide layer [24]. Figure 2(a) and (b) compared III-V structure bonded on Si with different oxide thickness. The structure bonded with 40 nm thick oxide layer presents a high density of voids at the bonding interface. On the contrary, the structure bonded with 100 nm thick SiO_2 presents a void-free surface. By product species originating from the bonding reaction are principally absorbed by oxide layer. In the case of 40 nm thick, there is less volume to store by-products, which could explain the formation of interfacial defects. For an oxide thickness of 100 nm, all the by-product species are stored in the SiO_2 bonding layer and thus no defects are formed at the bonding interface. It should be noted that nucleation points can influence the defect apparition. So it is important to bond III-V epitaxial layer with low surface defects density.

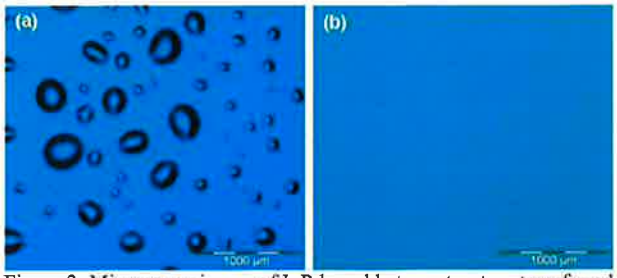

Figure 2. Microscopy image of InP-based hetero-structure transferred on Si wafer with (a) 40 nm thick silicon oxide and (b) 100 nm thick silicon oxide.

Figure 3 (a) shows an optical image of the 2 inch InP wafer bonded to processed SOI (with 100 nm thick SiO_2) after annealing and InP substrate removing. Over 98% of III-V laser structure is transferred onto Si waveguide systems. The 2% un-transferred part coming from both edge under-etching of the structure during chemical substrate removal and from the presence of localized voids on the structure. The latter probably originate from the presence of epitaxial defects on the III-V structure acting as nucleation point for the voids formation. Cross-sectional SEM (Scanning Electron Micrograph) images of the Figure 3(b) shows the quality of the bonding above the Si waveguides.

An original III-V epi layer design where the laser and the photodetector heterostructures are stacked within the same epitaxy was implemented to fabricate the photonic chips (cf. Fig. 1). Compared to already demonstrated point-to-point links where some dice are dedicated to laser structures and some others to photodetectors structures [3], this enables a much simpler integration scheme as well as much lower footprint optical links. The total epitaxy thickness is only 1µm which enables the use of 248nm deep ultraviolet (DUV) lithography without focalization issues. The subsequently III-V processing, including wet and CH_4-H_2-based reactive ion etching, oxide isolation layer deposition, metallization, is optimized at 200mm wafer scale [4]. Regarding electrical contacts, the standard gold-based metallization and the usual lift-off technique to define the contact area were discarded. Instead, a Ti/TiN/AlCu metal stack is full-sheet deposited. After a lithography step, the metal stack is dry-etched with a chlorine-based chemistry down to the oxide isolation layer which also acts as an etching stop layer. Ohmic contacts on both n-InP and p-InGaAs are obtained without any annealing performed on the wafers [4]. Figure 4 shows an image of a fully processed microdisk laser after contact metallization.

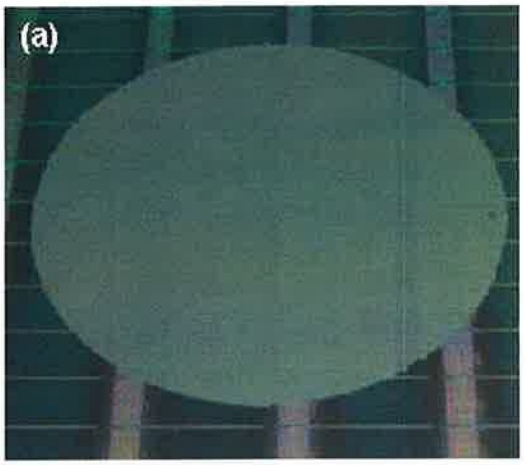

Figure 3: (a) Optical image of 2 inch III-V heterostructure reported to processed SOI by direct bonding. InP substrate and etch stop layer was removed. (b) SEM cross sectional image of III-V structure bonded above Si waveguides.

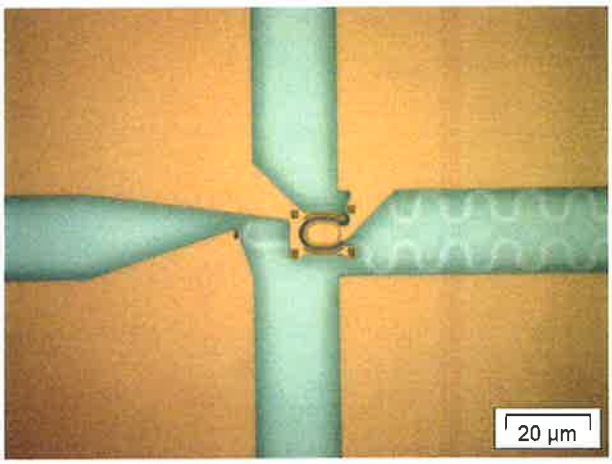

Figure 4: Integration of InP µlaser devices on top of SOI passive circuits after the last metallization step.

III. Microdisk Lasers, Photodetectors, and Thermally Tuned Ring Demultiplexers

Microdisk lasers with diameters of 20µm and 40µm were fabricated and characterized. The output power was collected at one end of the SOI waveguide by using a fiber grating coupler. Continuous-wave (CW) lasing at room temperature was observed. The light-current-voltage (LIV) curve of a 40µm diameter microdisk laser is shown in Fig. 5(a). The VI curve is similar to devices

fabricated earlier where gold contacts were used [6]. It can be seen that these devices have a threshold current of 6mA, corresponding to a threshold current density of 0.48kA/cm^2. A maximum output power of 150μW in the SOI waveguide was measured. The optical spectrum of such a microdisk laser at 23.4mA bias shows a side mode suppression ratio higher than 27dB (inset of Fig. 5a).

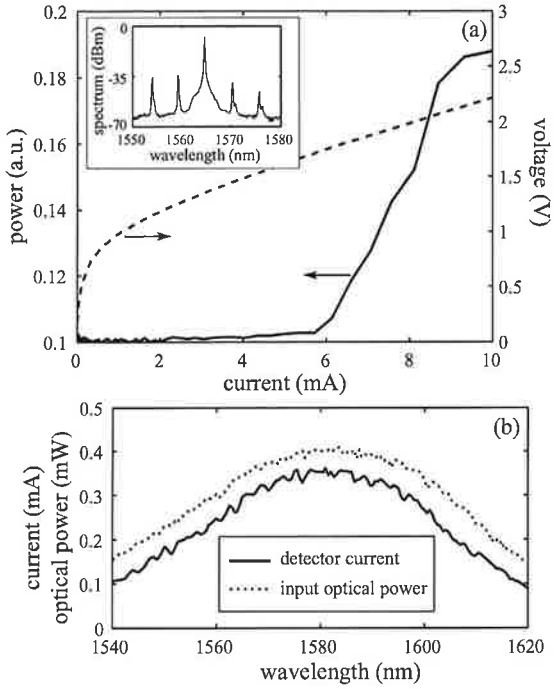

Figure 5. (a) LIV curve of a 40μm diameter microdisk laser. Inset shows the laser spectrum at 23.4mA bias. (b) Wavelength response of an evanescently coupled waveguide detector with an 80μm long absorption section.

Evanescently coupled waveguide detectors with various lengths were fabricated, and the SOI waveguides under the detectors were tapered to different widths to examine the coupling efficiency. Responsivity varies from 0.7A/W for detectors with 20μm long absorption sections to 0.9A/W for 100μm long absorption sections on top of 500nm wide waveguides. The wavelength response is shown in Fig. 5b) for a detector with an 80μm long absorption section. The Gaussian shaped spectrum is caused by the fiber grating couplers.

Wavelength division multiplexing (WDM) is necessary for improving the capacity of one connection. In ONoCs wavelengths can also be used as a routing mechanism between difference processor cores. Ring based (de)multiplexer is an ideal structure in this case concerning the footprint.

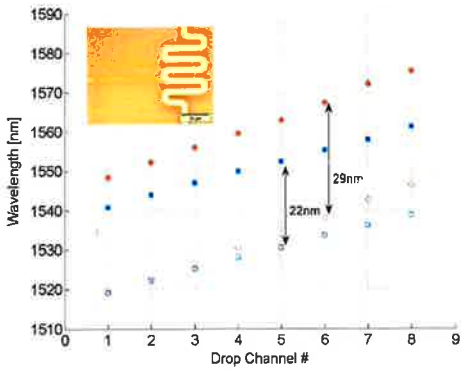

Figure 6. Experimentally measured channel wavelengths for two 8-channel demultiplexers with 29nm and 22nm FSR, respectively. The inset shows a microscope image of the fabricated heater with underlying ring resonator.

Figure 6 shows the measured channel wavelengths from two such demultiplexers. Each of them was built by cascading 8 SOI ring filters with slightly different diameters on one bus SOI waveguide. Uniform distribution of the channel wavelengths between one free spectral range (FSR) is presented. Further fine-tuning of the wavelength positions can be realized through an integrated Ti/TiN heater on top of each ring as shown in the inset of Fig. 6. A tuning rate of 0.3nm/mW was obtained experimentally [5].

IV. Conclusion

We have demonstrated a CMOS compatible III-V/SOI technology at 200mm wafer scale that enables the realization of microdisk lasers, photodetectors, and thermally tuned ring filters with promising performance, therefore paving the way to the demonstration of ONoCs.

V. Acknowledgment

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