LASER & PHOTONICS REVIEWS

Abstract In this paper III-V on silicon-on-insulator (SOI) heterogeneous integration is reviewed for the realization of near infrared light sources on a silicon waveguide platform, suitable for inter-chip and intra-chip optical interconnects. Two bonding technologies are used to realize the III-V/SOI integration: one based on molecular wafer bonding and the other based on DVS-BCB adhesive wafer bonding. The realization of micro-disk lasers, Fabry-Perot lasers, DFB lasers, DBR lasers and mode-locked lasers on the III-V/SOI material platform is discussed.

$20\,\mu m$

L1   L2   L3   L4

Artist impression of a multi-wavelength laser based on micro-disk cavities realized on a III-V/SOI heterogeneous platform and a microscope image of a realized structure.
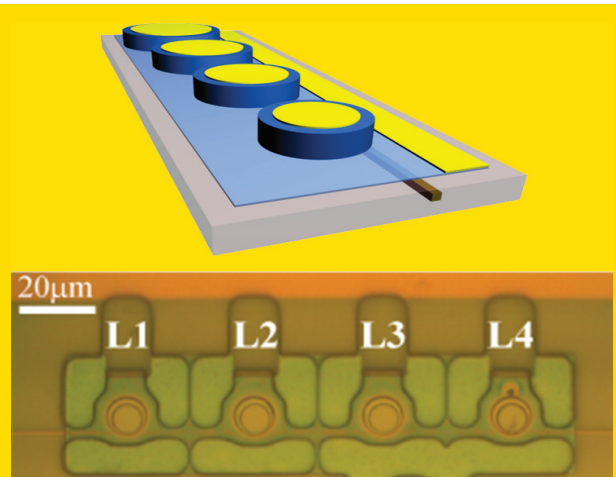
III-V/silicon photonics for on-chip and inter-chip optical interconnects

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1. Introduction

The CMOS industry is driven by Moore's law, with transistors per chip (and hence computational power per dollar) roughly doubling every 24 months [1]. However, limitations are being approached that fall beyond the transistor design. Interconnect bandwidth, e.g. for I/O and clock distribution, is a major source of uncertainty for higher performance computer systems. The reason for this is because electrical interconnects do not scale at the same rate as transistors as their dimensions are shrunk, resulting in a decrease in reach for faster interconnects [2]. Optical interconnects have been proposed as an alternative to copper-based interconnects for both on-chip and off-chip applications. Optical

on-chip interconnects were first proposed by Goodman in 1984 [3] and analysis from various groups agree that optical interconnects would be useful for global clock distribution. To be competitive with copper interconnects, wavelength-division multiplexing (WDM) will be needed to increase the bandwidth density [4,5]. Off-chip electrical interconnects on FR4 have demonstrated 20 Gb/s over 7 in. [6] but over a distance of 10 in. or above electrical communication at 10 Gb/s is extremely challenging; and, with aggregate I/O interconnect bandwidths approaching 1 Tb/s by the middle of the next decade [7], again WDM-type optical networks have to be considered. As well as the obvious bandwidth and latency advantages that optical interconnects provide they also offer secondary advantages dis-

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cussed by Miller [2], including voltage isolation, reduced power dissipation and architectural advantages inherent in building larger synchronous systems. There is a wide range of research investigating different material systems and architectures for optical interconnects [8]; here we focus on using silicon due to its direct compatibility with CMOS processing, and small waveguide size leading to high bandwidth density. Many basic building blocks have been demonstrated in silicon photonic technology. High-speed, 40-Gb/s, modulators [9] and photodetectors [10] have been demonstrated as well as passive devices such as multiplexers and demultiplexers [11], leading to high-bandwidth silicon photonic chips [12]. In fact, the only device that has not been demonstrated from a group IV element is an electrically pumped laser. Various options have been suggested for this shortfall, such as fiber coupling an external packaged laser to the silicon chip. This has an advantage in terms of thermal isolation but is not an integrated solution and so has larger footprint and lower power efficiency due to fiber coupling loss. Alternatively, individual laser dies can be flip chipped to the optical wafer. Here tight mechanical alignment requirements make this option less attractive, especially as the number of lasers required per chip increases for WDM systems. In this paper we will review two different methods of achieving hybrid integration of III-V lasers with silicon-on-insulator (SOI) waveguides using molecular direct and adhesive bonding. The advantage of this approach is that many lasers may be fabricated by bonding a single III-V die onto the silicon chip, giving the possibility of fabricating arrays of multi-wavelength lasers integrated with other silicon photonic components suitable for WDM links. The paper is arranged as follows. Sect. 2 discusses the technologies behind the two bonding approaches and efforts to optimize them for this application, i.e. reducing the void density in direct-bonded samples using vertical channels and reducing the adhesive DVS-BCB (divinylsiloxane-bis-benzocyclobutene) thickness to sub-100 nm. Sect. 3 discusses lasers suitable for on-chip interconnects; here size and efficiency are important with the laser output required to be < 1 mW and both single and arrays of lasers are described. Lastly in Sect. 4 higher power lasers suitable for chip-to-chip communications are described; here Fabry-Perot (FP), distributed feedback (DFB) and distributed Bragg reflector (DBR) lasers are demonstrated integrated with SOI waveguides as well as a multi-wavelength mode-locked laser source.

2. Bonding technology: direct and adhesive bonding

As elaborated on in the introduction, the integration of III-V compound semiconductors on top of an SOI waveguide circuit allows realizing complex active/passive photonic integrated circuits. In order to realize these circuits, III-V material has to be transferred to the silicon waveguide platform. Two approaches could be envisioned. In one approach the III-V opto-electronic component is (partially)

processed on the III-V wafer and then transferred to the silicon platform using flip-chip integration [13] or epitaxial lift-off processes [14]. This however requires stringent alignment in the assembly process, making this an expensive operation. The approach followed in this work is to transfer sheets of epitaxial material to the silicon platform (this could be on the III-V die or III-V wafer level) and to process the III-V opto-electronic components afterwards. This makes the assembly process easier since no stringent alignment is required and it allows exploiting lithography to align the III-V components to the underlying SOI waveguide circuit on a wafer level. This transfer of III-V epitaxial layers is realized by wafer-bonding technology. In the following sections, two different technologies (direct bonding and adhesive bonding technology) will be discussed.

2.1. Direct bonding technology

Wafer bonding normally refers to a technology that brings mirror-polished, flat and clean wafers into contact to realize a strong bond between them either by interfacial bonds or by using a 'glue', e.g. polymers or metals. Direct wafer bonding and adhesive bonding are used to differentiate two mainstream bonding techniques in this paper. High-quality direct wafer bonded silicon-on-insulator (SOI) substrates up to 300 mm in diameter have been commercially available since 2000, showing wafer bonding as a highly manufacturable and high-yield fabrication process.

A key challenge for direct bonding of dissimilar materials, for example compound semiconductor to silicon bonding, is the thermal expansion coefficient mismatch. This is problematic as a key step in conventional direct bonding is a high-temperature (> 600 °C) anneal, which is forbidden when bonding dissimilar materials. Several approaches have been proposed to enable bonding at low temperature (< 400 °C) or even room temperature. A more detailed discussion for problems associated with low-temperature bonding can be found in [15].

Recently, a process called 'O$_2$ plasma-assisted wafer bonding' has been developed for this purpose as well [16, 17]. Taking InP-based compound semiconductor and Si as examples here, Fig. 1 shows the typical bonding process flow of the O$_2$ plasma-assisted process for fabricating hybrid III-V/silicon devices [18].

After a rigorous sample-cleaning procedure, native oxides on Si and III-V compound semiconductors are removed in HF and NH$_4$OH solutions, respectively. The following O$_2$ plasma step converts the hydrophobic sample surfaces to hydrophilic ones by growing a thin layer of highly reactive native oxide, subsequently resulting in a high density of $-$OH groups (i.e. hydroxyl groups) on the sample surfaces after contacting with H$_2$O-based solutions. After mating the two substrates at room temperature via relatively poor Van der Waals forces or hydrogen bonds, the well-known chemical reactions in Si-based hydrophilic bonding given in Eqs. (1) and (2) start forming strong covalent bonds [19],
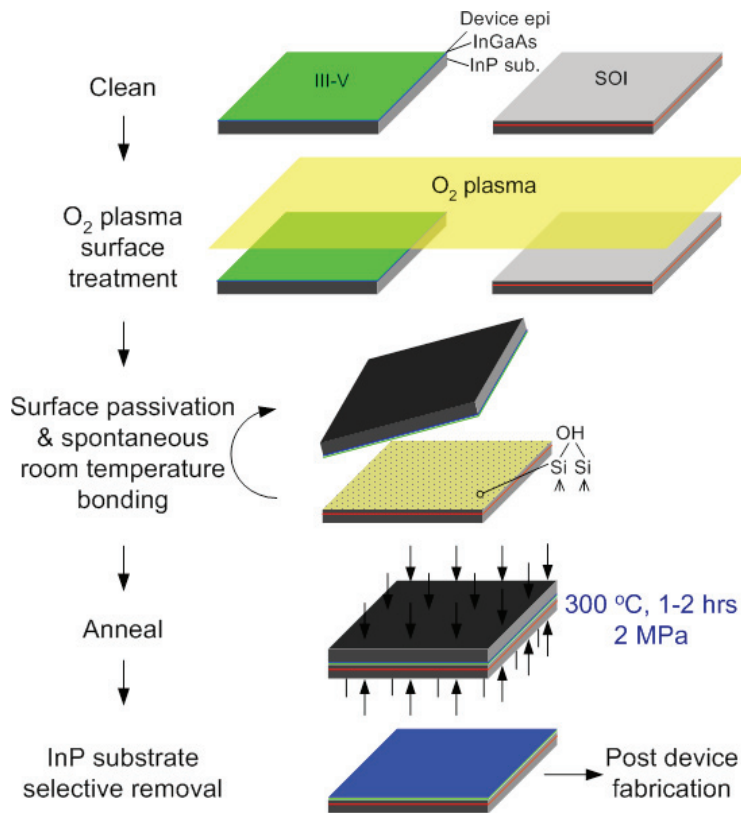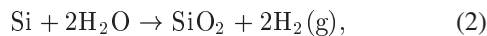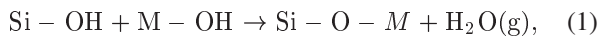
Figure 1 (online color at: www.lpr-journal.org) Schematic of the O_2 plasma-assisted low-temperature III-V-to-Si bonding process flow.

a process accelerated by further annealing at elevated temperature (300 °C in this work).

$$Si - OH + M - OH \rightarrow Si - O - M + H_2O(g), \quad (1)$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2(g), \quad (2)$$

where M stands for a metal with high electronegativity, such as group III and group V elements.

The gas byproducts of H_2O and H_2 from the intrinsic chemical reactions in Eqs. (1) and (2) can accumulate and cause a large number of interfacial voids at the bonding interface as shown in Fig. 2 and can even cause debonding. The void size varies in Fig. 2, depending on different wafer surface states, such as surface roughness, defect density, etc. [20]. Removing the gas byproducts efficiently is therefore a critical step in obtaining high-quality low-temperature bonding.

The first efficient approach to eliminate the outgassing issue in this work is to utilize a layer of interfacial amorphous dielectric to absorb the gas byproducts. The common interfacial amorphous dielectric is thermal or plasma-enhanced chemical vapor deposition (PECVD) SiO_2 or SiN_x. In order to maintain good optical and thermal coupling between a III-V epilayer and Si, the amorphous dielectric of thermal SiO_2 for silicon and PECVD SiO_2 for III-V needs to be less than 100-nm thick [21]. In our experiments 30 nm of each is chosen to give a total interfacial layer thickness of 60 nm. Other than the processing steps illustrated in Fig. 1, several special sample preparation steps
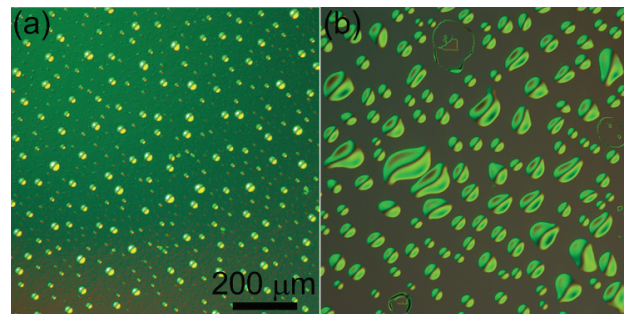

Figure 2 (online color at: www.lpr-journal.org) Nomarski-mode microscopic images of InP thin epitaxial layers directly transferred to the SOI substrate after 300 °C anneal for 2 h, showing a large number of interfacial voids. (a) and (b) are bonding pairs using materials from different III-V and SOI vendors. Scale in (a) applies to (b) as well.

are required for this oxide bonding. Due to the inhomogeneous nature of the PECVD process [22, 23], a degassing bake at 250 °C for 1 to 2 h is needed after depositing SiO_2 on III-V in order to drive undesirable gas molecules out of the thin film. Immediately after the O_2 plasma surface treatment, the second surface activation step is to dip the SOI and III-V samples in a very dilute HF solution (0.025 percent) for 1 min to form a more porous fluorinated oxide network [23]. The last activation step involves further converting Si–OH to Si–NH$_2$ bonds in NH$_4$OH [19, 24].
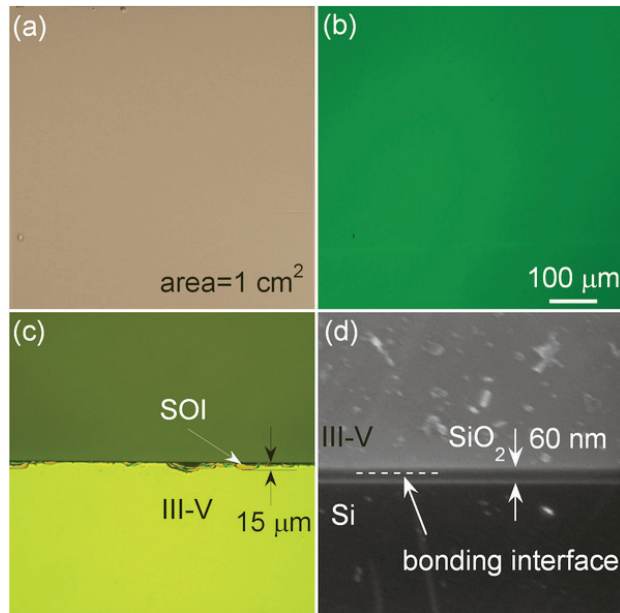
Figure 3 (online color at: www.lpr-journal.org) (a) Photograph of 1-cm^2, 2-μm-thick III-V epilayer transferred to the SOI substrate; (b) close-up Nomarski-mode microscopic image showing a void-free interface, (c) microscopic top view of a diced bar showing 15-μm III-V chipping due to dicing; (d) SEM cross-sectional view of a polished bar, showing III-V epitaxial layers tightly bonded on the SOI substrate with a 60-nm interfacial SiO$_2$ layer.

Figure 4 (online color at: www.lpr-journal.org) Schematic cartoons of vertical outgassing channels (VOCs) on the SOI substrate (a) before and (b) after contacting with InP epitaxial layers; (c) microscopic top view of a racetrack ring resonator layout with VOCs; (d) SEM cross-sectional view of VOCs with InP epitaxial layers bonded on the top, showing intimate contact with no deformation or delamination.

Figs. 3a and b show a 1-cm^2 thin III-V epilayer transferred to the SOI substrate and its typical close-up ($\times 100$) Nomarski-mode microscopic image. Compared with Fig. 2, a void-free interface is obtained both locally and globally. It is noted that the surface morphology after removing the thick InP substrate is inspected using high-resolution Nomarski-mode microscopy routinely, which can resolve sub-μm features. However, the conventional infrared transmission imaging or scanning acoustic microscopy, whose best resolutions are usually more than 100 μm and 15 μm, respectively, are not capable of resolving all the tiny interfacial voids.

According to a statistical study, the average void density is less than 5 cm^{-2}, which we believe is due to surface defects in the III-V epilayer rather than outgassing. Bonding strength is measured prior to InP substrate removal using the conventional crack-opening method. Consistent results of III-V breakage upon inserting a thin blade (100-μm thick) indicate that the bonding surface energy exceeds the bulk InP fracture energy of 0.63 J/m^2 [25]. III-V/SOI bonded samples were also subjected to a harsh dicing test to qualitatively study the bonding strength by measuring the chipping from the dicing edge. With the III-V side up and without surface protection during the 10,000 rpm dicing, the chipping of the III-V epitaxial layer is no more than 15 μm as shown in Fig. 3c. Fig. 3d shows a scanning electron microscopic (SEM) cross-sectional view of a final polished bar, showing III-V epitaxial layers tightly bonded
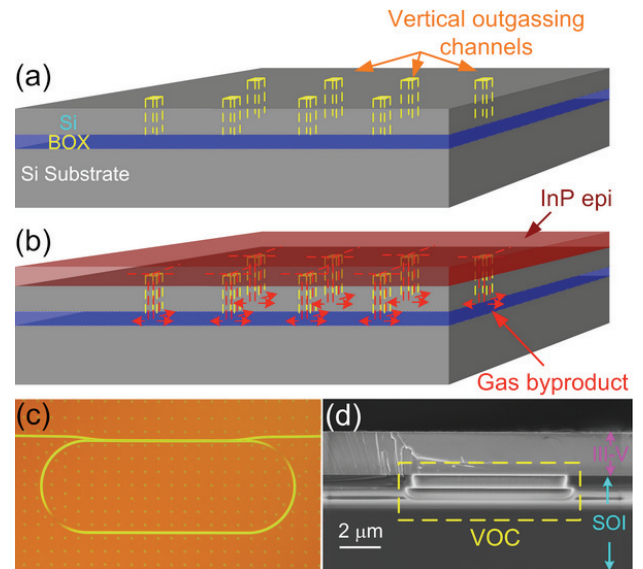
on the SOI substrate with a 60-nm interfacial SiO$_2$ layer. The survival of a harsh dicing and polishing indicates strong bonding between the III-V material and the SOI substrate. This bonding technology has also been used by other groups to realize III-V on silicon bonding [26].

Another efficient method to avoid outgassing is to deploy vertical outgassing channels (VOCs) on SOI prior to mating [27]. As illustrated in the cartoon image in Fig. 4a, VOCs are an array of holes, a few micrometers in diameter, etched through the top Si device layer to the underlying buried oxide (BOX) layer prior to contact with the III-V material. The generated gas byproduct molecules plus a small amount of trapped air molecules including any gaseous impurities can migrate to the closest VOC and can be promptly trapped in VOCs and eventually absorbed by the buried oxide layer as shown in Fig. 4b. Thereafter, they may also gradually diffuse out through the BOX layer, due to its open network of only 43 percent of occupied lattice space [28] and its large diffusion cross section, generally 0.3–3-μm thick. Due to the strong optical confinement in SOI waveguides, VOCs can be placed flexibly around the waveguide layout as shown in Fig. 4c. A SEM cross-sectional view of a VOC with thin III-V epitaxial layers bonded on top is shown in Fig. 4d, demonstrating intimate contact of III-V and Si with no III-V deformation above the VOC.

Studies of the VOC effectiveness dependence on VOC spacing and VOC size show that a smaller VOC spacing gives fewer interfacial voids. Eventually, void-free bonding is achieved when the spacing is equal to or less than
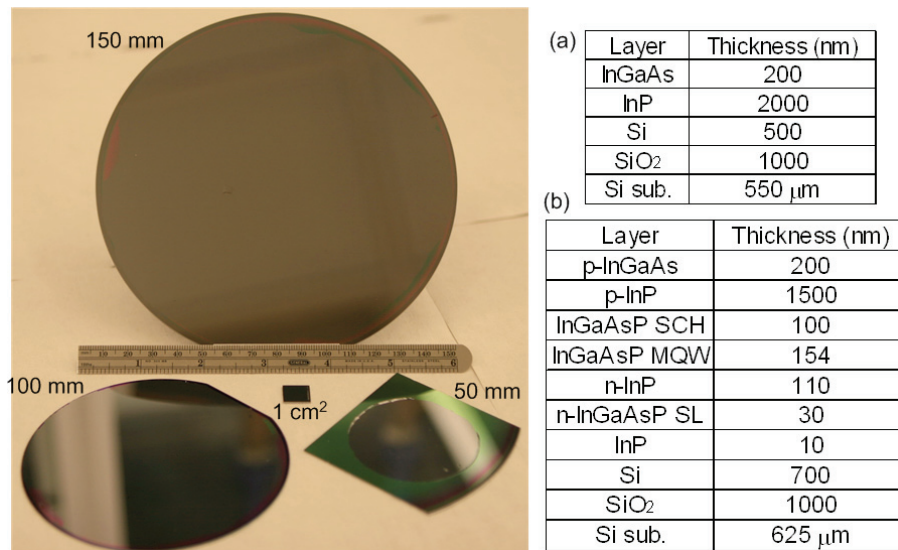
(a) Layer	Thickness (nm)
InGaAs	200
InP	2000
Si	500
SiO2	1000
Si sub.	550 μm

(b) Layer	Thickness (nm)
p-InGaAs	200
p-InP	1500
InGaAsP SCH	100
InGaAsP MQW	154
n-InP	110
n-InGaAsP SL	30
InP	10
Si	700
SiO2	1000
Si sub.	625 μm

Figure 5 (online color at: www.lpr-journal.org) Photographs of thin InP epilayer of $1 \, cm^2$, 50, 100 and 150 mm in diameter bonded on the SOI substrate. Table (a) represents the bonded epitaxial structure for all bonding experiments except the 150-mm one, which is the MQW diode laser structure of Table (b).

$50 \, \mu m$ [27]. The size of the VOC plays a secondary role with larger size leading to fewer voids. The strong dependence on the spacing indicates the existence of a limited area coverage for each VOC. Ideally, void-free bonding can be achieved as long as the area coverages start overlapping each other, eliminating the existence of a 'dead zone', which is most likely to be $S = 50 \, \mu m$ in this work. In other words, the outgassing issue can be fundamentally eliminated if VOCs with the appropriate scheme are employed, regardless of the wafer dimensions. Fig. 5 is a photograph of a thin III-V epilayer bonded onto an SOI substrate of $1 \, cm^2$, 50, 100 and 150 mm in diameter where the same VOC scheme ($S = 50 \, \mu m$, $t = 8 \, \mu m$) is employed. The insets (a) and (b) are the epitaxial structures of the 150-mm SOI and InP-based multiple quantum well (MQW) wafers for the 150-mm bond. Mirror-like, void-free III-V epitaxial transfer is achieved with over 95 percent transfer yield regardless of the wafer size. The epitaxial transfer quality is further characterized by a high-resolution X-ray diffraction (XRD) rocking curve measurement. The (004) diffraction peak from the 1.5-μm InP cladding layer is used as the reference. Fig. 6 represents the direct comparison of simulated and measured Omega-2Theta scans at the center of the as-grown and transferred epitaxial layers of the 150-mm bond. All MQW satellites are able to be probed at nearly identical positions with no peak broadening, indicating the well-preserved crystalline structural integrity and low-strain bonding.

2.2. Adhesive bonding technology

2.2.1. Literature review

Besides the direct bonding approach, described in the previous section, adhesive bonding methods can also be used to integrate III-V semiconductors on top of an SOI waveguide circuit. As the choice of the adhesive depends on the
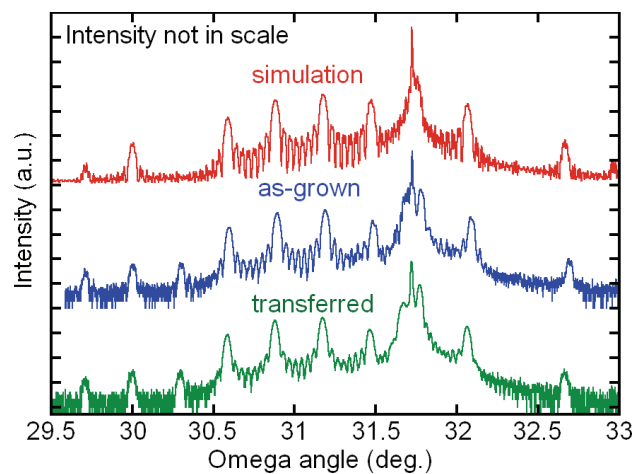

Figure 6 (online color at: www.lpr-journal.org) XRD simulated Omega–2Theta scan (top) of InP epitaxial structure and rocking curve measurements of the 150-mm as-grown layer (middle) and transferred layer (bottom) at the InP epitaxial wafer center with (004) InP peak as the reference peak.

application, we will start with a literature review of the various types of adhesives available before concluding with the selection of DVS-BCB as the adhesive for III-V/SOI bonding. This literature review is not exhaustive and an extensive review of adhesive wafer bonding can be found in [29].

In the literature, thermoplastic, elastomeric and thermosetting materials are used for adhesive bonding. As thermoplastics remelt when heated sufficiently, the postbonding thermal budget for processing of devices is limited in these cases. Elastomers (often referred to as rubbers) typically show viscoelastic behavior: they exhibit the characteristics of a viscous liquid and an elastic solid at elevated temperature. These adhesives (thermoplastic and

elastomers) can therefore not be used for the integration of III-V material on an SOI substrate due to their limited thermal budget, since the post-bonding process temperatures for the III-V components typically go up to 400 °C. Thermosetting materials are more attractive for this purpose, since it is the temperature stability of the material in this case which will determine the post-bonding thermal budget.

There are several reports on the use of thermosetting polymers as a bonding agent. DVS-BCB, epoxies, spin-on-glasses and polyimides are the most common ones. Polyimides are known to result in large unbonded areas due to the presence of voids at the bonding interface, which is attributed to the creation of byproducts during the imidization process, which get trapped at the bonding interface [30]. Silver-loaded conductive epoxies were used in [31] to realize thin-film III-V LEDs on a host substrate. Since the bonding layer in this case is not optically transparent, it cannot be used for our envisioned application. Spin-on-glass (SOG) was used in [32] to transfer III-V VCSEL epitaxial layer structures to a silicon substrate. A careful choice needs to be made here in selecting the right SOG (especially the amount of organic content in the SOG), since a too low organic content can result in excessive shrinkage of the SOG upon cure resulting in large film stress and low cracking resistance.

Many reports are available on the use of DVS-BCB (divinylsiloxane-bis-benzocyclobutene, a thermosetting polymer, also referred to as BCB) as an adhesive bonding agent. In [30], DVS-BCB was compared to other types of adhesives (photoresist and polyimide) for the bonding of 4-in. silicon wafers. High bonding strength and void-free bonds were obtained with DVS-BCB. This is attributed to the low volume shrinkage of the adhesive. After spin coating of a 1.2-μm-thick DVS-BCB layer, the polymer was

pre-baked to evaporate the solvent. After evaporation, the wafers were joined in a vacuum environment. A bonding pressure of 200 kPa was used to mate both silicon wafers and the wafer stack was cured at 250 °C to obtain a fully polymerized DVS-BCB layer. In [33], 8.3-μm DVS-BCB layers were used to bond 200-mm silicon wafers. DVS-BCB was spray coated onto the silicon surface and the bonding procedure was identical to the previously discussed method. In [30], DVS-BCB was used to bond structured wafer surfaces, using multiple micron-thick bonding layers. Structured silicon wafers were bonded both to unpatterned silicon wafers and Pyrex wafers. Many other papers report on the excellent properties (bonding strength, residual stress, bonding quality) of DVS-BCB bonding [34–36].

For the integration of III-V semiconductors on SOI waveguide circuits using adhesive bonding, DVS-BCB was therefore chosen due to its high bonding strength and superior bonding quality [30], its high degree of planarization, its high resistance to all sorts of chemicals used in standard III-V processing and the fact that no byproducts are created during curing. As will be discussed in a subsequent section, sub-micron-thick bonding layers are required for efficient optical coupling between an SOI waveguide layer and the bonded III-V layer stack. Sub-micron DVS-BCB bonding layer thicknesses were however not yet demonstrated prior to this work and will be discussed later on in this section.

2.2.2. DVS-BCB adhesive

The divinylsiloxane-bis-benzocyclobutene monomer is depicted in Fig. 7. It is a symmetrical molecule consisting of a silicon backbone terminated by two benzocyclobutene rings. The monomer can be B-staged; this means that it
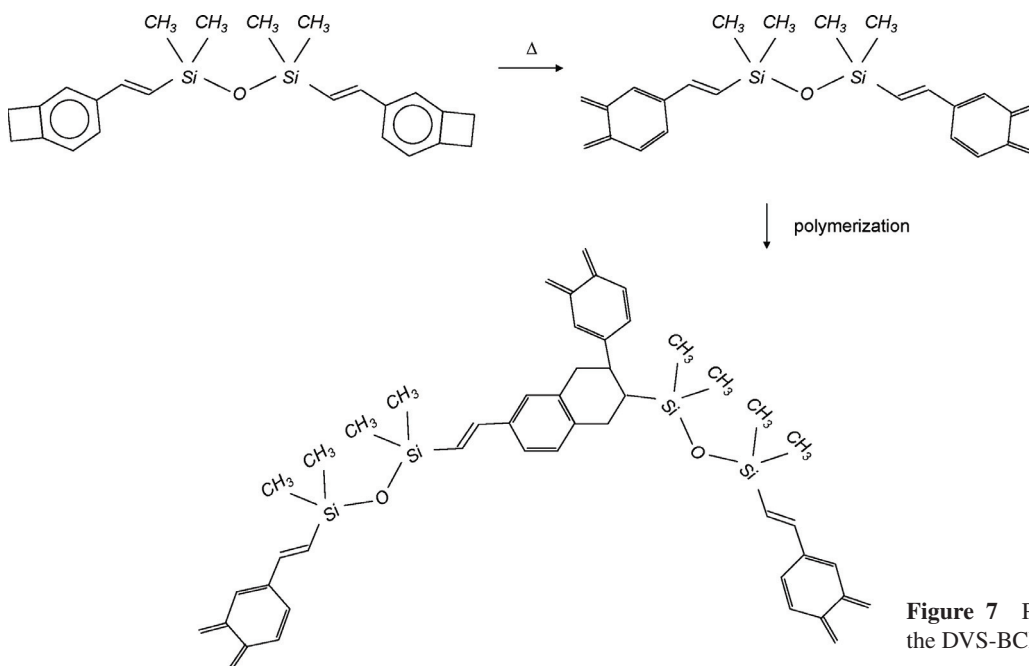

Figure 7 Polymerization reaction of the DVS-BCB monomer.
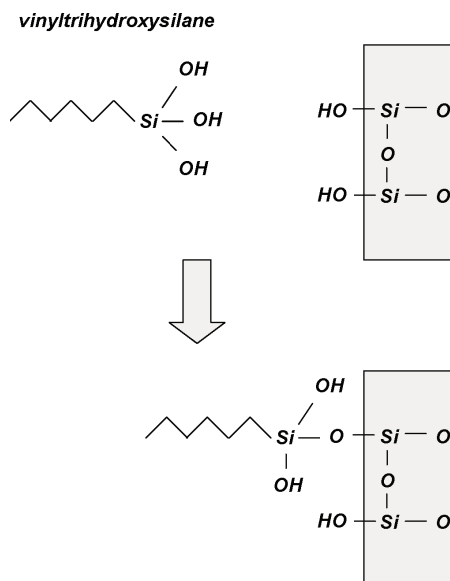
vinyltrihydroxysilane

Figure 8 Operation principle of an adhesion promoter for DVS-BCB.

is partially cured to form an oligomer. An oligomer solution is made by adding mesitylene. The achievable layer thickness by spin coating of the solution is determined by the amount of mesitylene solvent added and the degree of polymerization of the oligomer in the solution. Upon curing, the benzocyclobutene ring thermally opens to form o-quinodimethane. This very reactive intermediate readily undergoes a so-called Diels-Alder reaction with an available vinylsiloxane group to form a three-dimensional network structure as is shown in Fig. 7 [37]. As is clear from this reaction mechanism, no byproducts are created during the polymerization.

Besides the oligomer solution, several adhesion promoter solutions were developed to improve the adhesion of the polymer to a wide range of surfaces. Adhesion promoter molecules for use with silicon wafers often have the generalized chemical formula $G-Si(OR)_3$ [38], where R can be hydrogen, methyl, ethyl or other more complex groups. The resulting silanol group is understood to react with free hydroxyl groups on an oxidized surface. The G-group consists of a moiety with favorable interaction with the polymer. The operation of the simple adhesion promoter vinyltrihydroxysilane on an oxidized silicon surface is shown in Fig. 8.

The electrical, optical, mechanical and thermal properties of DVS-BCB [37, 39] are listed in Table 1. Most important for our application are the low optical loss at telecommunication wavelengths, the low shrinkage upon cure (as this can be the origin of void formation at the bonding interface), its high glass transition temperature (allowing a large post-bonding thermal budget) and its excellent planarization properties. From a device point of view, the major drawback is the low thermal conductivity, which will be discussed later.

Table 1 Various properties of DVS-BCB [37].

Electrical properties	
Dielectric constant	2.5 at 10 GHz
Dissipation factor	0.002 at 10 GHz
Breakdown voltage	5.3 MV/cm
Optical properties	
Refractive index	1.543 at 1.55 μm
Optical loss	< 0.1 dB/cm at 1.55 μm
Mechanical properties	
Tensile modulus	2.9 GPa
Intrinsic stress	28 MPa
Tensile strength	89 MPa
Poisson ratio	0.34
Shrinkage upon cure	0.05
Thermal properties	
Glass transition temperature	> 350 °C
Thermal expansion coefficient	42 ppm/K
Thermal conductivity	0.29 W/mK
Other properties	
Planarization	Very good
Moisture uptake	Very low

Upon curing, the DVS-BCB goes through some transformations at a rate which depends on the temperature used for curing. This can be graphically represented in a time-temperature transformation isothermal cure diagram as shown in Fig. 9 [37]. The main features of such a diagram are obtained by measuring the times for events to occur during isothermal cure at different temperatures. This includes the monitoring of the degree of polymerization and the onset of gelation and vitrification. Gelation corresponds to the incipient formation of an infinite molecular network, which gives rise to long-range elastic behavior in the macroscopic fluid. After gelation, the material consists of normally miscible sol (finite molecular weight) and gel (infinite molecular weight) fractions, the ratio of the former to the latter decreasing with conversion [40].

Vitrification occurs when the glass transition temperature T_g rises to the isothermal temperature of cure. The material is liquid or rubbery when $T_{cure} > T_g$. It is glassy when $T_{cure} < T_g$. Vitrification retards further chemical conversion. The glass transition temperature can be defined as the temperature below which the molecules have little relative mobility. Above T_g, the secondary, non-covalent bonds between the polymer chains become weak in comparison to thermal motion, and the polymer becomes rubbery. Therefore, it can be understood that the glass transition temperature of a polymer increases with increasing degree of polymerization. For fully cured DVS-BCB, the glass transition temperature is about 400 °C.
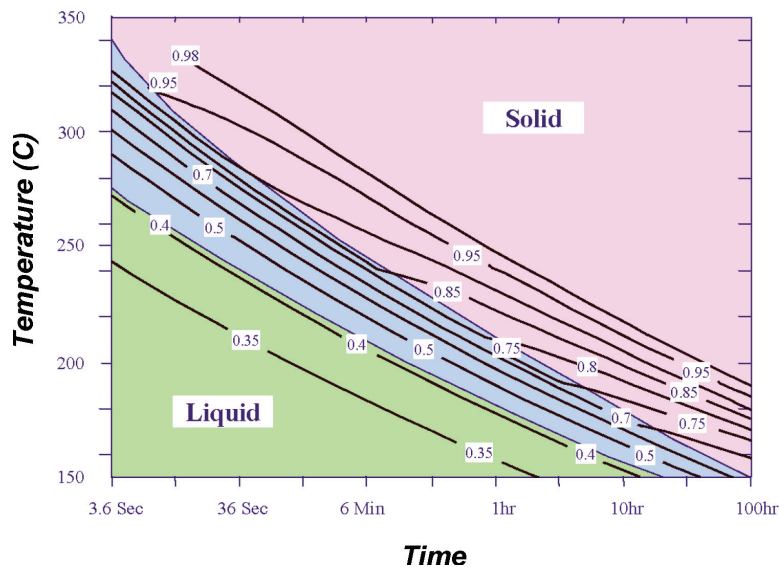
Figure 9 (online color at: www.lpr-journal.org) Time-temperature transformation diagram for DVS-BCB (from [37]).
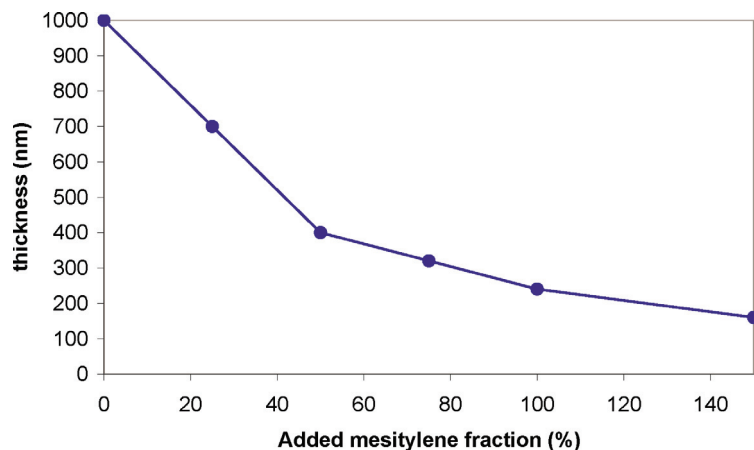

Figure 10 (online color at: www.lpr-journal.org) Influence of the DVS-BCB dilution on the achievable bonding layer thickness.

B-staged DVS-BCB solutions are formulated and commercialized by Dow Chemicals as the CYCLOTENE 3022 product series. It is photoinsensitive, but can be dry etched using a gas mixture of SF_6 and O_2 [41]. The commercially available layer thicknesses range from 1 μm to 25 μm. For the envisaged application of III-V on SOI integration, thinner DVS-BCB layers are required. Therefore, a custom DVS-BCB solution was formulated by adding mesitylene to CYCLOTENE 3022-35. The effect of this dilution on the layer thickness is shown in Fig. 10, in which the resulting layer thickness for a spin speed of 5000 rpm is plotted as a function of the amount of added mesitylene. The use of strongly diluted solutions requires ultrasonic agitation prior to application to obtain reproducible layer thicknesses.

2.2.3. DVS-BCB bonding technology

In order to achieve a good bond, the wafer surface needs to be very clean, since the inclusion of particles at the bonding interface can result in large unbonded areas. While the spin-coated DVS-BCB layer can accommodate some topography on the wafer surfaces, the surface quality requirements become more stringent when the bonding layer thickness is reduced. Obtaining particle-free surfaces is however not easily achieved. Especially large particles can occur on the surface due to cleaving or dicing of the dies. Moreover, hydrocarbon contamination (due to storage in plastic boxes and exposure to air) on the die surface can reduce the adhesion of the DVS-BCB and thereby decrease the bonding strength. Wafer cleaning and substrate preparation are therefore of paramount importance. The cleaning of the substrate depends on the type of substrate. Hydrocarbon contamination can be removed from the silicon-on-insulator dies by immersing the sample in a Piranha solution, a warm mixture of $3H_2SO_4:1H_2O_2$. The mixture is a strong oxidizer and will remove most organic matter and leave the surface hydrophilic. In a second step particles can be removed by using a Standard Clean 1 solution, which is a mixture of NH_4OH, H_2O_2 and H_2O. This is an alkaline solution, capable of removing particles and organic materials. For particles, it primarily works through oxidation of the particles and electrical repulsion. H_2O_2 is a powerful oxidizing agent that oxidizes the wafer surface and the particles. The

NH$_4$OH slightly etches the wafer surface and undercuts beneath the particles. This can lift off the particles from the surface. Actually, an electrical repulsion of the particles is achieved. The NH$_4$OH builds up a negative charge on the particles and the wafer surface, which serves to repulse the particles from the surface.

After surface cleaning, the commercially available adhesion promoter AP3000 is applied by spin coating. It was found that the cleaning of the InP/InGaAsP dies can best be done by removing a pair of sacrificial InP/InGaAs layers by selective wet etching using the etchants 3HCl:H$_2$O and 1H$_2$SO$_4$:3H$_2$O$_2$:1H$_2$O, respectively. This etch lifts off foreign particles and etches down and lifts off InP/InGaAsP particles, created by the cleaving or dicing operation. No adhesion promoter is applied to the III-V surface, as this would require spin coating of the individual cleaved dies, which is very time intensive and leads to the formation of an edge bead.

After surface cleaning and conditioning, the DVS-BCB is deposited on the silicon-on-insulator wafer surface by spin coating. Although most of the mesitylene solvent already evaporated during the spin-coating process, some solvent is still remaining in the spin-coated film, which is evaporated by a thermal treatment at 150 °C for 1 min. This thermal treatment also causes a reflow of the DVS-BCB, which improves its planarizing properties.

After cleaning, surface conditioning and thermal treatment of the DVS-BCB layer, both samples are brought into contact. Attachment is done at 150 °C, as DVS-BCB has about the lowest viscosity at this temperature [36] and keeping the DVS-BCB at this temperature does not significantly increase the degree of polymerization for at least an hour (see Fig. 9).

The attachment of the III-V die onto the SOI waveguide circuit can be done in clean room air, by using tweezers to attach the die to the host substrate. This approach can result in the incorporation of air pockets at the bonding interface, making the bonding process less reproducible. Therefore, we are currently investigating the use of commercial wafer-bonding solutions to transfer the III-V epi structure in a vacuum-bonding chamber.

After attachment of the III-V die, the DVS-BCB film has to be cured. The curing has to be performed in an atmosphere containing less than 100 ppm oxygen, to prevent the oxidation of the DVS-BCB. To achieve this, nitrogen is purged through the curing chamber. The rapid thermal curing of DVS-BCB has also been reported in the literature [37] using peak temperatures as high as 315 °C and cure cycle times lower than 5 min. Although this works fine for as-deposited DVS-BCB layers, rapid thermal annealing of DVS-BCB used as a bonding agent always resulted in delamination and failure of the III-V/SOI bond in our experiments. This is probably related to the fact that an intimate contact between the DVS-BCB and the bonded die (through wetting) can only be achieved by slowly polymerizing the DVS-BCB.

After bonding of the InP/InGaAsP die, the InP substrate needs to be removed, to be able to access and process the InP/InGaAsP epitaxial layers. The InP substrate can be removed by complete wet chemical etching or by using a combination of mechanical grinding and wet chemical etching. Complete chemical etching can be done using a mixture of HCl and H$_2$O. High etch rates can be obtained by using pure HCl. Although this leads to the shortest etching time, the use of pure HCl should be avoided, as the etching is vigorous and lots of gas bubbles are created. These can stick to the substrate and thereby mask the etching, which causes etching inhomogeneity. A good compromise between etching speed and etching quality is to use a 3HCl:1H$_2$O mixture. An InGaAs etch stop layer can be used, which shows nearly complete etching selectivity to InP. It was found, however, that an important drawback of complete chemical etching using a HCl:H$_2$O etching solution is the arising of unetched ramps at two sides of the cleaved InP die due to the exposure of the (112) crystallographic plane, which forms an angle of about 35 degrees with the surface [42]. This is due to the fact that HCl is an anisotropic etchant and does not etch an exposed $(01-1)$ plane. This plane is exposed by the cleaving of the dies. The origin of the ramps is graphically explained in Fig. 11. These ramps prohibit a good contact between the mask and sample in the post-processing lithography, making the
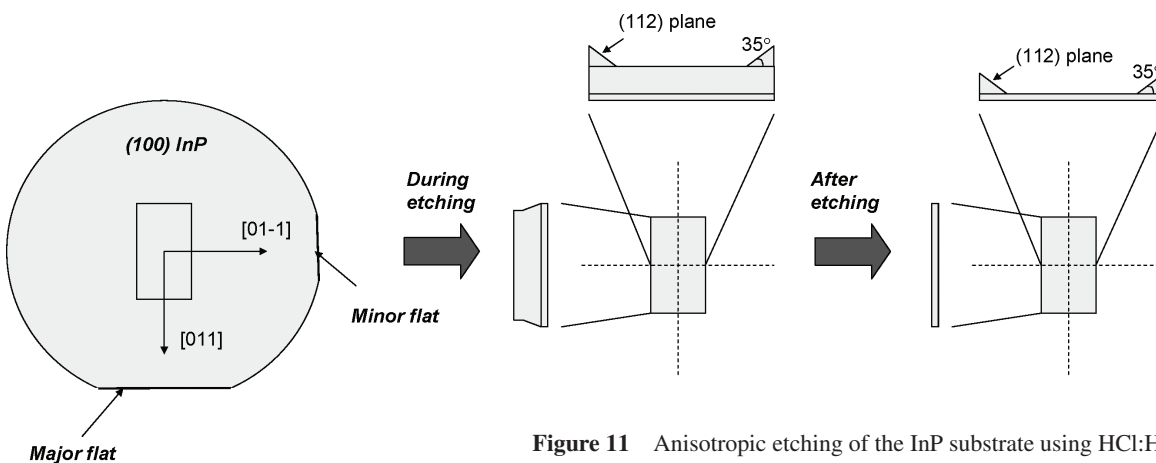

Figure 11   Anisotropic etching of the InP substrate using HCl:H$_2$O solutions.

definition of fine features difficult for contact lithography. As no isotropic but selective etching solution for InP is known, a combination of isotropic non-selective etching and anisotropic selective etching can be used to avoid the formation of the ramps. We successfully used a combination of HNO_3:HCl and 3HCl:H_2O to avoid the formation of the ramps. Good timing for changing the etch bath is needed in order to prevent the etching of the InP/InGaAsP epitaxial layers by the non-selective HNO_3:HCl etchant.

Based on this bonding technology, a wide range of bonding layer thicknesses can be achieved, ranging from μm-thick bonding layers, over hundreds of nanometers bonding layer thicknesses down to 50-nm-range bonding layer thicknesses as shown in Fig. 12.

3. III-V/silicon light emitters for on-chip optical interconnect

3.1. Introduction

As discussed in Sect. 1, it is expected that in future high performance processor systems the only viable technology for transmitting the huge amount of information is using optical interconnects exploiting wavelength-division multiplexing. The requirements for a light source in such an optical interconnect system is very different for on-chip and off-chip communication. In on-chip communication the device footprint and the power dissipation are of paramount importance, while the optical output power can be on the order of a few tens of micro-watts. These output power levels are achievable using micro-laser sources, with typical dimensions on the order of 10 μm. In this section we will describe the design, fabrication and characterization of micro-disk laser diodes for on-chip optical interconnect networks. Both single-wavelength sources and multi-wavelength sources consisting of an array of micro-disk lasers will be described. In the subsequent section III-V/silicon light emitters for chip-to-chip optical interconnects will be discussed.

3.2. Single micro-disk laser

3.2.1. Device structure

Micro-disk lasers have attracted much interest due to the compact size and low threshold current [26, 43–45], which are very important figures for the application of on-chip interconnects. Bonded micro-disk lasers, which are either electrically pumped but not coupled to a passive waveguide (stand alone) [43–45], or coupled to an SOI waveguide but only optically pumped [26], have been reported recently. We have proposed a heterogeneously integrated micro-disk laser structure with all the above functionalities [46].

The proposed micro-disk laser (MDL) structure and some pictures of the fabricated devices are shown in Fig. 13. The laser III-V die was first bonded on top of a single-mode
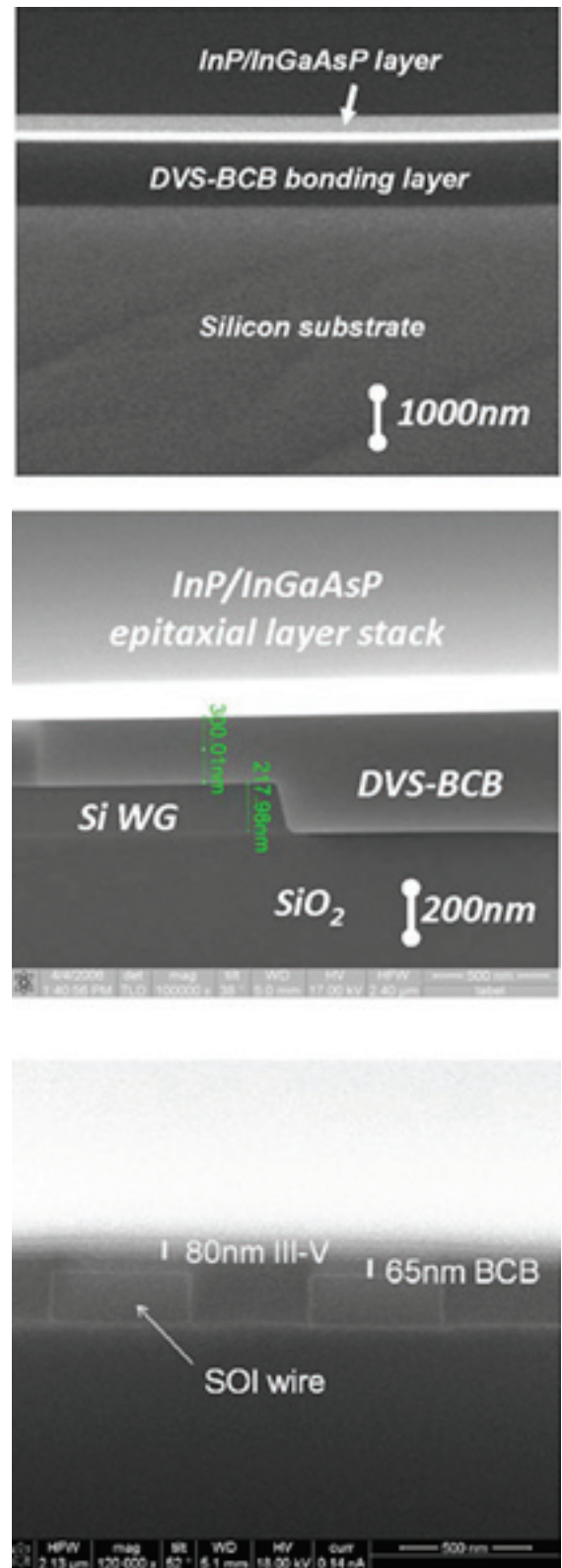

Figure 12 (online color at: www.lpr-journal.org) Versatility of the DVS-BCB bonding approach: range of bonding layer thicknesses that can be achieved.
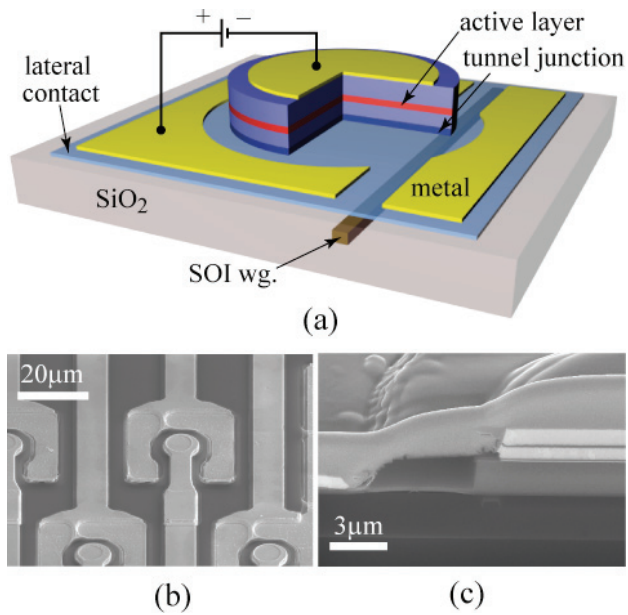
Figure 13 (online color at: www.lpr-journal.org) (a) Sketch of the proposed micro-disk laser. (b) Bird's-eye view of some fabricated lasers. (c) Cross-sectional picture of a fabricated laser.

SOI waveguide (dimensions: 500 nm × 220 nm) by either SiO$_2$ direct bonding (at CEA-LETI in France) or DVS-BCB adhesive bonding. The total thickness of the III-V die is about 1 μm. Please refer to [46] for the detailed layer structure. The SOI waveguide is terminated with grating fiber couplers for interfacing to single-mode fibers. The micro-disk pattern was defined usually by e-beam lithography in order to ensure a fine alignment of the SOI waveg-

uide to the edge of the micro-disk cavity. The etching of the III-V layer was done by a commercial ICP-RIE tool with CH$_4$/H$_2$ chemistry. The etching depth was in-situ controlled with laser interferometry, and a thin slab of n-InP layer remained for the lateral electric contact. This lateral contact layer was etched away where it is not needed. The resonant mode of the micro-disk cavity is the whispering gallery mode (WGM) confined at the periphery of the disk. Fig. 14 shows the E_r field distribution (radial electric field) of several TE-polarized WGMs. The TE$_{00}$ mode, also the fundamental mode in both vertical and radial directions, is designed to be the lasing mode, by designing the layer stack such that this mode has the highest confinement factor in the QWs and the lowest losses due to the presence of the metallization and doped/absorbing semiconductor layers. Three compressively strained InAsP quantum wells embedded in unstrained InGaAsP barrier layers (with a band-gap wavelength of 1.2 μm – also referred to as Q1.2) were employed to provide gain for TE polarization. As compared to InGaAsP or InGaAs quantum wells, the surface recombination rate of InAsP QWs is believed to be lower. In order to ensure a low lateral radiation loss of the WGM, a deeply etched structure through the QW layers was employed in our design. Therefore, the surface recombination rate has a crucial impact on the laser performance. A high surface recombination rate will result in a serious depletion of the injected electrons and holes near the edge of the disk where the lasing mode is located, and hence in a high laser threshold current. The epitaxial layer structure was grown at INL, France. After the etching of the disk structure, a BCB layer (not shown in Fig. 13a) was spun on top of it for electrical isolation. Vias were then opened at the center of the disk and on the lateral contact layer, where two metal contacts were deposited. A tunnel junction consisting of
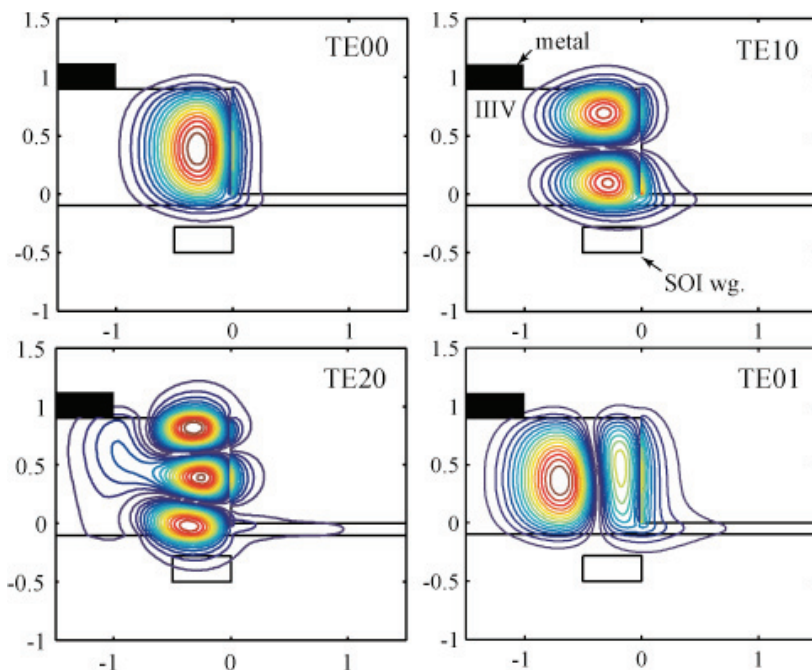

Figure 14 (online color at: www.lpr-journal.org) Four lowest-order WGMs supported in the micro-disk cavity with a diameter of 7.5 μm. Axis unit: μm.

a 20-nm heavily doped p-Q1.2 layer and a 20-nm heavily doped n-Q1.2 layer is employed for hole injection, since the conventional InGaAs-based p-type contact scheme gives a high optical loss due to the large inter-band absorption of the InGaAs material. Additionally, the tunnel junction based contact can provide a uniform current distribution across the whole disk area. The distance from the edge of the III-V disk to the top metal contact has be to be carefully designed. A too small distance will give an extra absorption loss for the lasing mode, while a too large distance will result in less contact area of the top metal, and hence a higher contact resistance. Other important parameters, including the thickness of the lateral contact layer, distance between the disk and the SOI waveguide, doping levels of the III-V layers, etc., also need to be systematically optimized concerning the optical and electrical properties. A detailed discussion about the optimization procedure under static conditions can be found in [47].

3.2.2. Static lasing performance

Fig. 15 shows the lasing characteristics of an MDL fabricated using SiO_2 direct bonding with 10-μm diameter under continuous driving conditions. The distance between

the disk and the SOI waveguide is measured to be 180 nm. The free spectral range (FSR) of the cavity resonance is about 24 nm in this case. Single-mode lasing was obtained as shown in Fig. 15a, with a side mode suppression ratio of about 22 dB. The light current-voltage (LIV) relation of the MDL is plotted in Fig. 15b. The threshold current is 1.0 mA and the threshold voltage is about 1.1 V. These figures are still high, as 40-μA threshold current has been achieved for a stand-alone InP micro-disk laser [44]. Although a coupled (to an output waveguide) micro-disk laser should intrinsically have a higher threshold than that of a stand-alone one, the threshold current here, we believe, is still limited by the scattering loss caused by the sidewall roughness. By optimizing the lithography and etching processes, further improvement should be feasible. The lasing powers measured at the two ends of the SOI waveguide are approximately equal. This means that the MDL actually works in the bi-directional regime, where both the clockwise and the counterclockwise propagation of the WGM exist [48]. Although the output lasing power reaches 100 μW under pulsed operation, it is limited to about 10 μW under continuous-wave (CW) operation, due to the early thermal roll-over. Fig. 16a shows the lasing spectra at different bias currents. An obvious red shift of
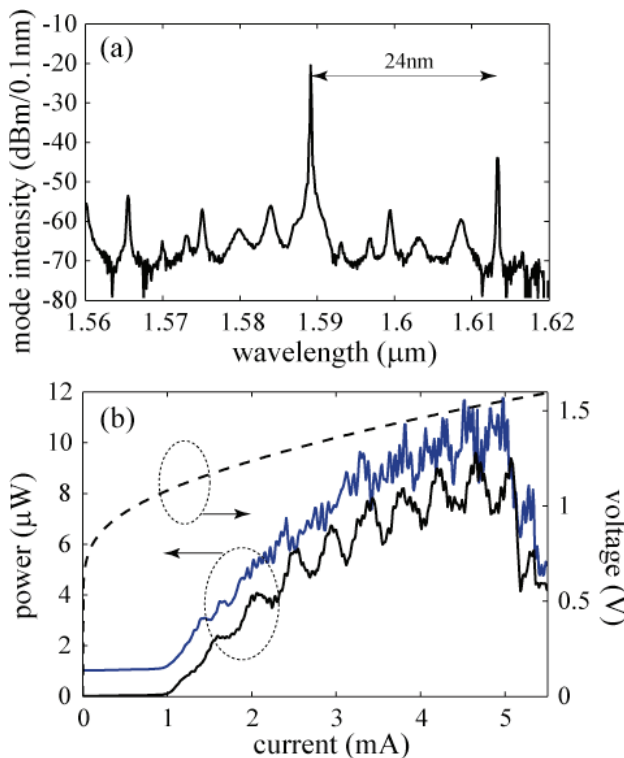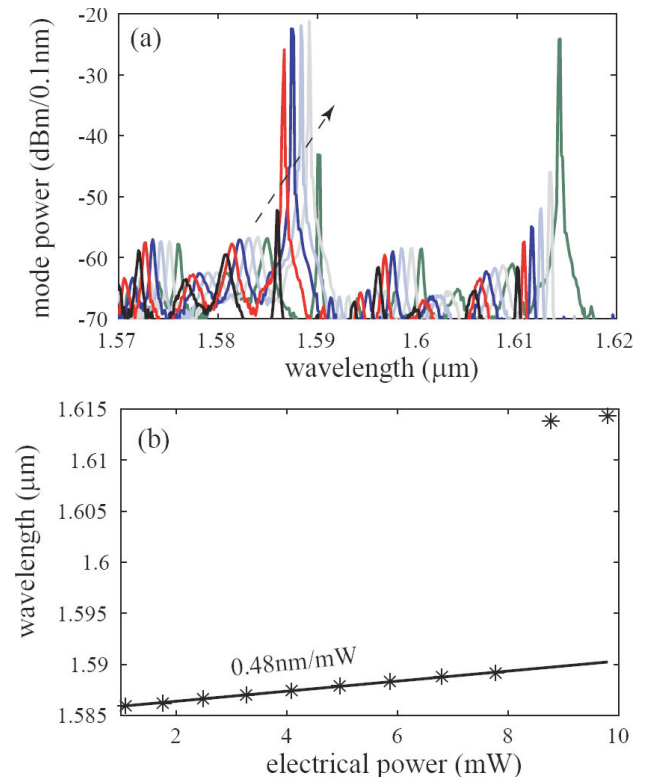

Figure 15 (online color at: www.lpr-journal.org) (a) Lasing spectrum of a 10-μm MDL at a bias of 4.8 mA. (b) LIV curves of the same laser. The dashed line indicates the voltage; the solid lines indicate the optical power towards the two ends of the SOI waveguide. The blue solid line is offset by 1 μW for clarity.

Figure 16 (online color at: www.lpr-journal.org) (a) Spectra obtained with different bias currents of the micro-disk laser. Along the arrow direction, the corresponding bias current increases from 1.0 to 6.0 mA with a step of 1.0 mA. (b) Peak lasing wavelength as a function of the applied electrical power.

the resonance can be observed due to self heating. The relation between the peak lasing wavelengths and the applied electrical power is plotted in Fig. 16b. The shift rate is extracted to be 0.48 nm/mW. Assuming the 0.1 nm/K variation of the resonant wavelength with respect to the temperature [49], the thermal resistance of the micro-disk structure can also be calculated to be 4.8 K/mW, which is consistent with the simulation results [49]. A sudden jump of the peak lasing wavelength can be found around 8-mW electrical power consumption, which results from the red shift of the peak gain wavelength of the QW at elevated temperature. This also corresponds to the sudden drop of the lasing power beyond 5.2 mA shown in Fig. 15b, since the lasing wavelength under this bias is outside the efficient coupling regime of the grating coupler used to couple the waveguided light to the optical fiber. The oscillations in the LI curve presented in Fig. 15b probably result from the shift of the lasing wavelength with increased bias and the reflection feedback from the grating couplers (calculated to be about -22 dB). Assuming that the period of the oscillation corresponds to a feedback phase shift of 2π and assuming a group index of 4.0 for the SOI waveguide, we can extract the physical distance between the grating couplers and the micro-disk laser to be $\sim 6500\,\mu$m (the fast oscillation) and $\sim 700\,\mu$m (the slow oscillation). This matches with the device layout, and also confirms our assumption. Generally, this phenomenon should not be a problem for practical on-chip interconnects since no grating couplers are needed in this case, but the back reflections from other devices involved in the communication link should be avoided as much as possible.

MDLs through DVS-BCB adhesive bonding were also prepared and tested. Continuous-wave lasing operation was obtained. Fig. 17 shows the lasing spectrum and the LIV curve of such a MDL with a diameter of 7.5 µm. The FSR is about 32 nm in this case. The threshold current and voltage are 0.8 mA and 1.3 V, respectively. By using a light field SOI mask, the distance between the disk and the waveguide was pushed down to about 20 nm in this device, which results in a higher outcoupling efficiency as compared to the SiO$_2$ direct bonded MDL discussed in Fig. 15. Therefore, the peak lasing power reaches 29 µW as shown in Fig. 17. The oscillation phenomenon in the LI curve is still present, but with a larger period, since the distance between the grating couplers and the MDL is much shorter ($\sim 200\,\mu$m) in this processed device. Although the thermal conductivity of BCB (0.3 W/mK) is less than that of SiO$_2$ (1.2 W/mK), the thermal resistance of the whole device was measured to be similar as that of the SiO$_2$ bonded ones, since the dominant thermal resistance comes from the thick BOX layer (1–2 µm) of the SOI chip. We are now exploring the possibility of creating a thermal short circuit between the disk volume and the Si substrate, e.g. by etching a via through the bonding layer and BOX layer and depositing a thick metal connection between the micro-disk and the substrate. Simulation shows that the thermal resistance can be decreased by a factor of five by this means.
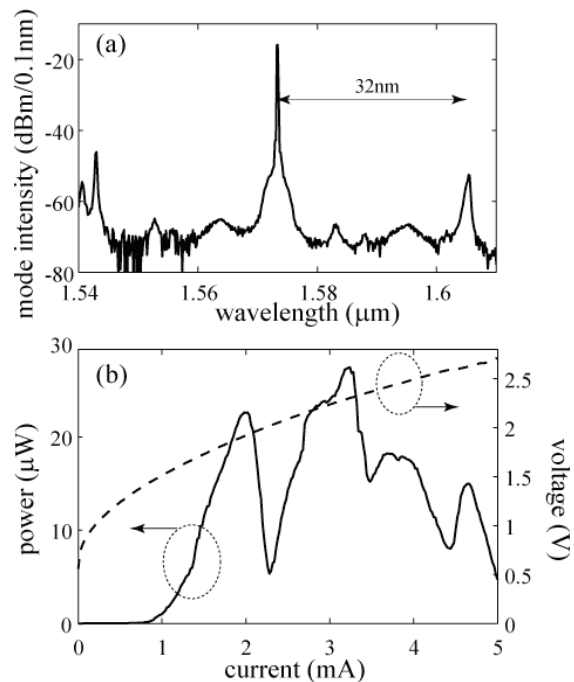

Figure 17 (a) Lasing spectrum of a 7.5-µm MDL through DVS-BCB adhesive bonding at a bias of 3.2 mA. (b) LIV curves of the same laser.

3.2.3. Dynamic response

The dynamic response of an MDL is an important characteristic, as the direct modulation of the bias current is the easiest and most compact way to imprint a data pattern onto the laser beam. Fig. 18a shows the typical small signal modulation response of a 7.5-µm-diameter MDL. The 3-dB bandwidth is about 3.5 GHz. The large signal modulation response is also plotted in Fig. 18b, where the MDL was modulated with a periodic square-wave signal at 1.5 GHz (3.0 Gbps). Here, the low level of the driving signal was slightly above threshold, and the high level was at the current giving the highest power. No significant overshoot is observed. The extinction ratio of the optical signal is 10 dB after the amplification by an Er-doped fiber amplifier (EDFA). The rise and fall times are 110 ps and 150 ps, respectively. The bit-error rate is still modest in this case since too much noise is introduced due to amplification of such a weak signal (e. g. 10 µW in the SOI waveguide, 2 µW coupled to the fiber). It is believed that the data-transmission performance should be improved by using an on-chip photodetector, where the coupling loss can be avoided.

3.3. Multi-wavelength micro-disk laser array

3.3.1. Structure and static performance

WDM technology enables us to dramatically increase the communication capacity of a single link. It can also be
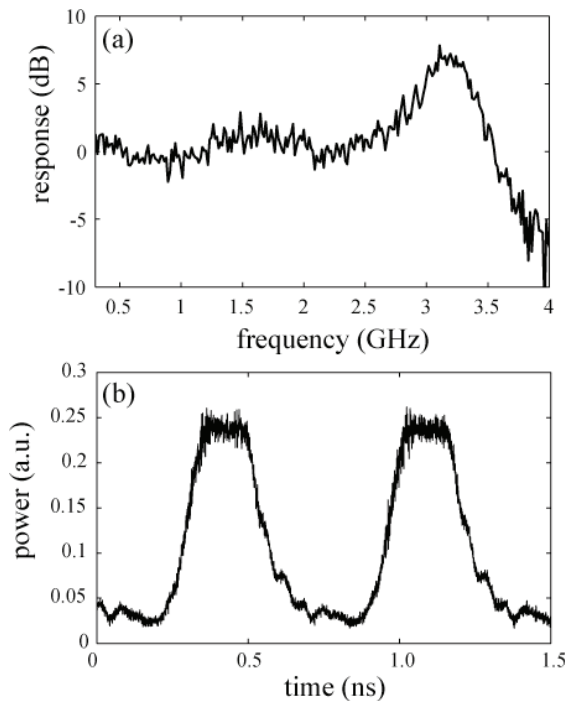
Figure 18 (a) Small signal modulation response of a 7.5-μm-diameter MDL. (b) Large signal modulation response of the same laser with periodic square-wave electrical driving signal at 1.5 GHz.

Figure 19 (online color at: www.lpr-journal.org) (a) Fabricated multi-wavelength laser before metallization, composed of four MDLs on one SOI bus waveguide. The arrows indicate the directions towards the grating couplers. Spectra when monitoring from the left (b) and right (c) grating couplers. The bias current is 3.5 mA.

used as a routing method for the communications between different cores within one chip. In this case, a laser source which can emit several wavelength signals preferably at an equal spacing is required. This sort of multi-wavelength laser (MWL) source can be realized by cascading several micro-disk lasers on one SOI bus waveguide as shown in Fig. 19a [50]. Fig. 19b and (c) show the spectra recorded from the two ends of the SOI waveguide, when the four micro-disk lasers were simultaneously biased at the same current. It can be seen that the emitting wavelengths are equally distributed within one FSR of an individual micro-disk laser. This is matched with the design, where the difference in diameter between adjacent disks is 44 nm, which theoretically corresponds to a laser peak shift of $\lambda_{FSR}/4$. Note that, in the measured spectra, the dominant peak powers of the lasers show about 10-dB fluctuation. The micro-disk laser that is closer to the grating coupler generally has a higher output power level (cf. the disk number on each of the laser peaks and the corresponding position in Fig. 19a). This non-uniformity is due to the leakage losses to the neighboring micro-disks when light passes under them on its way to the grating couplers. As discussed above (cf. Fig. 14), the micro-disk structure supports several high-order modes, and the coupling coefficient to these modes is much larger than that to the lasing mode (TE_{00}) due to the larger field overlap and better phase matching with the mode in the SOI waveguide. Fig. 20 shows the transmission spectrum through the SOI waveguide of one unbiased
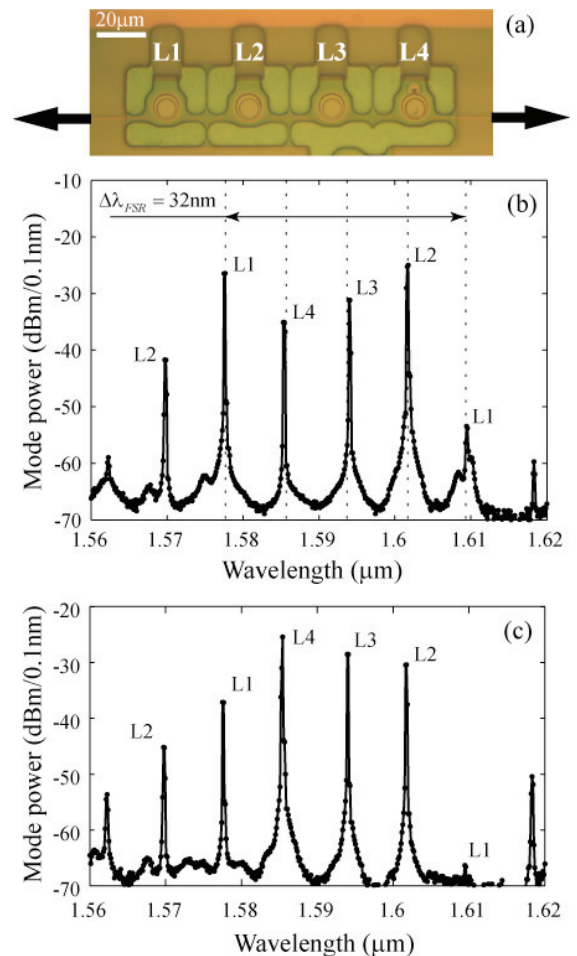
micro-disk laser. From this picture, we can find that the overall transmission is about -3 dB, which explains the stepwise 3-dB decrease of the lasing peak powers when the corresponding micro-disks are located further away from the grating coupler. Secondly, there exist multiple dips in the transmission curve, which is evidence of the coupling to the high-order modes and their resonances inside the micro-disk cavity. Obviously, these resonances impose an additional ~ 4–6 dB loss at the resonant frequencies. We will further discuss the impact of this phenomenon on the performance of the multi-wavelength lasers in the following paragraph. The emitted power of the lasing peaks can be made uniform by adjusting the bias current to each micro-disk. The result is shown in Fig. 21. However, this approach might become unrealistic for MWLs with a large number of channels, as the non-uniformity scales directly with the number of micro-disks included in the device. An alternative solution to this problem is to decrease the III-V layer
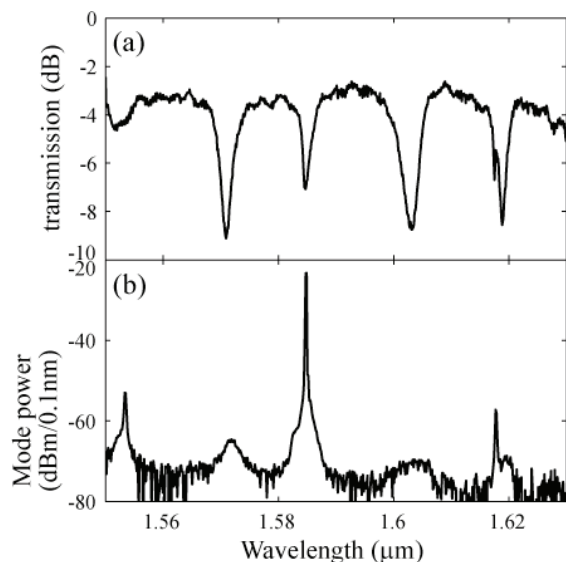
Figure 20 (a) Transmission spectrum of an unbiased micro-disk laser with diameter of 7.5 μm. (b) Lasing spectrum of the laser at 2.0-mA bias showing the correspondence between the resonant peaks here and the dips in (a).
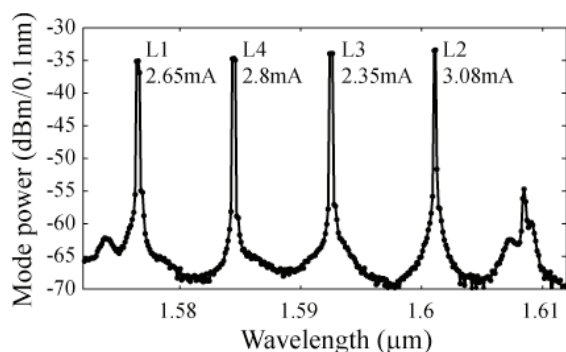

Figure 21 Balanced output spectrum obtained by adjusting the individual micro-disk drive currents.

thickness (e.g. to about 300 nm) so that single-mode operation is ensured in the vertical direction. Numerical simulations suggest that 0.1-dB insertion loss can be achieved with this approach. However, designing an efficient p-i-n structure in this thin III-V layer, while keeping a reasonable optical loss, is still challenging.

3.3.2. Thermal crosstalk

The crosstalk of the present MWL was also tested by varying the bias current of one micro-disk laser and recording the whole spectrum while keeping the drive conditions of the other lasers unchanged. An example of such a measurement is shown in Fig. 22. It is obvious that the lasing wavelength of the corresponding micro-disk shifts clearly when changing the drive current due to self heating, similar
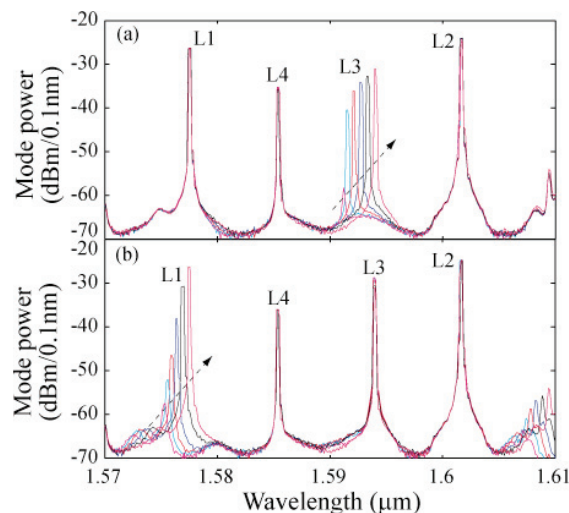

Figure 22 (online color at: www.lpr-journal.org) Spectra obtained with different bias currents of one micro-disk laser (a) for L3 and (b) for L1. Along the arrow direction, the corresponding bias current increases from 1.0 to 3.5 mA with a step of 0.5 mA. The other three micro-disk lasers are all biased at 3.5 mA.

to what we have discussed for a single MDL. However, for the other three micro-disk lasers, the lasing wavelengths remain unchanged (at least within the resolution limit of the spectrum analyzer, i. e. 0.1 nm), which means that the thermal crosstalk is negligible, even though the distance between adjacent micro-disks is only 33 μm (see Fig. 19a). Generally, the peak intensities of the other micro-disk lasers are also stable, but in some cases they can vary by several decibels, e.g. the L3 peak in Fig. 22b. This can be explained with the transmission curve presented in Fig. 20. For some combinations of micro-disk drive currents, a lossy higher-order mode of a disk located closer to the grating coupler can get spectrally aligned with the lasing mode of another micro-disk positioned further away. In that case, the measured output power of the latter will be affected through this resonance dip. This effect can also be eliminated by reducing the thickness of the micro-disk lasers.

4. III-V/silicon light emitters for chip-to-chip optical interconnects

4.1. Introduction

While the micrometer-scale lasers discussed in the previous section are small-footprint devices with output power levels compatible with intra-chip optical interconnect applications, these devices are less suitable for off-chip communication. Higher output power devices are typically required for that purpose. In this section we will describe the realization of III-V on silicon light sources suitable for off-chip optical communication. Both DVS-BCB bonded laser diodes (Fabry-Perot laser diodes) and direct bonded laser

diodes (single-wavelength and multi-wavelength mode-locked laser sources for WDM applications) will be described. The DVS-BCB bonded Fabry-Perot laser diode relies on a classical design, where the laser mode is guided by the III-V waveguide structure and then an adiabatic taper structure is used to efficiently couple the light into the SOI waveguide circuit. In the case of the direct bonded laser diodes, a III-V/silicon hybrid mode concept is used, in which the mode is confined by the silicon waveguide, while the overlap with the III-V gain region provides the gain. We will elaborate more on this concept in Sect. 4.3.1.

4.2. DVS-BCB bonded Fabry-Perot laser diodes

As a first demonstration of the viability of milliwatt level output power laser diodes, heterogeneously integrated on a silicon-on-insulator waveguide structure, a thin-film Fabry-Perot laser diode bonded on and coupled to an underlying SOI waveguide circuit was realized [51]. The DVS-BCB die-to-wafer bonding approach was used for this purpose. In order to efficiently couple light between the InP/InGaAsP laser diode (in which the lasing mode was completely confined) and the SOI waveguide layer, a coupling scheme based on an inverted adiabatic taper approach as shown in Fig. 23 was used.

In this coupling approach, the laser mesa is butt coupled to a polymer waveguide. Underneath this polymer waveguide, an inverted taper in the SOI waveguide layer is used to adiabatically transform the polymer waveguide mode to the SOI waveguide mode. In this way very efficient and broadband coupling can be obtained. The polymer waveguide consists of a polyimide waveguide core ($n = 1.67$) surrounded by a DVS-BCB cladding ($n = 1.54$). The InP/InGaAsP layer stack used for the Fabry-Perot laser diodes is shown in Table 2. It consists of a six InGaAsP quantum well based active region. The polyimide waveguide was designed in such a way to obtain maximal coupling efficiency with the laser mode. Full vectorial eigenmode expansion calculations show that the losses at the III-V/polymer interface can be kept below 1 dB for a polyimide waveguide height of 1.3 μm (for a 3-μm-wide mesa).

The fabrication cycle of the active devices is outlined in Fig. 24. The epitaxial layers were transferred using the adhesive bonding approach outlined in Sect. 2.2.3. A DVS-BCB bonding layer of 300 nm was chosen in the design. After bonding and substrate removal, the laser cavity facets were etched using dry etching in a CH_4:H_2/O_2 plasma. A 100-nm-thick Ti hard mask was used for the 3.2-μm-deep etch. After facet etching a polyimide layer (1.3-μm thickness) was spin coated on the waveguide circuit and it was again selectively removed on top of the formed III-V is-
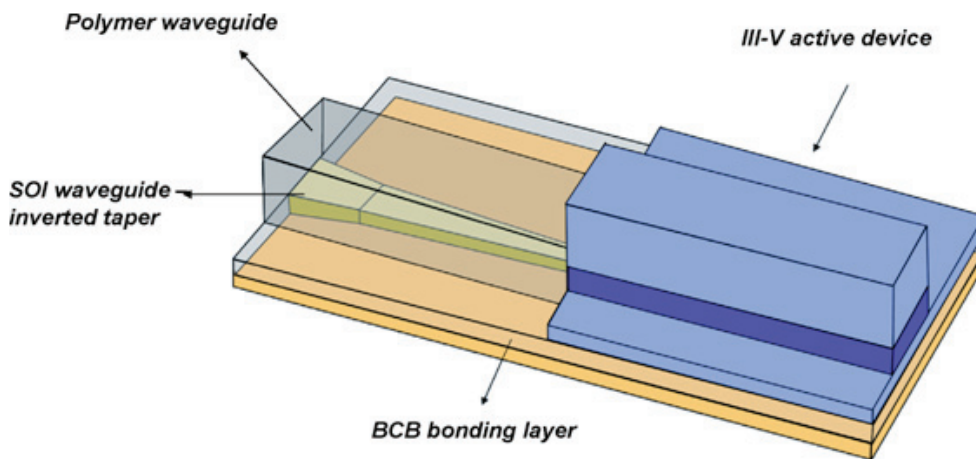

Figure 23 (online color at: www.lpr-journal.org) III-V/SOI coupling scheme based on an inverted taper coupler structure.

Table 2 Epitaxial layer structure for the fabrication of bonded laser diodes.

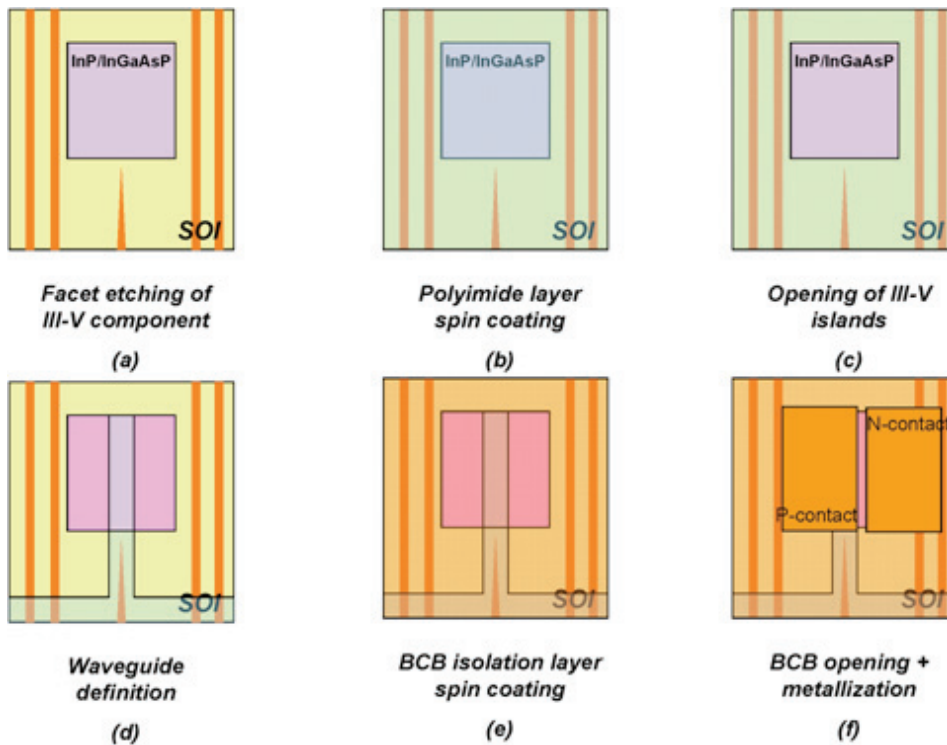| Material	Thickness	Doping
InP	600 nm	n-type 10^{18}
InGaAsP ($\lambda = 1.25$ μm)	150 nm	n.i.d.
4 × quantum wells ($\lambda = 1.55$ μm)	2.25 nm	n.i.d.
3 × InGaAsP barriers ($\lambda = 1.25$ μm)	10 nm	n.i.d.
InGaAsP ($\lambda = 1.25$ μm)	150 nm	n.i.d.
InP	150 nm	n.i.d.
InP	1850 nm	p-type 4×10^{17}
InGaAs	150 nm	Heavily p-type doped
InP	50 nm	Not relevant
InGaAs	150 nm	Not relevant
InP substrate	Not relevant	Not relevant

Figure 24 (online color at: www.lpr-journal.org) Fabrication procedure for DVS-BCB bonded laser diodes.

lands. This approach allows for the self-aligned definition of the laser mesa and the polymer waveguide structure of the adiabatic taper. Both the laser mesa and polymer waveguide are defined using a single CH_4:H_2/O_2 plasma. The laser ridges are etched through the active layer to be able to access the n-type contact layer. The polyimide waveguide was completely etched through. After the etching of the III-V and polymer waveguide, a DVS-BCB layer is coated on the waveguide structure and openings are defined for the TiAu p-type contact and the AuGeNi n-type contact. Rapid thermal annealing at 400 °C was carried out to achieve ohmic contacts. All alignment was done lithographically to the underlying SOI features. A top view of the fabricated structure is shown in Fig. 25.
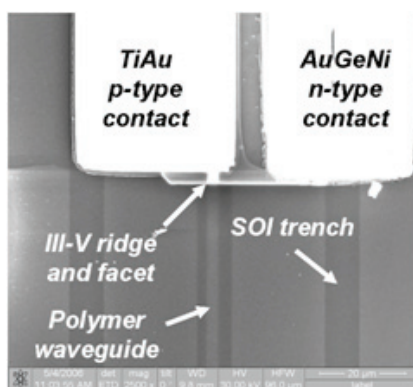

Figure 25 SEM top view of the fabricated laser diodes: the laser diode mesa and polymer waveguide can be clearly seen. The SOI inverted taper is buried underneath the laser mesa.

Laser emission was observed from these bonded devices under pulsed operation. Up to 1 mW of output power was coupled into the SOI waveguide layer. A high threshold current density of 10.4 kA/cm^2 was required to achieve lasing. This is most probably related to the quality of the etched facets and the surface recombination in the active region, since the laser mesa was etched through the active layer. No continuous-wave operation could be obtained for these devices due to the low thermal conductivity of the DVS-BCB bonding layer and the underlying SiO_2 buried oxide layer, resulting in substantial self heating of the device. This problem can be circumvented by integrating a heat-sink structure on the laser diode by using the metal contacts as a heat sink through the bonding layer. This was demonstrated for DVS-BCB bonded Fabry-Perot lasers bonded with a 2-μm-thick layer to a carrier substrate. By connecting the plated gold top contact to the host substrate, through the bonding layer, efficient heat sinking can be achieved, provided that the plated gold top contact is sufficiently thick. A SEM image of the fabricated device is shown in Fig. 26. The thick DVS-BCB bonding layer was chosen in order to demonstrate the efficiency of the heat-sinking structure. The laser ridge is 10-μm wide and is located 20-μm away from the thermal via. 700-μm-long laser bars were used in the experiment. Continuous-wave operation of these devices at room temperature was obtained. Still, a considerable thermal resistance remains, which prevents lasing at higher ambient temperatures. The thermal resistance can however further be reduced by using narrower laser stripes and thinner DVS-BCB bonding layers.

Besides the DVS-BCB bonded Fabry-Perot laser diodes coupled to the underlying SOI waveguide circuit, other re-
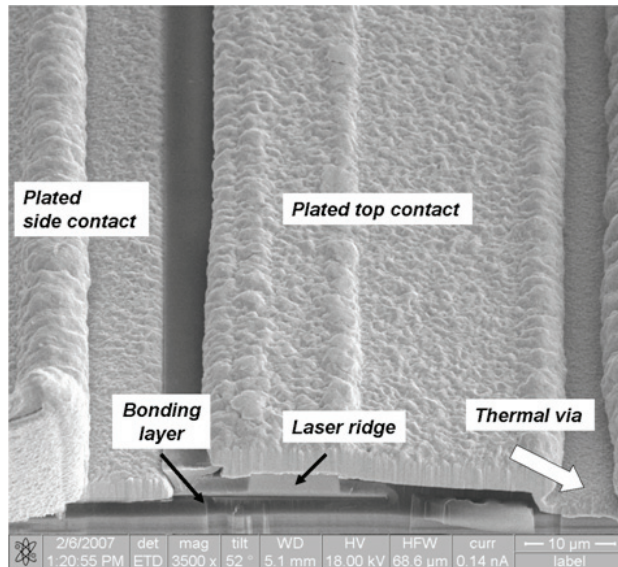
Figure 26 SEM view of the DVS-BCB bonded Fabry-Perot laser diode with an integrated heat-sink structure.

ports can be found in the literature on heterogeneously integrated Fabry-Perot lasers [52, 53]. These devices however are stand-alone devices, not coupled to an underlying SOI waveguide circuit.

4.3. Direct-bonded single-wavelength laser diodes

4.3.1. Silicon evanescent laser devices

Fig. 27 shows the general structure of hybrid silicon devices based on the direct III-V to silicon bonding technology. The hybrid structure comprises a III-V region bonded to a silicon waveguide fabricated on an SOI wafer prior to III-V epitaxial transfer. The mesa structure formed on the III-V region enables the current flow through the multiple quantum well region. The general structure of III-V layers consists of a p-type contact layer, a p-type cladding, a p-type separated confinement heterostructure (SCH) layer, an undoped multiple quantum well layer, an n-type contact layer and n-type superlattices. Amplifiers and lasers have a wide III-V mesa (12 μm to 14 μm) for better heat conduction and mechanical strength (Fig. 27a) while a narrow III-V mesa (2 μm to 4 μm) is chosen for detectors and modulators for high-speed operation with a reduced capacitance (Fig. 27b). The optical mode in this hybrid waveguide lies both in the silicon waveguide and the multiple quantum well layers. Once the gain from the III-V active region is equal to the cavity and mirror loss, lasing is achieved. The confinement factor in quantum wells is therefore critical to determine how much gain/absorption is achievable. The silicon confinement factor is an important parameter determining coupling efficiency when the device is integrated
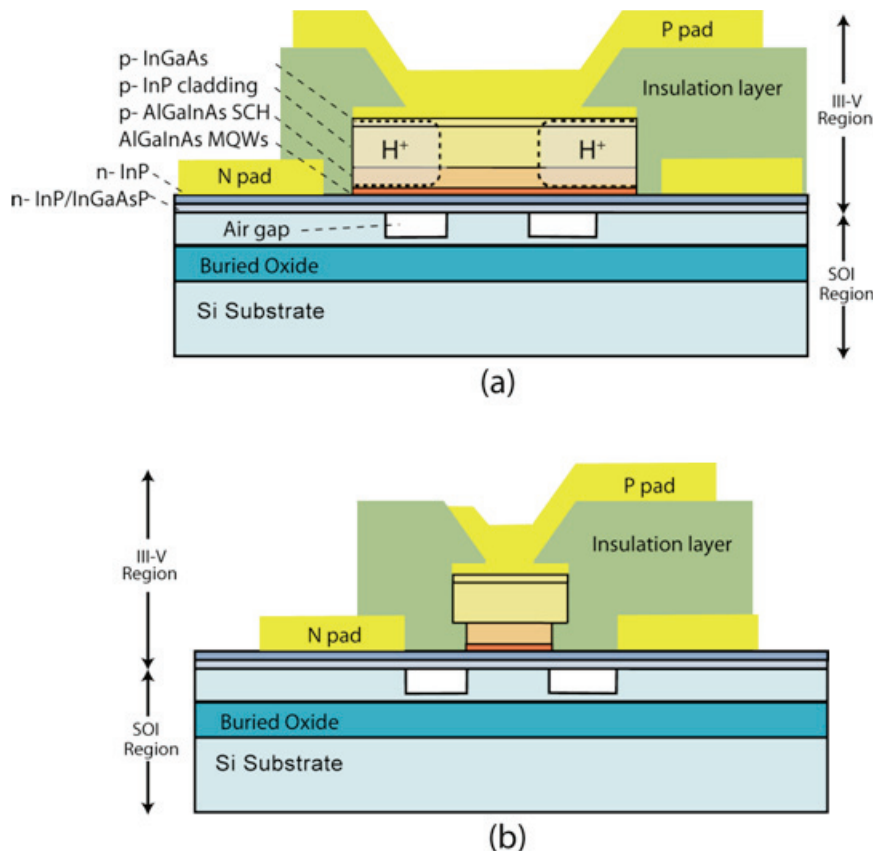

Figure 27 (online color at: www.lpr-journal.org) The hybrid silicon evanescent device cross-sectional structures. (a) A wide III-V mesa for amplifiers and lasers, (b) a narrow III-V mesa for detectors and modulators.
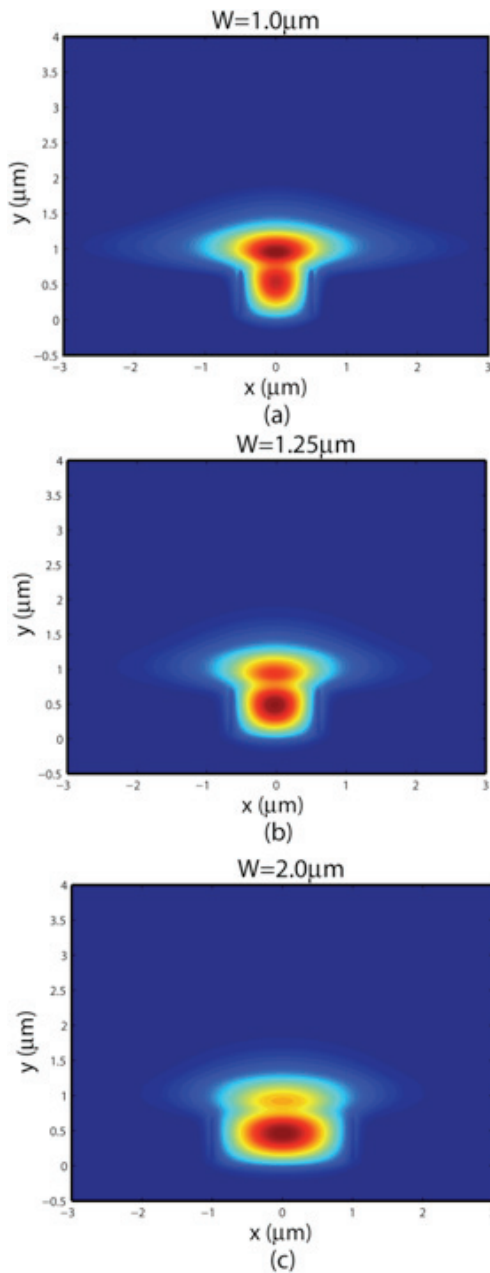
Figure 28 (online color at: www.lpr-journal.org) Mode profiles with different waveguide widths. The height of the silicon waveguide is fixed at 0.7 µm.

with silicon passive devices. The confinement factors in III-V and silicon regions of the hybrid waveguide can however be manipulated by changing the silicon waveguide dimensions. Fig. 28 shows three different mode profiles with three different SOI waveguide widths. In general, the silicon confinement factor increases as the height or width of the silicon waveguide increases, while the quantum well confinement factor decreases. The epitaxial structures and confinement factors for each device set will be specified in the device result section [54].

4.3.2. Single-wavelength laser diodes

While the multi-mode Fabry-Perot laser discussed in the previous section was the first demonstration of a heterogeneously integrated laser diode realized on and coupled to an SOI waveguide circuit, single-wavelength light sources will typically be required in uncooled longer distance communication links. Grating-based lasers are an attractive option for heterogeneous integration as they offer facet-less single-wavelength light sources. There are several geometries to create gratings on the hybrid silicon evanescent platform as Fig. 29 shows. Hybrid active gratings can be formed by patterning a surface corrugation at the bonding interface between the III-V regions and the silicon on either the silicon surface (Fig. 29a) or the III-V surface (Fig. 29b). Passive gratings can be fabricated by etching a surface corrugation on the top surface of the silicon waveguide (Fig. 29c). The grating strength, κ, can be three to four times larger for hybrid gratings with grating dimensions equal to their passive grating counterparts, since the field intensity at this interface is much stronger.

4.3.3. Hybrid silicon DFB lasers

Fig. 30a shows a schematic device layout of a hybrid silicon DFB laser [56] with integrated photodetectors connected to both facets (only one shown). The III-V mesa region above the silicon waveguide consists of a 200-µm-long gain region plus 80-µm-long tapers. The tapers adiabatically transform the optical mode from the hybrid waveguide to the passive silicon waveguide allowing for losses on the order of 1.2 dB per taper and reflections on the order of 6×10^{-4} [57]. The integrated photodetectors are 240-µm long including two 80-µm-long tapers. A ~ 25-nm-deep surface corrugated grating with 238-nm pitch and 71 percent duty cycle is formed on the silicon waveguide by electron-beam lithography and dry etching. The grating stop band is designed around 1600 nm in order to account for the spectral shift seen in previous devices due to device heating [55]. The silicon waveguide has a width, height and rib etch depth of 1.5 µm, 0.7 µm and 0.5 µm, respectively, resulting in a quantum well confinement factor of 5.2 percent and a silicon confinement factor of 59.2 percent. Fig. 30b shows a cross-sectional SEM image of the fabricated device. The effective indices of the unetched region and the etched region are calculated using the film mode matching method to be 3.3688 and 3.3441, respectively. This results in a κ of 309 cm^{-1}. The κ values of these gratings are large when compared to the 91.81 cm^{-1} of surface corrugated gratings on silicon rib waveguides of similar dimensions, since the index perturbation of air is quite large and the grating is located near the center of the mode. The grating is 340-µm long with a quarter-wavelength shift in the center in order to break the modal degeneracy.

The light-current (L-I) characteristics are measured on chip by collecting light out of both sides of the laser with integrated photodetectors. A 100 percent internal quantum
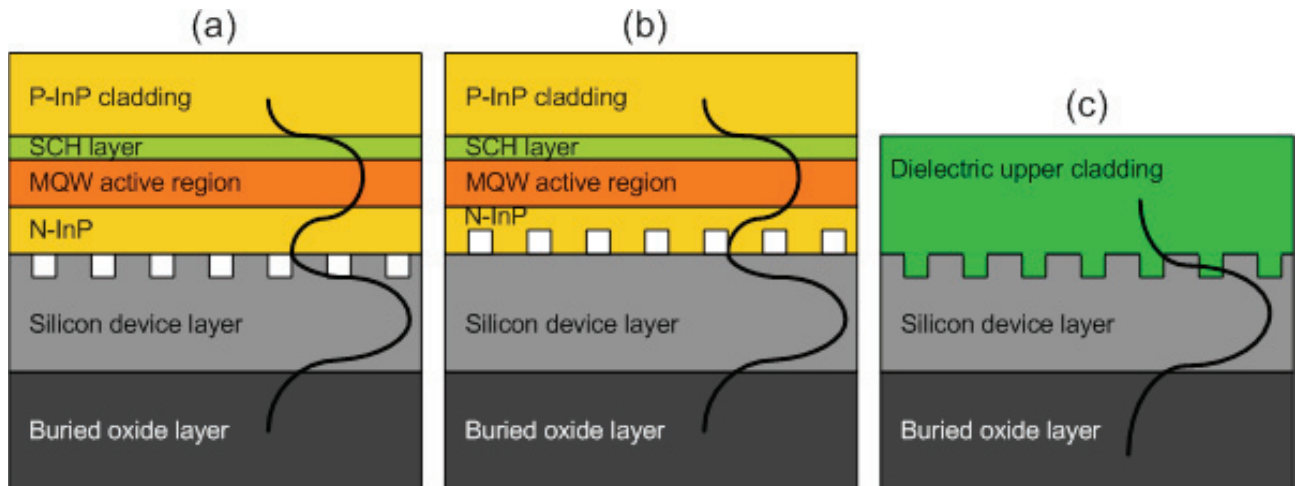
Figure 29 (online color at: www.lpr-journal.org) Longitudinal cross section and mode intensity profile of a silicon hybrid grating (a), a III-V hybrid grating (b) and a passive silicon grating (c).
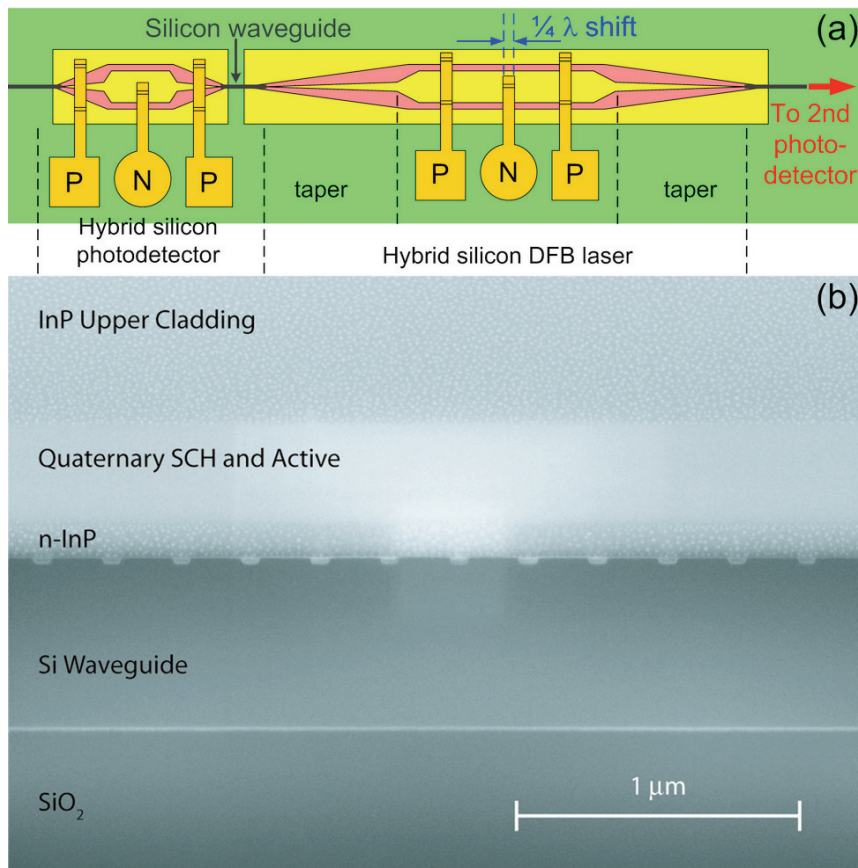

Figure 30 (online color at: www.lpr-journal.org) (a) Schematic layout of hybrid silicon DFB devices. (b) SEM image of longitudinal cross section.

efficiency of the photodetectors is assumed in order to conservatively assess the laser output power. Fig. 31 shows a minimum lasing threshold of 25 mA with a maximum output power of 5.4 mW at 10 °C. The maximum lasing temperature is 50 °C. The lasing spectrum is measured by dicing off the right photodetector and polishing and anti-reflection coating the silicon waveguide output facet. Light is collected with a lensed fiber into an HP spectrum analyzer with a 0.08-nm resolution bandwidth. The spectrum in the inset of Fig. 31 exhibits a lasing peak at 1599.3 nm with 30-mA injection current with a 50-dB side mode suppression ratio. Accurate spectral line width is measured by using the
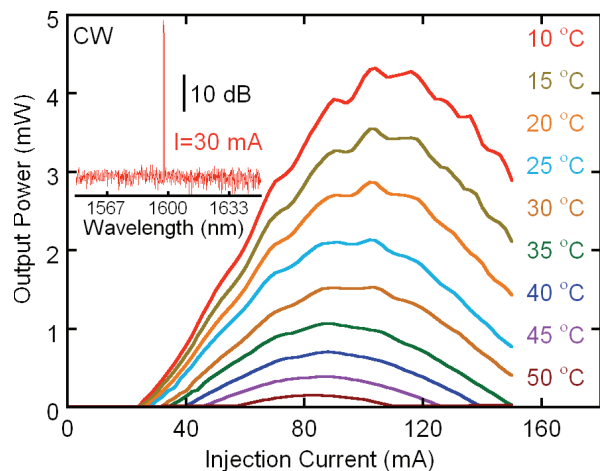
Figure 31 (online color at: www.lpr-journal.org) L-I curve of silicon evanescent DFB lasers at stage temperatures of 10 °C to 50 °C. Inset: the lasing spectrum at 30-mA injection current, showing a single-mode operation span over 100 nm.
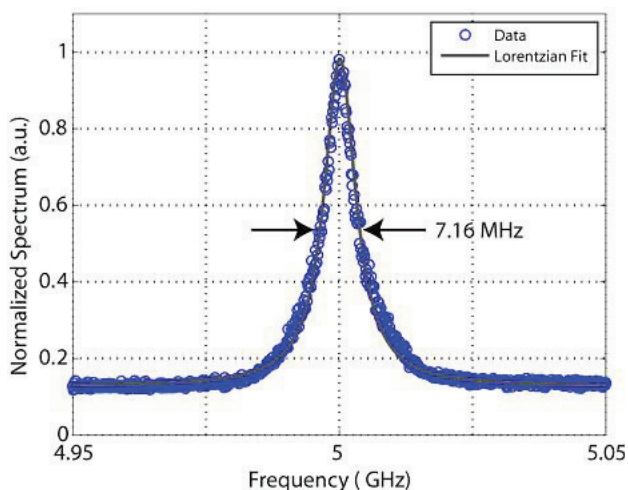

Figure 32 (online color at: www.lpr-journal.org) Delayed self heterodyned line width trace at 1.8-mW silicon evanescent DFB laser output power.

delayed self heterodyne method [59] in Fig. 32. The minimum line width measured at a laser output power of 1.8 mW had a convoluted Lorentzian line width of 7.16 MHz corresponding to 3.6-MHz deconvolved line width, a typical value for commercial DFB lasers.

4.3.4. Hybrid silicon DBR lasers

In contrast to DFB lasers, the longer lasing cavity of DBR lasers reduces their thermal impedance and consequently enhances their output powers [60]. As shown in Fig. 33, the device layout includes two passive Bragg reflector mirrors placed 600-μm apart to form an optical cavity. As for the

DFB lasers, two 80-μm-long tapers sandwich the 440-μm-long silicon evanescent gain region. The back and front mirror lengths are 300-μm and 100-μm long, respectively. The silicon waveguide has a width, height and rib etch depth of 2 μm, 0.7 μm and 0.5 μm, respectively. This results in silicon and quantum well confinement factors of 66 percent and 4.4 percent in the hybrid region. The surface corrugated gratings have an etch depth and duty cycle of 25 nm and 75 percent, respectively, with an upper cladding of SU-8 leading to a grating strength, κ, of 80 cm^{-1}. The power reflectivities of back and front mirrors are calculated to be 97 percent and 44 percent, respectively.

The laser output power is measured with an integrating sphere at the front mirror of the laser. The front mirror L-I characteristic is shown in Fig. 34. The device has a lasing threshold of 65 mA and a maximum front mirror output power of 11 mW, leading to a differential efficiency of 15 percent. Based on our estimations of the material and laser properties, calculations show that the taper loss of 1.2 dB increases the threshold current by a factor of two due to the accumulated loss through four taper transitions in one round trip through the cavity. The laser operates up to a stage temperature of 45 °C. The kinks in the L-I characteristic are because of a longitudinal mode hop caused by the laser wavelength red shifting due to self heating. The lasing spectrum is shown in the inset of Fig. 34 with a lasing peak at 1597.5 nm and 50-dB SMSR when driven at 200 mA.

Fig. 35 shows the lasing spectrum as a function of drive current along with the corresponding L-I curve. Note that the output power in this case is fiber coupled, which is ~5 dB lower than the total output power measured earlier in Fig. 34. It can be seen that as the device heats with larger current injection, the lasing mode moves to longer wavelengths due to the thermo-optic effect in the cavity. When the mode moves far enough from the reflection peak, a longitudinal mode hop to another mode occurs. The mode hopping appears to be chaotic between stable mode positions and the reason for the exact hopping pattern we observed is unknown at this time.

Direct modulation characteristics of the device are studied by using a bias-T to drive the laser simultaneously with a direct bias current and a radio-frequency (RF) signal while measuring the electro-optic (EO) response on a photodetector. Fig. 36 shows the photodetected EO response of the laser under small-signal modulation of −10 dBm. S_{11} measurements indicate that the electrical contact geometry is not limiting the performance of the device, so reflected power has not been factored out of these curves. A 2-pF device capacitance was extracted from the S_{11} measurement, resulting in an RC limited bandwidth of 7 GHz. The inset of Fig. 36 shows the resonance frequency versus the square root of the direct drive current above threshold, which has a roughly linear dependence, as expected. Under higher modulation powers the resonance peak becomes significantly damped. The 3-dB electrical bandwidth at 105 mA is ~2.5 GHz.

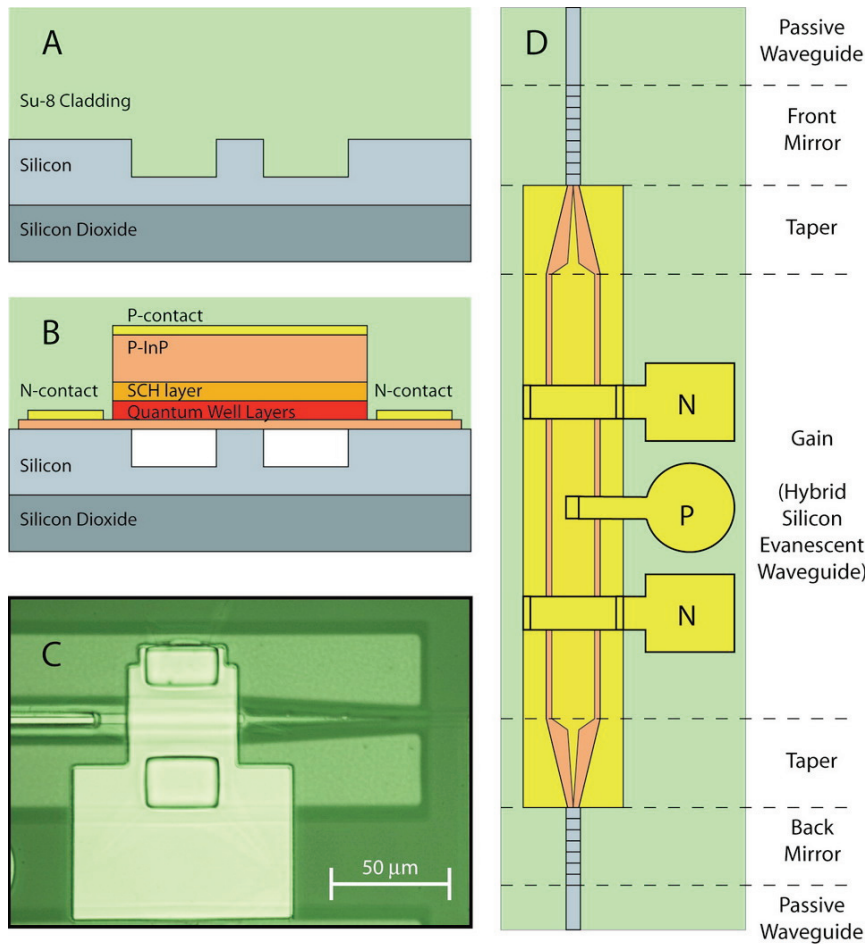The eye diagram in Fig. 37a represents the modulation signal of the device biased at 105-mA direct current with a

Figure 33 (online color at: www.lpr-journal.org) (a) Passive silicon rib, (b) hybrid silicon evanescent waveguide cross section, (c) microscope image of a hybrid to passive taper, (d) DBR-SEL top-view topographical structure.
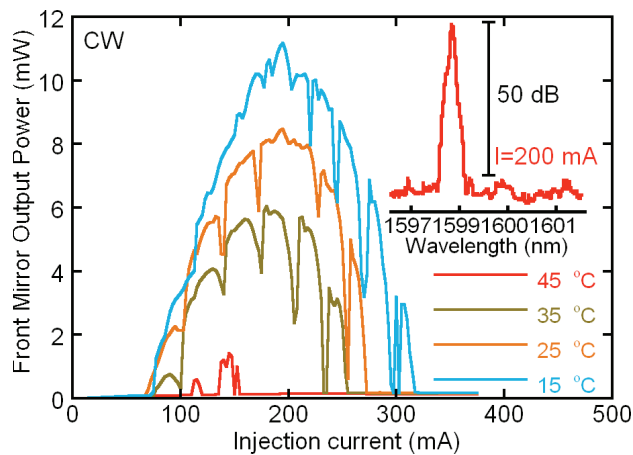

Figure 34 (online color at: www.lpr-journal.org) DBR laser L-I curve for various temperatures measured out of the front mirror. Inset: the lasing spectrum at 200-mA injection current, showing a single-mode operation with 50-dB SMSR.

Figure 35 (online color at: www.lpr-journal.org) Fiber-coupled DBR L-I curve and spectrum versus current at a stage temperature of 18 °C.

2.5-Gb/s, $2^{31} - 1$ PRBS electrical signal with 20 mW of RF power. The extinction ratio is 8.7 dB and the fiber coupled output power is ~ 0.7 mW when cooled to 18 °C. Although 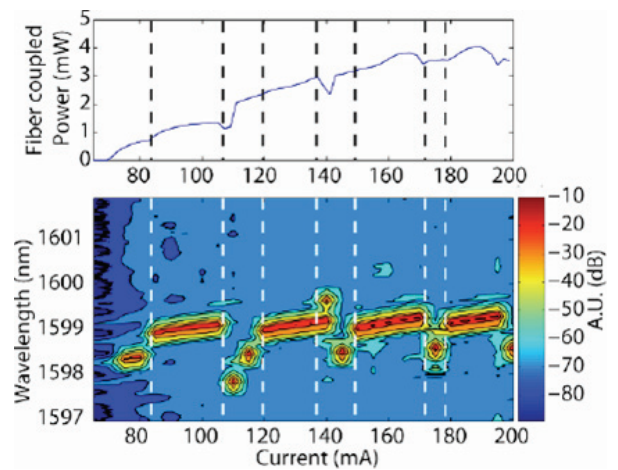the output power and modulation bandwidth increase at higher direct currents, the extinction ratio decreases unless larger corresponding RF modulation powers are used. For example, Fig. 37b shows an eye diagram at 4 Gb/s that can be obtained with a DC bias of 135 mA and an RF power of
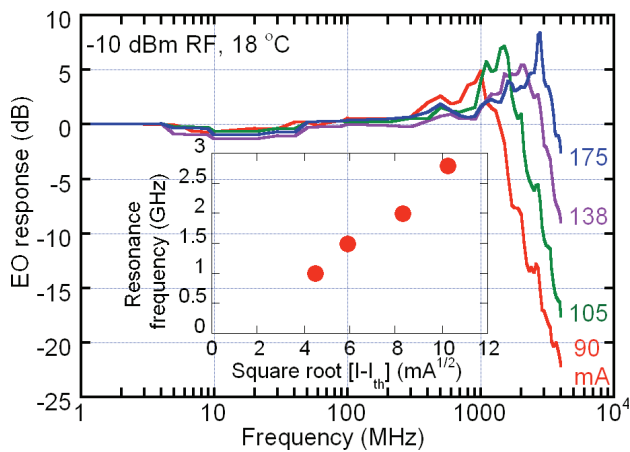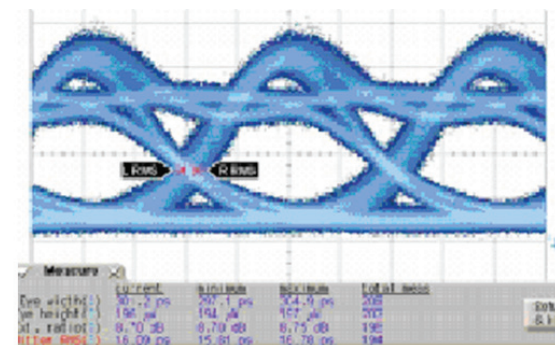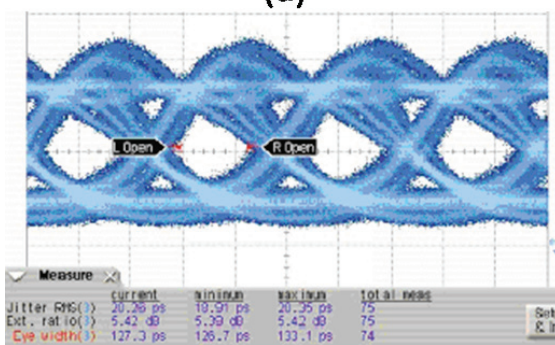
Figure 36 (online color at: www.lpr-journal.org) Photodetected frequency response of the DFB-SEL for three different bias currents with a stage temperature of 18 °C and (inset) plot of resonance frequency versus the square root of current above threshold.

(a)

(b)

Figure 37 (online color at: www.lpr-journal.org) Eye diagrams of a directly modulated DBR-SEL at (a) 2.5 Gb/s and (b) 4 Gb/s.

39 mW. However, in this case the extinction ratio (ER) is close to 5.5 dB. Improving the laser design to decrease the threshold current and increase the differential gain is expected to significantly improve the modulation bandwidth in future devices.

4.4. Direct-bonded multi-wavelength mode-locked laser source

4.4.1. Introduction

Another approach to achieving a WDM source is to use a single laser with multiple longitudinal modes. For a regular multi-mode laser, e.g. a Fabry-Perot laser, instability in the powers, phases and wavelengths of the individual modes makes this approach unfeasible. However, these instabilities can be reduced significantly in a mode-locked laser (MLL), which emits an array of continuous-wave (CW) wavelengths that are phase locked to each other. Stability is especially improved if optical injection locking is implemented [61–63].

Semiconductor MLLs can be made by introducing a small absorbing section into a standard laser cavity. Fabrication of these lasers requires only one additional process step to isolate a section of the active material from the rest. This isolated section can then be reverse biased to act as a saturable absorber, while the rest of the active material is forward biased as a gain section to generate light as shown in Fig. 38. With the proper choices of length for the two regions and the proper bias conditions, it becomes favorable for all laser modes to interfere constructively when passing through the absorber section. This means that all laser modes are in phase with each other and as a result pulses are generated in the cavity. The mode spacing and pulse-repetition rate are determined by the cavity length of the MLL. The wavelength positions of the laser modes are locked to each other but it is possible for the wavelengths of these modes to shift together in time due to changes in temperature or other instabilities. Fine temperature control
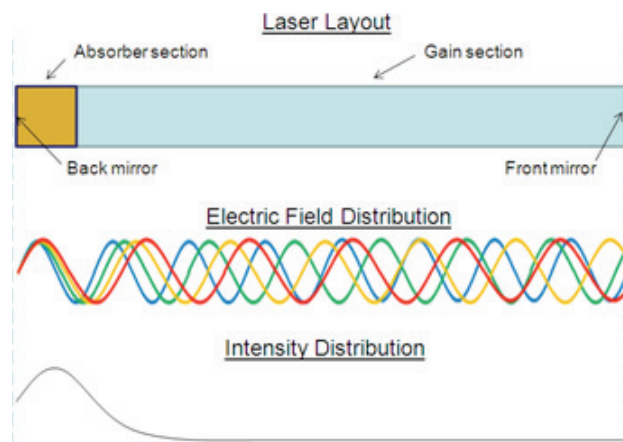

Figure 38 (online color at: www.lpr-journal.org) A mode locked laser (MLL) layout consisting of a long gain section that is forward biased and a relatively short absorber section that is reverse biased. The multiple longitudinal modes of the laser combine constructively in the absorber section, which causes the modes to lock in phase with each other and also results in intensity pulses.
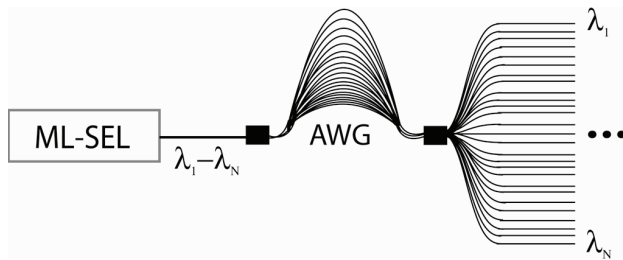
Figure 39 Envisioned implementation of a mode-locked silicon evanescent laser as a WDM source.

can stabilize the modes, but the problem can be better overcome by injecting a stable external laser signal into the MLL cavity. One of the MLL modes can become locked to this external laser signal. Since the MLL modes are locked to each other, all of the MLL modes become locked in position and their positions can be moved by tuning the input laser wavelength.

Previous studies of integrated semiconductor MLLs designed for multiple-wavelength generation in WDM systems have shown successful results in terms of the number of modes that can be generated and mode quality of the individual modes. Teshima et al. demonstrated a 25-GHz MLL with over 70 modes within 3 dB of the peak power [62]. Using optical injection locking, the line widths of these modes were reduced to less than 100 kHz. Mori and Sato used supercontinuum generation in conjunction with an MLL to generate 25-GHz spaced modes covering the wavelength range from 1460 to 1625 nm [61]. Although system-level demonstrations have not been done using MLLs as a WDM source, similar experiments have proven that effects such as four-wave mixing and crosstalk between the channels can be overcome even in long-haul transmission. Ohara et al. used phase modulation of a single-wavelength source in combination with supercontinuum generation to generate

1046 modes [64]. This technique is similar to the MLL technique except that the multiple modes are generated outside of the laser cavity by an RF phase modulator. They demonstrated transmission of 1046 channels at 2.46 Gb/s with 6.25-GHz spacing over 126 km in a field-installed standard single-mode fiber. Although such a demonstration has not been done with an MLL yet, it is at least feasible based on the MLL mode qualities demonstrated in other works.

Depending on the output power per mode and the stability of each mode, a MLL could be used as part of an intra-chip or inter-chip transmitter [61]. This section discusses test results and analysis of the output characteristics for modes of a 10-GHz mode-locked silicon evanescent laser (ML-SEL) [65]. Fig. 39 shows a potential implementation of an ML-SEL-based WDM source. To transmit data a modulator needs to be added to each channel, either immediately at the output of the arrayed waveguide grating or elsewhere on the chip after the channels have been spatially separated and routed to different locations.

The hybrid III-V/SOI ML-SEL discussed here is schematically depicted in Fig. 40. It has a ∼ 4-mm-long cavity composed of an 80-μm-long saturable absorber (SA) section placed next to the back mirror and a large gain section that extends along the rest of the cavity. This laser's mirrors are formed by the end facets, which provide approximately 33 percent power reflectivity each. The SA section is made up of the same active material as the gain section but it is electrically isolated from the gain section via a proton implantation between the sections. Future designs could clearly benefit from a higher-reflectivity back mirror and the inclusion of a passive section in the cavity. These changes are now readily achievable on this platform through the use of ring cavities [66], DBR mirrors [67] and active-passive tapers [67], which together also allow for the integration of this laser with other components on a single silicon chip.
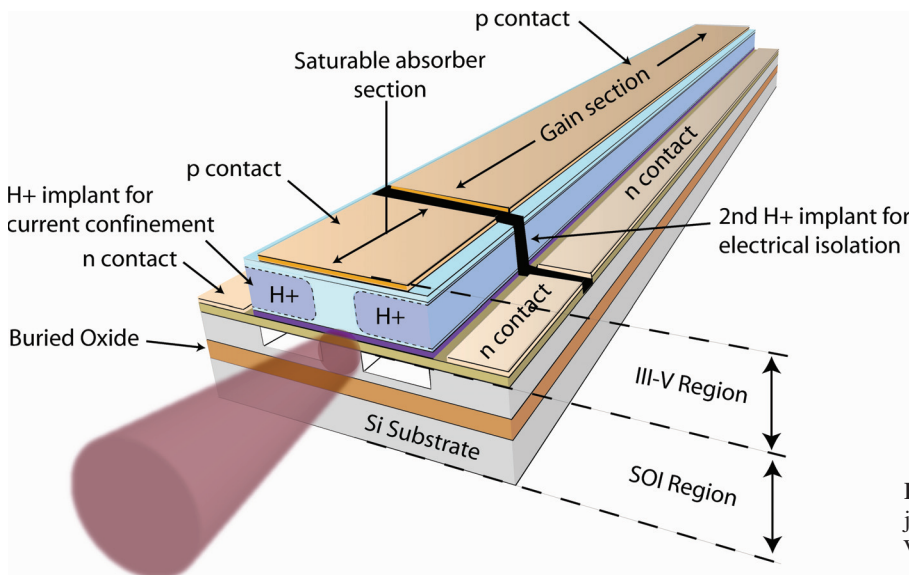

Figure 40 (online color at: www.lpr-journal.org) Schematic of the studied III-V/SOI hybrid mode locked laser [68].
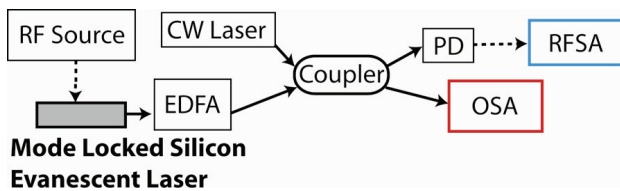
Figure 41 (online color at: www.lpr-journal.org) Experimental setup used to drive and characterize the mode-locked laser diode.

4.4.2. Experiments and results

The gain section was biased at 1.03 A and the SA section was reverse biased at -2.5 V in order to induce passive mode locking. For these experiments the laser's output was stabilized by also applying a 15-dBm RF signal at 10.26 GHz to the SA section through a bias-T. The experimental setup is shown in Fig. 41. The output of the ML-SEL is sent into an EDFA and to a coupler. At the coupler the signal is combined with a stable (< 0.1-pm resolution), narrow line width (< 100 kHz) CW probe signal used to measure the individual modes of the ML-SEL as described below. The output of the coupler is sent to an optical spectrum analyzer (OSA) and a photodetector (PD) connected to an RF spectrum analyzer (RFSA).

The optical spectrum is shown in Fig. 42. The 10-dB spectral width is 9 nm, with over 100 modes spaced by
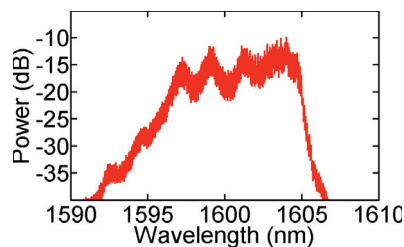

Figure 42 (online color at: www.lpr-journal.org) Optical spectrum of the 10-GHz ML-SEL with 0.06-nm resolution, which cannot resolve the individual modes well.
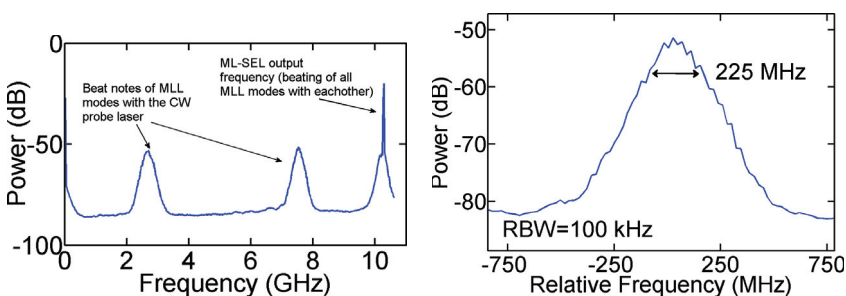
0.089 nm. The average output power was -2.8 dBm in the fiber after 6-dB coupling loss. When the probe laser is combined with the ML-SEL output, beat notes are created between the probe wavelength and the individual longitudinal modes of the ML-SEL. By looking at the RF spectrum of these combined signals as shown in Fig. 43, we can determine the line width [61, 62] and OSNR [63] of the ML-SEL modes from the beat notes. Fig. 44 shows a zoom of one of the beat notes. The resolution of the line-width measurement is determined by the line width of the probe laser, which is less than 100 kHz. We define the OSNR as one half of the ratio of the peak level to the bottom level of the comb as measured on the RFSA. This measurement provides a lower limit of the OSNR because the RF spectrum between the modes also contains noise from beating between other harmonics of the CW probe laser with other ML-SEL modes. Fig. 45 shows line-width and OSNR measurements for several modes across the ML-SEL 10-dB spectral width. The performance is not adequate for long haul communication links but is likely to be useable for intra- and inter-chip communications. There will be more discussion on applications later in this section.

To test the performance under optical injection locking, a stable -6 dBm (after fiber coupling) CW seed signal was injected into the back of the ML-SEL. This reduced the 10-dB spectral width to about 2.5 nm (30 modes) but improved all of the other characteristics. The optical spectrum of the ML-SEL for three different injected wavelengths is shown in Fig. 46. For injected laser wavelengths in the approximate range of 1599 to 1610 nm the line width was reduced to that of the CW input signal (100 kHz) across 30 modes. An example mode is shown in Fig. 47. Fig. 48 shows that the OSNR was improved by approximately 10 dB due to the injection locking. Again, this number is likely limited by the measurement capabilities.

4.4.3. Discussion

Table 3 compares the output characteristics for no injection locking and with injection locking. Even without injection

Figure 43 (online color at: www.lpr-journal.org) RF spectrum of the ML-SEL output combined with the CW probe laser.

Figure 44 (online color at: www.lpr-journal.org) Zoom of the RF spectrum of the CW signal beat together with the ML-SEL output with 100-kHz resolution.
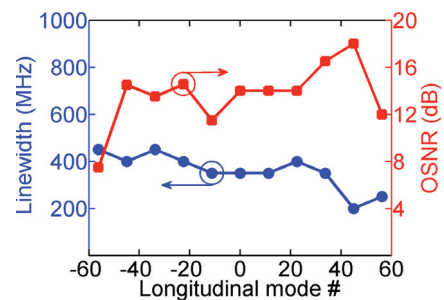

Figure 45 (online color at: www.lpr-journal.org) OSNR and 3-dB line width versus ML-SEL mode number. Mode 0 corresponds to 1600 nm.
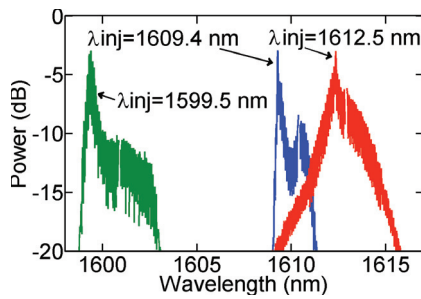
Figure 46 (online color at: www.lpr-journal.org) Optical spectrum of the ML-SEL output under optical injection locking to an external CW laser, for three different wavelengths of the injected laser.
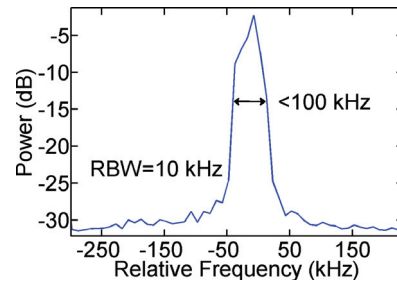
Figure 47 (online color at: www.lpr-journal.org) Zoom of the RF spectrum showing the line width under CW injection to the ML-SEL at 1609.4 nm, with 100-kHz resolution.
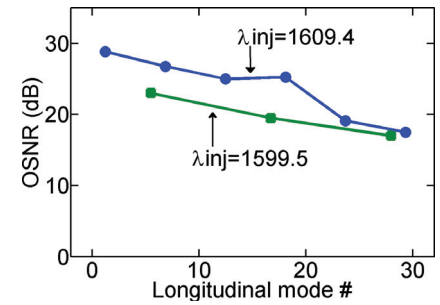
Figure 48 (online color at: www.lpr-journal.org) OSNR versus mode number for two different injected wavelengths. Mode 0 corresponds to the injected CW wavelength.

Table 3 Comparison of ML-SEL performance with no optical injection and with injection.

Method	No injection	Injection
Number of modes within 10 dB	100	30
Average power per mode (dBm)	-17	-12
Line width (MHz)	200–500	0.1
OSNR (dB)	> 12–18	> 17–29
Wavelength stabilized	No	Yes

locking, the OSNRs are sufficient to provide error-free operation assuming that significant signal degradation is not accumulated during transmission (the BER can be lower than 10^{-12} for these OSNRs, assuming that OSNR limits performance). The average power of each mode is -17 dBm providing a loss budget of ~ 6 dB above a typical p-i-n PD sensitivity at 2.5 Gb/s (~ 17 dB above a typical APD sensitivity). With detector sensitivities ~ 3–6 dB lower at 10 Gb/s, an APD would almost certainly be required at this data rate unless the power of each mode were increased. We must keep in mind that if 10-GHz spaced channels are modulated at 10 Gb/s, they cannot be multiplexed together because the modulated spectra will overlap. However, it is possible to multiplex the signals to two fibers/waveguides each with every other wavelength channel on it. Otherwise a higher repetition rate mode locked laser with wider channel spacing is required. Of course, if the channels are never multiplexed and parallel waveguides or fibers are used, the modulation can be at any data rate regardless of the channel spacing.

The RIN of each mode is another important characteristic that we unfortunately could not measure due to the narrow channel spacing. It would be critical to measure this before stating with certainty that these modes could be used. However, the data collected so far suggests that it is likely that this laser could be utilized as an on-chip or chip-chip WDM transmitter. The main practical issue appears to be that although each mode is locked to the others, the absolute wavelength position of the wavelength array can fluctuate in time as the temperature and index of refraction in the cavity change. In the integrated chip shown in Fig. 39, this will result in misalignment of the ML-SEL output modes and the AWG pass bands. Here injection locking could be used unless very strict control of the temperature were possible, as, although it requires an additional laser, it dramatically improves the output characteristics. Furthermore, the ability to tune the output wavelengths by controlling the input wavelength provides the capability to match the mode positions to the AWG pass bands, which may be difficult in grating-based single-wavelength lasers unless they are all tunable. Also, it should be noted that although optical injection reduced the number of lasing modes for this laser, this is not an inherent result, and optical injection locking has even been shown to increase the spectral width of a mode-locked laser in some cases [66]. A better understanding of mode locking and injection locking dynamics in this device platform should allow for optimization of the performance in all aspects. Interestingly, the devices needed to create integrated sources employing this technique on this platform already exist. For example, a DBR [67] or DFB injection laser could be integrated with a racetrack ML-SEL [66] or a ML-SEL having broadband etched mirrors.

5. Conclusions

In this paper the concept of using heterogeneous integration as a means to realize light emission on a silicon photonic platform was presented. Two bonding techniques were discussed, one based on the realization of interfacial bonds (direct bonding) and one based on using the polymer DVS-BCB as a bonding agent. Both techniques are believed to be viable from an industrial perspective. They each have their own advantages and disadvantages, depending on the particular application. Therefore, it is impossible to select one particular technology. Moreover, in the design of the envisioned devices, one can counter some of the drawbacks of a particular technology. In order to stress the fact that both technologies are equally attractive, in Sect. 3.2 we reported on the realization of both direct bonded and adhesively bonded micro-disk lasers with comparable performance. In

terms of reliability, it is unclear at this point which technology is preferable, but research on this topic is under way both at IMEC and INTEL.

A whole set of light-emitting devices were presented in this paper, which can be used in intra-chip and chip-to-chip optical interconnect applications. On the intra-chip interconnect side, small-footprint devices such as micro-disk lasers (and arrays of micro-disk lasers for wavelength-division multiplexing) have been presented. These devices have a footprint of approximately $100\,\mu m^2$ and provide optical output powers in the range of tens of micro-watts. For chip-to-chip optical interconnect applications higher output powers are required however and therefore longer-cavity laser structures such as adhesively bonded Fabry-Perot lasers and direct-bonded DFB, DBR and mode-locked lasers were presented, where the output power exceeds the 1-mW level. Although these demonstrations show the potential of bonding unprocessed III-V dies or wafers onto silicon photonic integrated circuits, several issues still have to be overcome in order to make this a platform technology for commercial products. From a performance point of view, there is a clear need to reduce the thermal resistance of the bonded devices. While a first demonstration of integrating a heat-sink structure on bonded III-V/SOI lasers is reported in this paper, further development is needed to achieve sufficiently low thermal resistance. From a fabrication point of view, yield of the bonding and III-V processing needs to be improved. This is not an intrinsic problem but requires more development to bring this technology to an industrial level. In the not so near future one could even foresee the processing of the III-V layers to happen in the CMOS fabrication line, given the fact that more and more materials are starting to be accepted in the CMOS fabrication flow. If these issues can be tackled in the coming years, this technology has a wide range of applications from the short-reach computer interconnects discussed here to communications to biological and environmental sensors.

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