

Efficient evanescent coupling between SOI waveguides and heterogeneously-integrated III-V pin photodetectors

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Integrating III-V materials on Si is a promising candidate to realize both passive and active optical functions on a single silicon chip. We have developed this heterogeneous integration technology by means of a low-temperature die-to-wafer bonding process with divinylsiloxane benzocyclobutene (DVS-BCB) as the bonding layer [1]. By using this technology, we have reported III-V pin photodetectors integrated on Si with the help of a grating coupler to diffract the light from SOI waveguides vertically to photodetectors [2]. However, like ordinary surface-illuminated detectors, there is a trade-off between the responsivity and the transition-time-limited bandwidth when choosing the thickness of the intrinsic InGaAs (i-InGaAs) absorption layer.

Here we investigate the evanescent coupling between SOI waveguides and heterogeneously-integrated III-V pin photodetectors. A typical cross section of an evanescently-coupled pin photodetector on an SOI waveguide is shown in Fig. 1. The n-type metal (not shown in the figure for clarity) is placed far away from the SOI waveguide on a thin n-InP lateral contact layer, and, therefore, has no influence on the optical coupling. In this configuration, however, p-type contact layers, i.e., the p-InGaAs and the metal contact are in direct touch with the optical field in the III-V layer. Therefore, a considerable part of the optical power is lost due to the absorption by these layers. In order to estimate this loss, we calculated the absorbed power as a function of detector length for both the real structure and a virtual structure where we only take into account the unwanted absorption of the p-InGaAs and the metal contact layers (assuming no absorption in i-InGaAs). The results are shown in Fig. 2, where it indicates that the absorption by the p-InGaAs and the metal contact layers is quite serious and it is necessary to reduce this loss for an efficient photodetector.

This problem can be effectively solved by introducing a central opening on the p-contact layers as shown in Fig. 3. Due to the large imaginary parts of the metal contacts on both sides of the detector mesa, the optical mode is confined in the central part of the mesa, and the overlap of the optical field with the p-type contact layers is reduced significantly. Again, we calculated the absorbed power for both the real structure and a virtual structure with no i-InGaAs absorption. The results are shown in Fig. 4. One sees that the absorption by the p-type contact layers is now less than 5% of input power.

References:

1. G. Roelkens, et al, J. Electrochem. Soc., vol. 153, pp. G1015-G1019, 2006.
2. G. Roelkens, et al, Opt. Express., vol. 13, pp. 10102-10108, 2005.

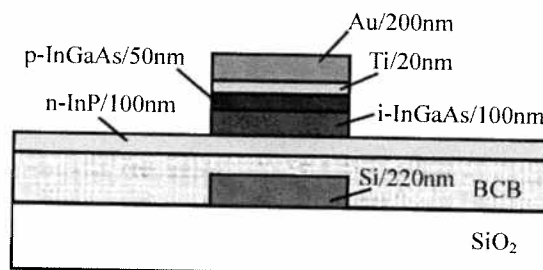


Fig. 1 The cross section of a pin photodetector evanescently coupled with an SOI waveguide. The thickness of each layer is also shown.

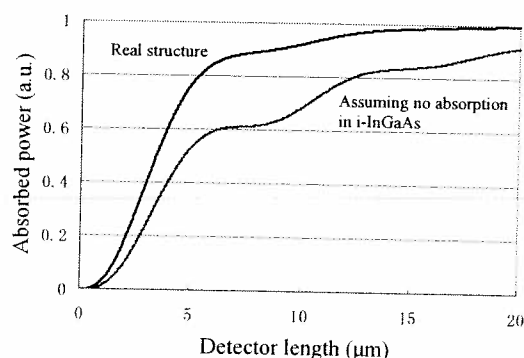


Fig. 2 The absorbed power for both the real structure and a virtual structure with no i-InGaAs absorption. The structure used is shown in Fig. 1.

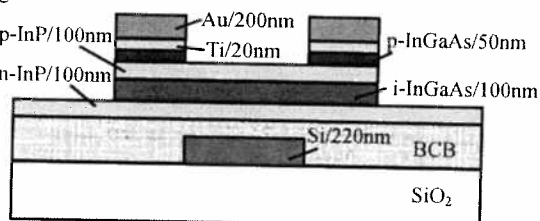


Fig. 3 The cross section of a novel configuration of a pin photodetector evanescently coupled with an SOI waveguide, where a central opening is introduced on the p-contact layers.

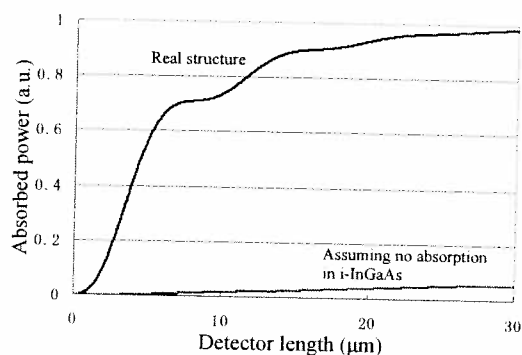
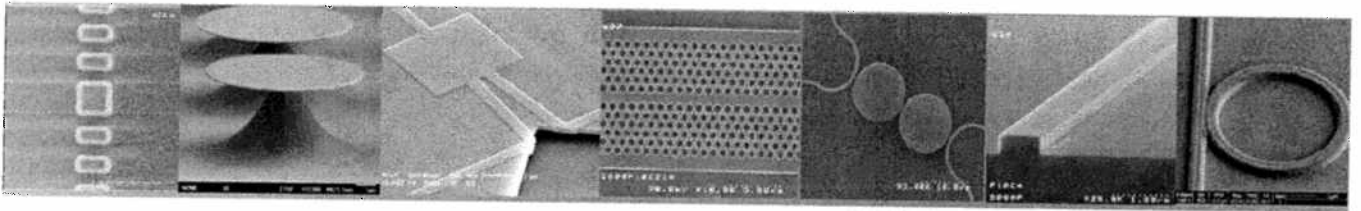


Fig. 4. The absorbed power for both the real structure and a virtual structure with no i-InGaAs absorption. The structure used is shown in Fig. 3.



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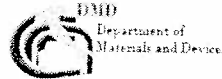
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Introduction

In its everlasting quest to deliver more data using smaller and lower cost components, the silicon industry is moving full steam ahead towards its final frontiers of size, device integration and complexity. For several years, **silicon-based photonic devices** have been widely considered to develop integrated circuits to overcome the microelectronic bottlenecks by combining existing silicon infrastructure with optical communications technology, and a merger of electronics and photonics into one integrated dual-functional device.

The challenge for **silicon photonics** is to manufacture low-cost information processing components by using standard and mature **CMOS technology**. Numerous photonic devices have already been developed in the last years to emit, propagate and distribute, modulate and detect light on silicon substrates. However, several obstacles should be overcome to foresee silicon photonics for the next generation high-speed systems.

The *5th Optoelectronic and Photonic Winter School* is dedicated to introduce, examine and review the recent achievements in the field covering fundamentals and devices, materials and technologies.

The School goals are:

1. to put the emphasis on the main building blocks towards a silicon photonics: from the light generation to the CMOS integration
2. to introduce PhD students and young researchers to this field and to determine the state of the art of silicon photonics, from the theory to the characterization with a point on the technology
3. to be a forum to exchange experiences about new advances and developments in the field thus promoting the scientific exchange between participants and contributors.

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