Heterogeneous integration of III-V optoelectronic devices on silicon

Dries Van Thourhout, Günther Roelkens, Joost Brouckaert, Katarzyna Komorowska, Liu Liu, Roel Baets
Department of Information Technology
Ghent University – IMEC
Ghent, Belgium

Richard Nötzel
Photonics and Semiconductor nanophysics
Eindhoven University of Technology
Eindhoven, The Netherlands

Abstract—**Silicon has been proven to be an excellent platform for photonics. However, active functionality and in particular light generation directly from silicon remains difficult. Therefore we developed a die-to-wafer bonding based approach for integrating III-V materials directly on silicon in a cost-effective way, which does not compromise the quality of the materials. In this paper we will illustrate the integration technology developed and several devices fabricated.**

Silicon nanophotonics, heterogeneous integration, lasers, detectors

I. INTRODUCTION

Silicon is an excellent material for realizing compact and cost-effective photonic integrated circuits. The high refractive index contrast with air and SiO_2 allows for fabricating very compact optical filter structures such as ring resonators and photonic crystal structures. Moreover, the structures can be fabricated using the same equipment used for realizing the most advanced electronic circuits, resulting in cost-efficient and high-yield fabrication processes [1-3].

Also several types of active devices such as modulators and detectors monolithically integrated on or with silicon passive waveguides have been shown in recent years. An efficient laser monolithically integrated with such waveguides and operating in the telecom wavelength band has not yet been demonstrated however.

Although different alternatives are being investigated, III-V based materials still are the most attractive for light emission and amplification. Different methods exist for integrating III-V based optoelectronic devices with silicon waveguides. Methods based on flip-chip or thin film devices start from prefabricated and pretested optoelectronic devices, which are subsequently bonded on the substrate. This requires accurate and time-consuming alignment of the devices with the underlying substrate and is not compatible with waferscale fabrication methods. Direct growth of III-V materials on silicon is also investigated intensively and is fully compatible with waferscale fabrication methods. However, the large difference in crystal structure poses significant challenges.

Therefore, we developed an alternative approach based on wafer-bonding technologies [4, 5]. Figure 1 illustrates the technology that was developed. In a first step the passive silicon waveguide structures are defined in an SOI wafer using DUV lithography and ICP-etching. The waveguide structures are typically around 220nm high. Subsequently, the waveguides are planarized using BenzoCycloButene (BCB) (Figure 1b), which is diluted to obtain the required layer thickness (from 50nm to 3µm). BCB has excellent planarizing properties and even for 100nm spin-on-layers, we obtain a flatness of better than 10%. Next, InP-dies with suitable epitaxial layers are bonded on the silicon waveguide substrates. The size of the InP-dies is typically from $2x2mm^2$ to $1x1cm^2$. Since the dies are unpatterned, only a very rough alignment is required (+/-50µm) and this process can be very fast.

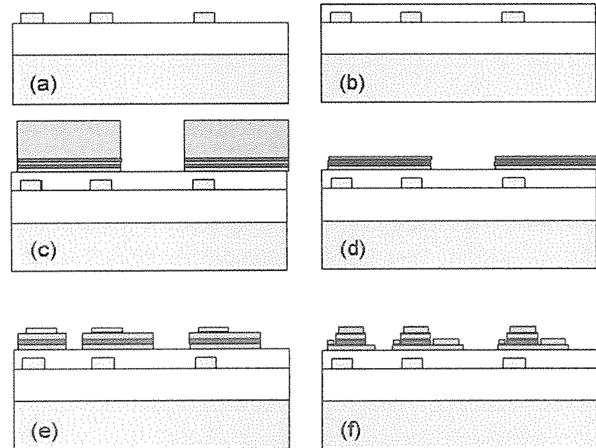


Figure 1 Heterogeneous integration process

Following bonding of the die, the InP-substrate is removed using mechanical grinding and chemical etching down to an InGaAs etch stop layer (which is then also removed) (Figure 1d). In this way only a thin epitaxial layer remains on the silicon waveguides, which then can be further processed using standard waferscale processes such as hard mask definition (Figure 1e), mesa etching and metallization (Figure 1f). Alignment between the optoelectronic devices and the underlying waveguides is assured through the lithographic process. Note that multiple devices can be processed from a single bonded die. Lately, research has focused on obtaining ultra-thin bonding layers. This is important for better optical coupling and improved heat removal. Figure 2 shows an example where a 80nm III-V film is bonded using a 65nm BCB layer.

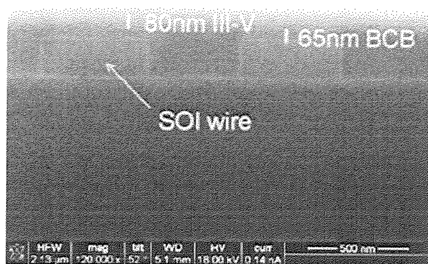


Figure 2 III-V film bonded on SOI-wire waveguides with 65nm bonding layer

II. Fabricated Devices

Figures 3-6 show some devices fabricated using the approach described above. Figure 3 (left) shows the cross-section of a micro-disk laser integrated on silicon waveguides. Micro-disk lasers are attractive because the whispering gallery mode allows can be separated from the top contact used for injecting the current [6].

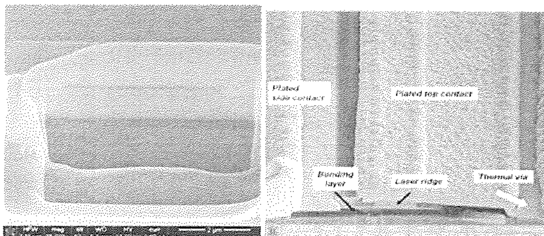


Figure 3 Microdisk laser: cross-section (left) and FP-laser with thermal via (right).

BCB is a very bad heat conductor. Figure 3 (right) shows how this problem can be overcome using a thermal via to the substrate [7].

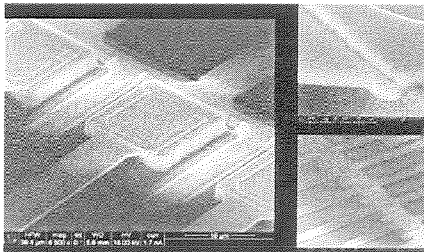


Figure 4 Array of PIN-detectors on silicon

Figure 4 and Figure 5 show respectively III-V PIN-detectors and MSM detectors on silicon. The PIN-detectors are intended for vertical injection, e.g. through a grating coupler, which allows for a thick bonding layer (>2μm). For the MSM-detectors, light is coupled through evanescent field coupling, which requires a bonding layer below 300nm [4].

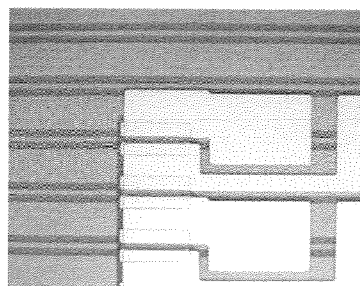


Figure 5 Array of MSM-detectors on silicon waveguides

III. Conclustion

We developed a new approach for integration of III-V optoelectronic devices on silicon waveguides. Several devices fabricated using this technology were demonstrated.

IV. Acknowledgements

We acknowledge support of the IWT through the SBO epSOC project and the ICT-PICMOS project.

References

[1] W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, and D. Van Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," *Journal of Lightwave Technology*, vol. 23, pp. 401-412, Jan 2005.

[2] Y. A. Vlasov and S. J. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," *Optics Express*, vol. 12, pp. 1622-1631, Apr 2004.

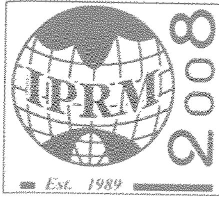
[3] T. Tsuchizawa, K. Yamada, H. Fukuda, T. Watanabe, T. Jun-ichi, M. Takahashi, T. Shoji, E. Tamechika, S. Itabashi, and H. Morita, "Microphotonics devices based on silicon microfabrication technology," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 11, pp. 232-240, 2005.

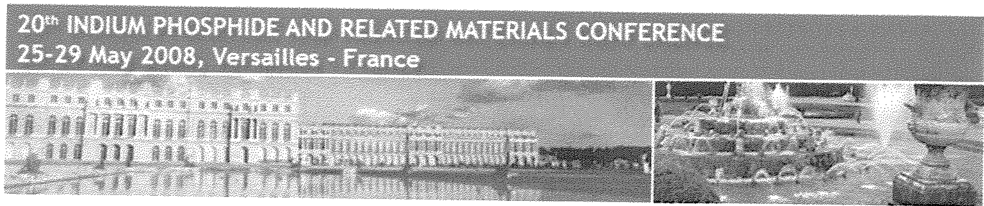
[4] J. Brouckaert, G. Roelkens, D. Van Thourhout, and R. Baets, "Compact InAlAs-InGaAs Metal-SemiconductorMetal photodetectors integrated on silicon-on-insulator waveguides," *Ieee Photonics Technology Letters*, vol. 19, pp. 1484-1486, Sep-Oct 2007.

[5] G. Roelkens, J. Van Campenhout, J. Brouckaert, D. Van Thourhout, R. Baets, P. R. Romeo, P. Regreny, A. Kazmierczak, C. Seassal, X. Letartre, G. Hollinger, J. M. Fedeli, L. Di Cioccio, and C. Lagahe-Blanchard, "III-V/Si photonics by die to wafer bonding," *Materials Today*, vol. 10, pp. 36-43, Jul-Aug 2007.

[6] J. Van Campenhout, P. Rojo-Romeo, P. Regreny, C. Seassal, D. Van Thourhout, S. Verstuyft, L. Di Cioccio, J. M. Fedeli, C. Lagahe, and R. Baets, "Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit," *Optics Express*, vol. 15, pp. 6744-6749, May 2007.

[7] G. Roelkens, D. Van Thourhout, and R. Baets, "Continuous wave lasing from DVS-BCB heterogeneously integrated laser diodes," in *IPNRA '07*, Salt Lake City, USA, 2007, p. iTuG4.





SEARCH
HOME
ABOUT IPRM 2008
COMMITTEES
CONFERENCE PROGRAMME
SHORTCOURSES
PLENARY SESSION
AUTHORS INDEX
PARTNERS AND SPONSORS
CONTACT US

ABOUT IPRM 2008

IPRM 2008 is the major conference worldwide on Indium Phosphide and Related Materials, from physics to applications. It aims at highlighting major developments in the field of InP and related materials, devices and processing at the heart of key technologies in optical telecommunications, ultrafast microelectronics, sensors.

The IPRM technical conference and exhibit is held yearly and its location alternates between North America, the Pacific Rim and Europe. IPRM'08 constitutes the 20th anniversary of this long established major event and will be held in Versailles, 25th - 29th May 2008.
In addition to the technical programme with plenary, invited and contributed presentations, together with two short courses, the conference also hosts a technical exhibit. A rump session devoted to 'hot topics' in the Conference technical scope is also organised.
The following five topical areas will be addressed:

Bulk crystal growth and characterisation
- Epitaxy and hetero-integration
- Optoelectronic devices and related processing
- Electron devices and related processing
- Nanostructures and novel materials

organized by

MAJOR SPONSORS

CO-OPERATING SOCIETIES