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Planar Concave Grating Demultiplexer with Distributed Bragg Reflection Facets

Joost Brouckaert, Wim Bogaerts, Pieter Dumon, Shankar Kumar Selvaraja, Gunther Roelkens, Dries Van Thourhout and Roel Baets

Ghent University – IMEC, Department of Information Technology (INTEC), Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium

Joost.Brouckaert@intec.UGent.be

***Abstract*—We present measurement results of a 4-channel silicon-on-insulator grating demultiplexer fabricated in a CMOS-line. On-chip loss is reduced below 4.5dB over a broad wavelength range by replacing each facet by a second order Bragg reflector.**

I. Introduction

One of the key components in wavelength division multiplexing (WDM) optical communication systems is the wavelength (de)multiplexer. The two main device technologies available today for implementing this functionality are Arrayed Waveguide Gratings (AWGs) [1] and Planar Concave Gratings (PCGs) [2]. Both these devices were recently fabricated on a nanophotonic silicon-on-insulator (SOI) platform [1], [3]. This material system has gained much research attention in recent years due to several factors and research developments. First of all, passive photonic components can be fabricated on a waferscale in a CMOS-line. Second, the large index contrast between silicon and silica allows to dramatically reduce the size of these devices by making use of nanophotonic waveguides.

We recently showed that the nanophotonic SOI platform - consisting of a 220nm thick Si layer on top of 1µm thick SiO_2 burried layer on a Si substrate – offers certain specific advantages for the fabrication of PCGs as compared with other material systems. Besides the reduction in size, performance can be increased due to the fact that the grating facets only need to be etched 220nm deep [3].

In this paper, we show that the insertion loss can be further decreased down to 2.2dB by coating the facets with gold and down to 2.4dB by replacing each grating facet with a second order Bragg reflector without any extra processing steps.

II. Design and fabrication

A. Grating demultiplexer design

The layout of the PCG is shown in Fig. 1. This device is discussed in detail in a previous publication [3]. The footprint of the device including photonic wire access waveguides is 280 x 150µm^2. The design is based on the Rowland geometry:

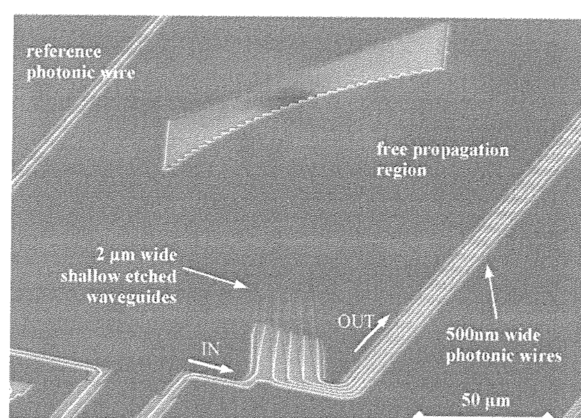

Fig. 1. SEM picture of 1x4 PCG demultiplexer.

the input and output waveguides are positioned on a circle with a radius of 94µm and the curved grating sits on a 188µm radius circle. The order of diffraction is 10 and the tapered entrance and exit waveguides are 2 µm wide with a spacing of 5 µm between the centers of the output waveguides along the Rowland circle. The angle between the input waveguide and the grating pole is 41°. This configuration results in a linear dispersion of 0.25µm/nm. The 31 facets are individually blazed to maximize the transmission of the two central output channels and the projected grating period is 4.35µm. Simulations are based on scalar diffraction theory and predict a free spectral range of 115nm around a central wavelength of 1550nm. The four output channels are separated by 20nm, making the device suitable for coarse WDM applications.

Structures were defined with 248nm and 193nm deep-UV lithography, and transferred into the silicon using ICP-RIE etching. The fabrication process is described in detail in [4]. The lithography is a two step process which combines deep- and shallow etching. For the definition of the grating and the photonic wires, the 220nm thick Si layer is etched through. A more shallow etch (70nm) is used for the definition of the fiber couplers and the 2µm entrance- and exit waveguides on the Rowland circle. The fiber couplers are gratings that convert the mode between a broad access waveguide and the fiber to

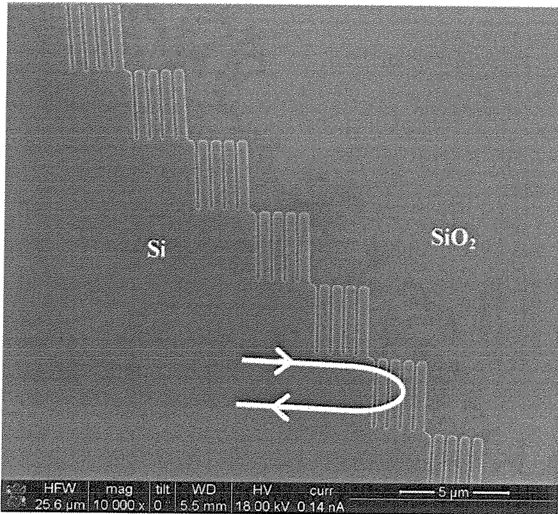

Fig. 2. Top view of DBR-type grating facets.

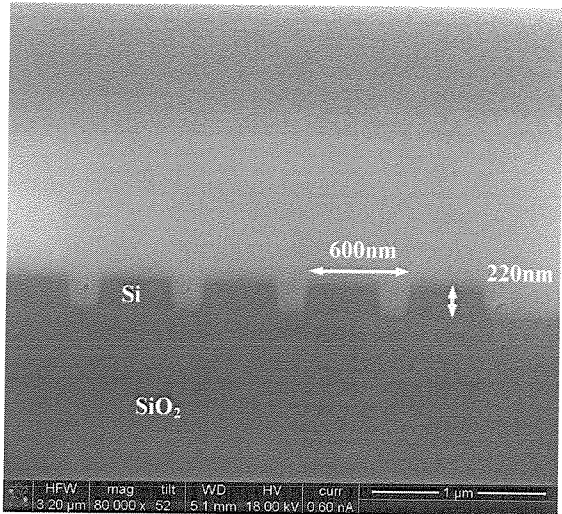

Fig. 3. Cross-section SEM picture of a 4-period DBR.

allow characterization of the component [5].

The largest contribution to the total insertion loss of this PCG demultiplexer is caused by the Fresnel loss (4.6dB) at the grating facets. The non-verticality of the grating facets (10.5°) only causes 0.3dB of additional loss, resulting in a total facet reflection loss of 4.9dB. PCGs fabricated in other material systems have a several micrometer thick free propagation region with deeply etched grating facets. Sidewall non-verticalities as reported here would completely destroy the transmission characteristics of these devices [3].

B. Gold coated facets

A popular technique to reduce the reflection loss at the grating facets is to coat the backside with a layer of Ti/Au. This is mostly done by means of tilted evaporation. A drawback of this method is that is can not be carried out on a waferscale. We applied another technique: before stripping the resist used to define the deeply etched structures (wires, broader waveguides and diffraction gratings), we evaporated a 220nm thick Ti/Au layer on the deeply etched gratings making use of a plastic evaporation mask to cover other deeply etched trenches followed by lift-off. This process was carried out on cleaved dies. However, it could be carried out on a waferscale.

C. DBR-type facets

The main drawback of the Au coating is that it requires several extra processing steps (evaporation mask, evaporation and lift-off). This can be avoided by changing the design of the grating facets. By replacing each single facet by a distributed Bragg reflection (DBR)-type facet, the reflection loss can also be significantly reduced without the need of extra processing. We propose a deeply etched second order DBR consisting of 4 periods as can be seen in Fig. 2 and Fig. 3. Fig. 4 shows the simulated reflection loss of a DBR-type facet consisting of 4 600nm periods and vertical sidewalls. Reflection loss below 0.5dB can be obtained in the entire 1.5-1.6µm wavelength range using a trench width of 130nm. These DBRs are also very tolerant on fabrication errors. A

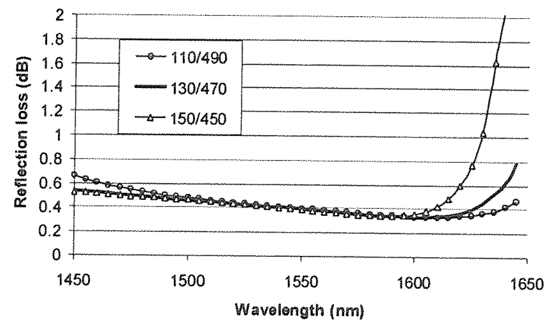

Fig. 4. Simulation results of the reflection loss of a 4-period DBR-type facet. The period is 600nm and the trench width varies from 110nm to 150nm, the unetched part from 450nm to 490nm. Perfect vertical sidewalls are supposed.

15% trench width deviation doesn't result in a higher loss for wavelengths from 1.5µm up to 1.6µm as can be seen in Fig. 4.

III. Measurement results

Light from a single mode fiber is coupled into the nanophotonic waveguides using shallowly etched fiber couplers [5]. The measured transmission spectra are for TE-polarized light and are normalized to a reference photonic wire waveguide (Fig. 1).

A. Gold coated facets

Fig. 5 shows the transmission spectrum of two 1x4 demultiplexers, fabricated with 248nm DUV-lithography. As can be seen, the transmission spectra are slightly disturbed by the high noise floor of the measurement setup. The spectra of PCGs with uncoated flat facets and Ti/Au coated flat facets are superimposed. The on-chip loss of the central channels of the uncoated device is ~6.7dB. The largest contribution of 4.9dB is caused by the reflection loss at the grating facets as mentioned earlier (taking into account a 10.5° sidewall non-

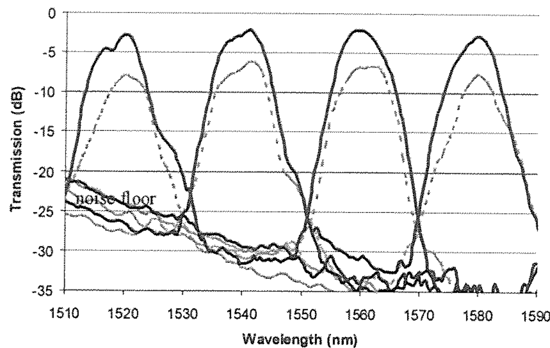

Fig. 5. Transmission spectrum of a 1x4 demultiplexer fabricated with 248nm DUV lithography. Demultiplexers with uncoated (dashed line) and Ti/Au coated facets are compared.

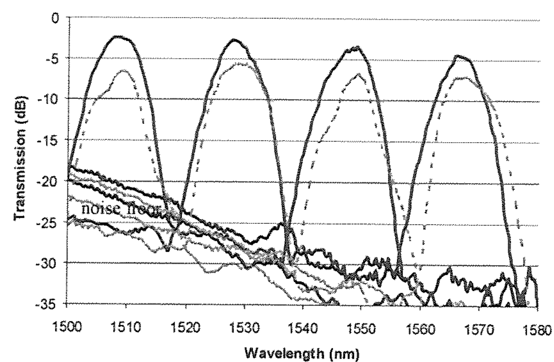

Fig. 6. Transmission spectrum of a 1x4 demultiplexer fabricated with 193nm DUV lithography. Demultiplexers with flat (dashed line) and DBR-type facets are compared.

verticality). Other contributions are diffraction loss of 0.5dB and excess loss due to grating profile imperfections, which adds 1.3dB.

The insertion loss of the Ti/Au coated device is 4.5dB lower resulting in an insertion loss of only 2.2dB for the central channels. It's important to notice that the reflectivity enhancement is rather constant over the operational wavelength range of the device. This means that the Fresnel reflection loss is reduced from 4.6dB down to 0.1dB (see section II).

B. *DBR-type facets*

Fig. 6 shows the transmission spectrum of the same device, but now fabricated with 193nm DUV-lithography. The spectra of PCGs with flat facets and DBR-type facets are compared. The loss of the central channels of the flat facet design is ~6.3dB. Again, 4.9dB is caused by reflection loss, 0.5dB by diffraction loss. This means that 0.9dB is caused by grating profile imperfections. This value is slightly better as compared with the PCG fabricated with 248nm DUV lithography. This means that a more perfect grating profile is obtained using 193nm DUV lithography.

The insertion loss of the device with DBR-type facets is 3.4dB better on average as compared with the flat facet device. However, it's important to notice that the reflection enhancement decreases for longer wavelengths. As can be seen in Fig. 4, the insertion loss varies from 2.4dB for the shortest wavelength channel up to 4.5dB for the longest wavelength channel. This discrepancy between measurements (Fig. 6) and simulation results (Fig. 4) can be explained by fabrication imperfections of the DBRs. As can be seen from the cross-section view (Fig. 3), the non-verticality of the sidewalls is about 5°, whereas the non-verticality of the isolated sidewall is about 10°. This was not taken into account in the simulation results (Fig. 4). On top of that, profile measurements revealed a grating period of 600nm, consisting of a 430nm wide unetched part and a 170nm deeply etched trench whereas a 470nm/130nm DBR period was expected.

IV. Conclusions

We presented measurement results of ultracompact PCG demultiplexers fabricated on a nanophotonic SOI platform. The on-chip loss was reduced below 4.5dB for wavelengths ranging from 1.5µm up to 1.6µm by utilizing DBR-type grating facets. This method doesn't require extra processing steps and simulation/measurement results suggest that the insertion loss can reduced to below 2.4dB over the entire wavelength range, only slightly higher as compared with the Ti/Au coated facets.

The higher than expected insertion loss non-uniformity is caused by fabrication imperfections, which can be avoided by tuning the reflector design and DUV-lithography process. If available, measurement results of denser demultiplexers will be presented at the conference.

Acknowledgment

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