Heterogenous integration of InP/InGaAsP photodetectors onto ultracompact Silicon-on-Insulator waveguide circuits

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ABSTRACT

We present the heterogeneous integration of InP/InGaAsP photodetectors onto ultracompact Silicon-on-Insulator (SOI) waveguide circuits using benzocyclobutene (BCB) die to wafer bonding. This technology development enables the integration of a photonic interconnection layer on top of CMOS. Fabrication processes were optimized and the transfer of a passive Silicon-on-Insulator waveguide layer using BCB was assessed.

Keywords: Heterogeneous integration, photodetectors, BCB

1. INTRODUCTION

In future generations of electronic circuits a severe bottleneck is expected on the global interconnection level. With decreasing device dimensions, it is increasingly difficult to keep propagation delays acceptable and even with the most optimistic estimates for conductor resistivity and dielectric permittivity, the projected performance roadmap will not be met [1]. Therefore there is a need for radically different interconnect approaches and, as indicated by the ITRS-roadmap, one of the most promising solutions is the use of an optical interconnect layer. An optical interconnect layer could allow for an enormous bandwidth increase, for immunity to electromagnetic noise, for a decrease in the power consumption, the possibility for synchronic operation within the circuit and with other circuits and for a reduced immunity to temperature changes [2]. To achieve an optical interconnection layer on top of a CMOS electronic circuit we propose to bond a Silicon-On-Insulator (SOI) optical waveguide layer on top of the electronic circuit. In recent years, SOI has emerged as a promising platform for high density passive integrated optics fabricated on a wafer scale.
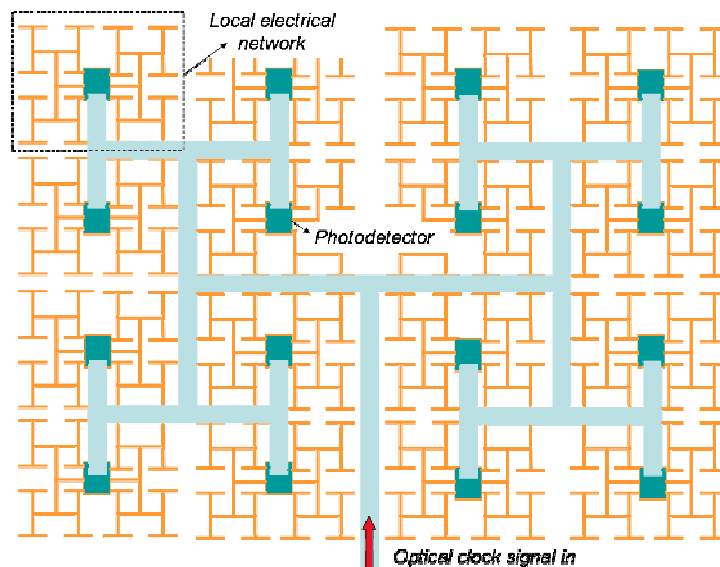

Figure 1: Optical clock distribution tree

SOI consists of a thin silicon layer on top of an oxide cladding layer carried on a bare silicon wafer. With its silicon core (n = 3.45) and its oxide cladding (n = 1.45) it has a high vertical refractive index contrast. Due to the high index contrast very compact wavelength scale components can be fabricated. Also, both the silicon and the oxide are transparent at the telecom wavelengths of 1.3μm and 1.55μm. The fabrication of the SOI waveguide circuits can be done using standard Deep UV lithography making it mass manufacturable [3]. Although Silicon-on-Insulator can easily be used as a platform for passive waveguiding, an optical interconnection layer also requires photodetectors and light emitters.

For active opto-electronic components like laser diodes, modulators and detectors, III-V material remains the workhorse of telecom industry due to its superior performance. Therefore, there is also the need to integrate III-V active components on top of the CMOS circuits. Depending on the application, different types of active opto-electronic devices are needed. For a clock distribution function there is the need for high speed photodetectors on top of an SOI H-tree waveguide circuit as shown in figure 1 assuming an off chip optical clock signal generation. For optical datalinks both laser diodes and/or modulators are needed together with photodetectors. As we focus on telecommunication wavelengths, InP/InGaAsP is the material choice of interest.

As the fabrication process needs to be as much as possible on a wafer scale to be industrially viable, we propose to follow a fabrication procedure as depicted in figure 2. The bonding method is not yet specified as there are different ways to achieve this task as will be discussed in section 2. The fabrication procedure consists of two bonding steps. In a first step unprocessed III-V dies are bonded, epitaxial layers down, to the SOI waveguide wafer. The size of the dies depends on the application. As unprocessed dies are bonded, alignment accuracy is not stringent and the positioning of the individual dies can be done using a fast pick and place machine. After this die to wafer bonding step, the InP substrate is removed, using an InGaAs layer as an etch stop layer. After substrate removal only a thin epitaxial layer stack remains in which subsequently active devices can be fabricated, lithographically aligned to the underlying SOI waveguide circuit. In a second step the photonic waveguide wafer, containing the clock distribution trees and/or optical datalinks is bonded after testing to the CMOS wafer surface. The Silicon substrate is removed and electrical connections are made.
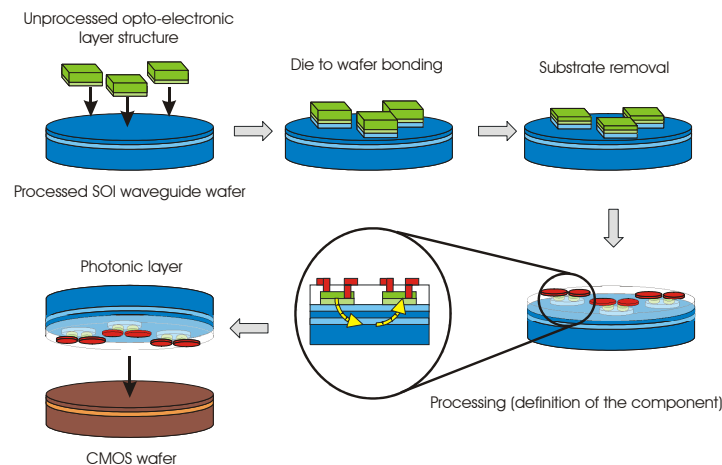

Figure 2: Process flow for the integration of a photonic interconnection layer on top of CMOS

The choice to first bond the InP dies onto the SOI wafer and subsequently bond the photonic wafer to the CMOS wafer is somewhat arbitrary. An equally interesting option would be to first bond the SOI waveguide wafer to the CMOS wafer, removing the silicon substrate and bonding the III-V components to the CMOS/SOI layer stack.

2. BONDING

There are several ways to accomplish the die to wafer or wafer to wafer bonding. As an optically transparent bonding layer is required, direct wafer bonding using a SiO_2 bonding layer [4] and adhesive wafer bonding using a polymer bonding agent [5] are the two main candidates. As direct wafer bonding requires high quality surfaces considering surface roughness and planarity, this technique requires advanced CMP technology to get the appropriate surface conditions for bonding of processed wafers. As the quality of InP wafers is less than Silicon wafers and very much dependent on wafer supplier additional effort is needed to do direct wafer bonding in a reproducible way. Using a polymer bonding agent reduces these problems because of the planarizing action of spin-coating the polymer layer on the substrate. Therefore, we focused in our work on the use of adhesives for the layer transfer. Both benzocyclobutene (BCB) [6] and spin on glass (SOG) [7] were investigated as bonding agents. The degree of planarization of both materials was assessed by bonding a III-V layer on top of an SOI waveguide circuit. SEM cross section pictures are shown in figure 3 [8].
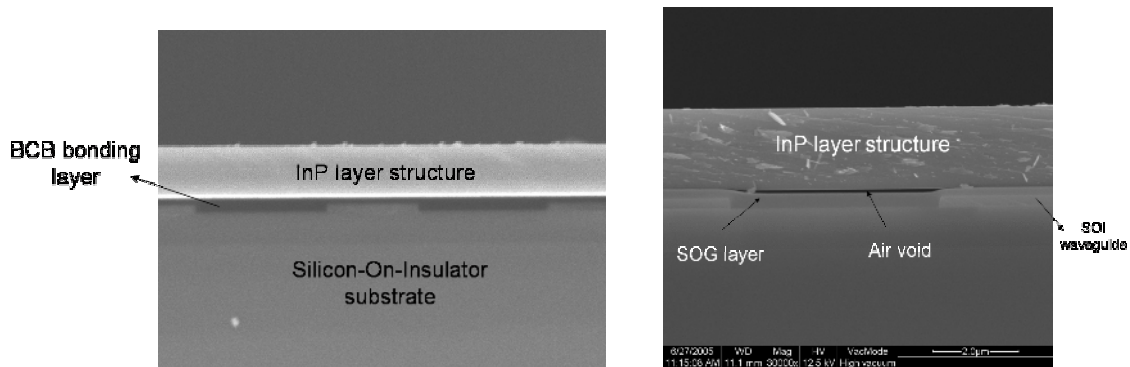

Figure 3: Comparison of BCB bonded InP dies (left) and SOG bonded InP dies (right)

Although the bonding layer thicknesses were equal (about 200nm) and the topography is identical, the planarization of SOG is less than that of BCB leaving interfacial voids at the SOG/InP interface while there was no observation of defects in the BCB case. Due to the superior planarization of BCB, this material was used as a bonding agent for the fabricated devices.

3. PHOTONIC INTERCONNECTION LAYER ON CMOS

In a first step, the influence of transferring an optical waveguide layer from its original Silicon host substrate to a transfer substrate was assessed. Therefore, long folded optical waveguide structures with various lengths were defined onto an SOI substrate to measure SOI waveguide losses and bend losses. The SOI waveguide layer consisted of a 220nm thick Silicon core layer on a 1μm thick oxide buffer layers. Waveguides were about 480nm wide. After loss measurement, a 3 μm thick BCB layer was spin coated on the SOI structures and this layer was soft-cured at 210C. Again a 3μm BCB layer was spin coated on the transfer substrate, being a semiconductor grade Pyrex 7740 substrate, and SOI die and transfer substrate are attached and cured at 250C to fully cure the BCB bonding layer. After bonding, the Silicon substrate is thinned by mechanical grinding down to 100μm thickness. The rest of the substrate is removed by wet chemical etching using 20 wt% KOH at 70C using the oxide buffer layer as an etch stop layer. An optical microscope image of a transferred SOI waveguide layer is shown in figure 4a. The comparison of optical waveguide losses before and after layer transfer is shown in figure 4b. A small increase of waveguide losses is visible, although sufficiently small for application in a real device.

4. BCB BONDING OF INP DIES

As in our application small InP dies need to be bonded to an SOI waveguide circuit, the bonding strength of the BCB bonded dies was assessed using a Dage die shear test setup. Factors that influence the bonding strength are surface quality, particle contamination and surface preparation for bonding. While it is clear

that particles can create voids at the bonding interface it is also known that adsorbed organic compounds can reduce the bonding strength. Therefore, three types of surface preparations were compared. Acetone/Isopropanol/deionized water clean, an oxygen plasma clean and an HF InP surface passivation were compared.
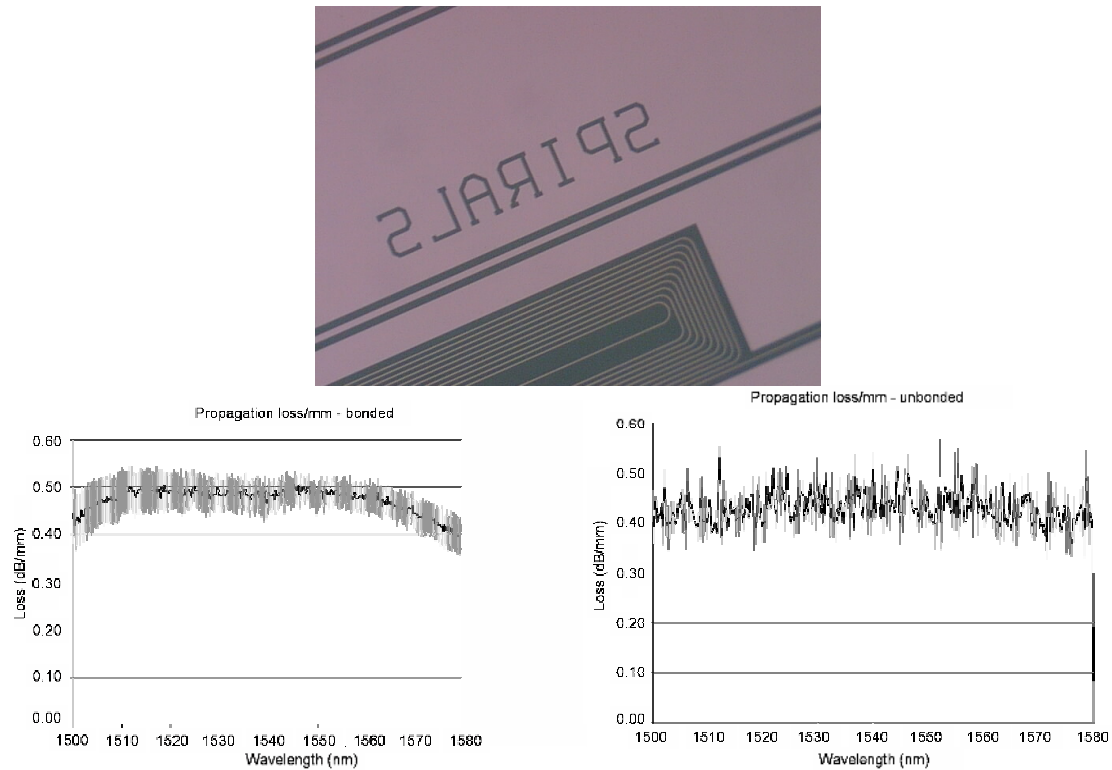

Figure 4: Optical microscope image of a transferred SOI waveguide layer and comparison of waveguide losses before and after bonding and substrate removal

Both thick BCB layers (3μm bonding layer thickness) and ultra-thin bonding layers (300nm) were used to individually identify the influence of surface quality and particle contamination on one hand and the chemical bonding on the other hand, as the influence of particles is reduced when applying thick bonding layers. Figure 5a shows measured die shear strength for thick BCB bonded InP dies. It is clear that oxygen cleaning plasma performs less than Acetone/IPA/DI and HF passivation, while there is a lot of fluctuation on the results for Acetone/IPA/DI cleaning. To look at the influence of surface quality and particle contamination, Acetone/IPA/DI clean and HF passivation were compared for ultra thin BCB bonding (300nm bonding layer) where the effect of defects at the interface is more prominent. Results are shown in figure 5b, which shows that HF removes particles better and more reproducibly than Acetone/IPA/DI clean. We suppose that immersing an InP surface in an HF solution removes the $InPO_x$ oxides at the surfaces [9] thereby also lifting of particles. After oxide removal a hydrogen terminated surface is left, to which organic compounds are only weakly physisorbed. These can be easily removed by heating the sample before bonding, therefore resulting in a more reproducible bonding strength.
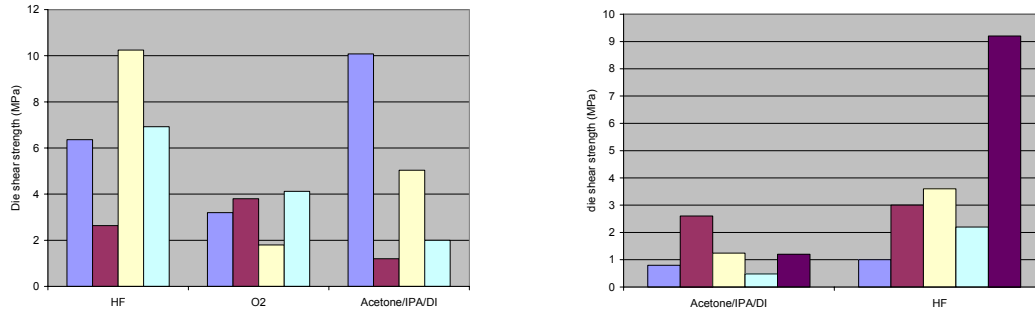
Figure 5: Measured die shear strength for 3μm BCB bonding layer thickness (left)
and 300nm bonding layer thickness (right)

5. INP/INGAASP PHOTODETECTORS ON SOI WAVEGUIDE CIRCUITS

To show the feasibility of integrating InP/InGaAsP active components onto an SOI waveguide layer, InP/InGaAsP photodetectors were fabricated on top of passive wavelength selective SOI filters. The filter structure consists of 4 to 6 ring resonators placed in series performing a wavelength selection operation. This type of components could be used for coarse wavelength division multiplexing on chip. To inject light from an optical fiber into the SOI waveguide circuit a grating coupler was used as shown in figure 6a [10]. Grating coupler period is 610nm and has a duty cycle of 50% and is etched 50nm deep. To diffract light in the SOI waveguide towards the photodetector, the same type of grating coupler was used as shown in figure 6b. After waveguide and grating fabrication using standard 248nm deep UV lithography using an ASML PAS5500/750 stepper, a 3μm thick BCB layer was spin coated onto the substrate and an InP die was bonded at 150C onto the substrate. Finally, the BCB adhesive layer was cured at 250C. After bonding, the InP substrate was removed by grinding down to 50μm and etching chemically using $3HCl:1H_2O$ until a thin InGaAs etch stop layer is reached [11]. The remaining epitaxial III-V layer stack consists of an n-doped 1μm thick InP undercladding layer, a 120nm thick InGaAsP absorption layer (1.55μm bandgap wavelength) and a 1.8μm p-doped InP topcladding. After substrate removal the detector mesa is etched through the absorbing layer and a AuGeNi n-type contact is deposited. After applying a BCB isolation layer, top windows are opened and a TiAu p-type contact is deposited and annealed. A top view of the fabricated devices before top contact
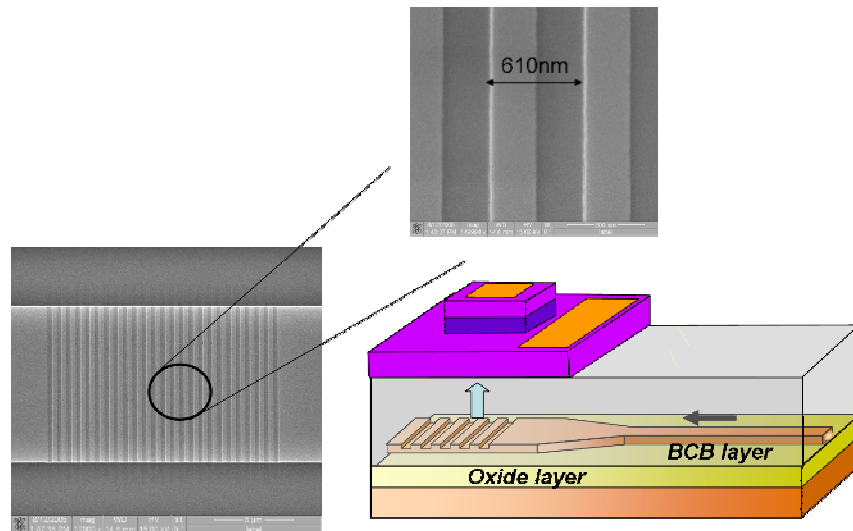

Figure 6: grating coupler structure to inject light into waveguide circuit and to diffract light towards a photodetector.
Grating period is 610nm and is etched 50nm into the Silicon waveguide core.

definition is shown in figure 7a. The dark current of the 10μm x 10μm device was 0.3nA at a reverse bias of 1V. The responsivity of the photodetectors was measured to be 0.02A/W referenced to the SOI waveguide power. Devices were bonded on a 4 racetrack resonator filter (with varying racetrack resonator circumference) acting as a wavelength demultiplexer. An SEM view of the fabricated SOI structure is shown in figure 7b.

Measured photodetector current versus wavelength is shown in figure 8a for the waveguide circuit shown in figure 7b. The simulated spectrum of the light injection from an optical fiber using a grating coupler is superimposed. By carefully tuning the radius of the racetrack resonators bandpass filter operation can be achieved. The measured photocurrent versus wavelength of a 6 ring resonator bandpass filter is shown in figure 8b. 13dB extinction ratio was achieved.
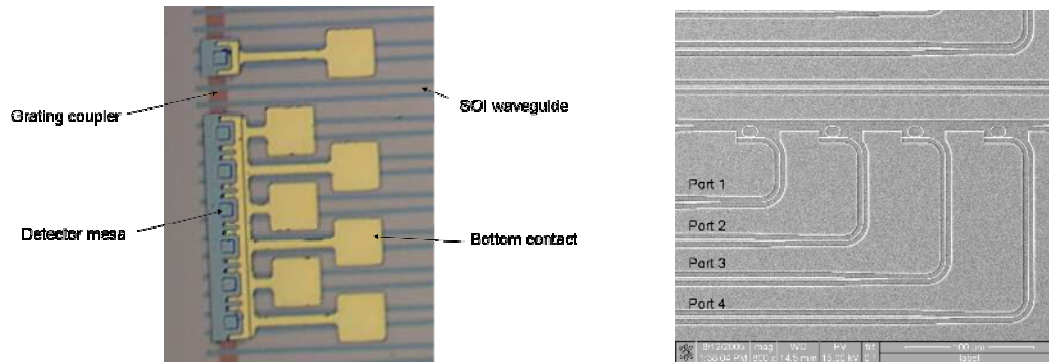

Figure 7: Photodetectors before top contact definition and fabricated SOI waveguide structures. The waveguide bend radius is varied by 15nm for every ring resonator (nominal radius 4μm)

As the measured device responsivity is rather low, we will show that by optimizing the III-V layer structure and by optimizing oxide buffer layer thickness, BCB layer thickness and device length, a drastic increase in efficiency is possible. This is due to the influence of the reflections at the InP/BCB interface and the Silicon/Oxide interface which determine the grating coupling length and directionality (being the fraction of the power coupled upwards versus the total amount of outcoupled power) of the grating due to constructive and destructive interference as is shown in figure 9 . Simulations are performed using CAMFR, a fully vectorial two-dimensionsal simulation tool based on eigenmode expansion [12]. TE polarization is assumed in the simulations.
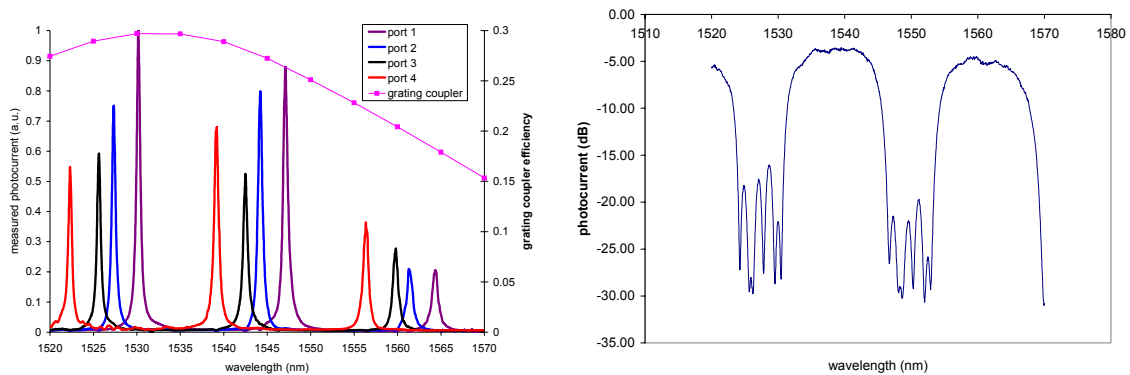

Figure 8: Measured photodetector current for a 4 racetrack resonator demultiplexer (left) and for a 6 racetrack resonator bandstop filter (right). About 13dB extinction ratio is achieved for the bandstop filter.
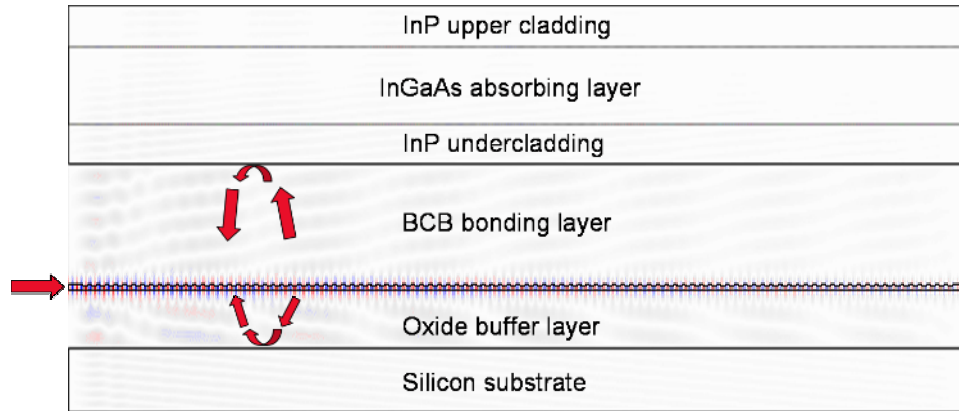
Figure 9: Simulation of a grating coupler + detector and the influence of reflections

A first optimization exists in replacing the 120nm InGaAsP absorbing layer (bandgap wavelength 1.55μm) by a 2μm InGaAs absorbing layer which is a compromise between responsivity, device speed (transit time limited) and ease of thick epitaxial layer growth. As the bandgap of lattice matched InGaAs is about 0.75eV, absorption coefficients are higher at 1550nm and longer wavelength operation is also possible. In a second optimization run, the oxide buffer layer thickness and BCB bonding layer thickness was varied. Results are shown in figure 10a, which shows the absorbed power fraction for a 50μm long device at 1550nm (2μm InGaAs absorbing layer). There is a clear optimum around a BCB thickness of 3μm and an oxide buffer layer thickness of 1.4μm. If we compare figure 10a with the simulated absorbed power fraction of the fabricated devices (120nm InGaAsP absorbing layer, 3μm BCB layer, 1μm oxide buffer layer and 10μm long) in figure 10b, we can see that an increase of about a factor 20 in responsivity is achievable by changing the design parameters.
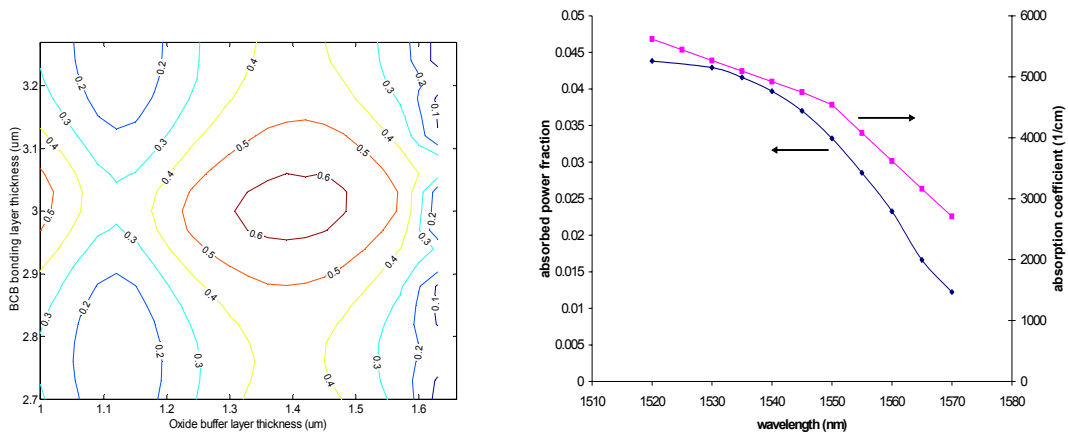

Figure 10: Optimization of oxide buffer layer thickness and BCB bonding layer thickness for a 50μm long device (left) and simulated absorption fraction for the fabricated devices. The InGaAsP absorption spectrum used in the simulations is also added.

6. CONCLUSIONS

We presented the technology development for the integration of a photonic interconnection layer on top of a CMOS IC. A photonic interconnection layer on top of CMOS is a possible solution for the interconnect bottleneck on the global interconnection layer of future generations electronic ICs. The bonding of Silicon-on-Insulator waveguide circuits onto a transfer substrate was assessed, showing a sufficiently small increase in waveguide losses. Bonding of InP dies onto processed SOI circuits was developed. HF surface passivation of InP dies resulted in the most reliable bonding strengths. Based on this technology first

generation photodetectors were integrated on top of functional optical circuits. It is shown that an excellent responsivity can be obtained by optimization of the InP/InGaAsP layer stack and the SOI structure.

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