Heterogeneous integration of III-V membrane devices and ultracompact SOI waveguides

G.Roelkens, *Student Member IEEE*, D. Van Thourhout, *Member IEEE*, R.Baets, *Senior Member IEEE*

***Abstract*—We present and analyze two schemes for efficient, large bandwidth and fabrication tolerant optical coupling of bonded III-V membrane active components to an underlying nanophotonic waveguide circuit fabricated in the Silicon-On-Insulator material system. Coupling of active membrane components to passive waveguides enables the integration of ultra compact passive waveguide circuits and active opto-electronic devices.**

***Index Terms*—Heterogeneous integration, thin-film opto-electronic components, Silicon-On-Insulator, nanophotonics.**

I. Introduction

The integration of different optical functions on a photonic IC fabricated using high yield wafer scale technologies is expected to result in systems-on-a-chip that outperform their discrete and die level integrated counterparts in compactness, performance, complexity and cost. As a general system contains both active functions (amplification, switching, modulation, light emission and detection) and passive optical waveguides, different materials need to be integrated into a single system.

High index contrast waveguides are very attractive to be used in the passive waveguide layer. Optical circuits based on photonic wires and photonic crystals make ultra compact optical functions possible and the high index contrast allows very large scale integration of optical waveguides. Recently, low waveguide propagation losses were obtained for Silicon-On-Insulator (SOI) high index contrast nanophotonic waveguide structures [1][2]. Moreover, these waveguide structures are defined by deep UV lithography, the workhorse of CMOS technology [3], and wafer scale processes. Based on the considerations above, in this paper we will focus on the coupling of opto-electronic devices and passive nanophotonic waveguides in SOI.

The choice of active layer material is determined by the optical transparency of the SOI waveguide (λ>1.1μm) at the active material bandgap wavelength. We will concentrate on InP/InGaAsP active devices with a bandgap wavelength around 1.55μm.

The application of this integration technique is not limited to complex optical systems-on-a-chip. In future CMOS technology nodes the metal interconnections are no longer expected to satisfy the bandwidth needs, especially for the global interconnection level, where interconnection distances are the largest. According to the ITRS roadmap [4], a promising approach is the use of a photonic interconnection layer on top of CMOS. This layer may contain on-chip sources and detectors, coupled to an optical waveguide layer.

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II. Heterogeneous integration

A. Integration technique

Integration of different materials into a single system can be accomplished in a variety of ways. Direct growth of InP material on a Si substrate, results in high dislocation densities due to the large mismatch in lattice constant. This optically degrades the active layers. Eutectic bonding [5] using metal alloys results in non-transparent bonding layers. In direct waferbonding [6] two polished wafer surfaces are fused together. This technique allows an optically transparent bonding interface, but requires advanced CMP processing to bond processed SOI waveguide substrates and InP dies. An alternative approach – which is assumed in this paper - is to use an optically transparent adhesive layer spin coated onto the substrates, used as a bonding agent by curing the adhesive.

B. Membrane device definition

As the size of industrially available CMOS wafers and SOI waveguide wafers (up to 300mm) differ from the size of InP wafers (50-75mm) a ‘die to wafer’ bonding approach is needed. This implies that InP dies need to be picked, placed and bonded on a SOI wafer. As our intention is to couple active devices to nanophotonic waveguide structures, alignment is very stringent. This can only be achieved through lithographic alignment of SOI structures and active devices. Therefore, unprocessed InP dies are bonded to the SOI waveguide substrate, epi-layers down and then the InP substrate is removed using mechanical and chemical thinning until an etch stop layer is reached. This leaves a thin active film that can be processed subsequently, with structures lithographically aligned to the SOI waveguides. As the bonded dies are unprocessed, positioning accuracy is less

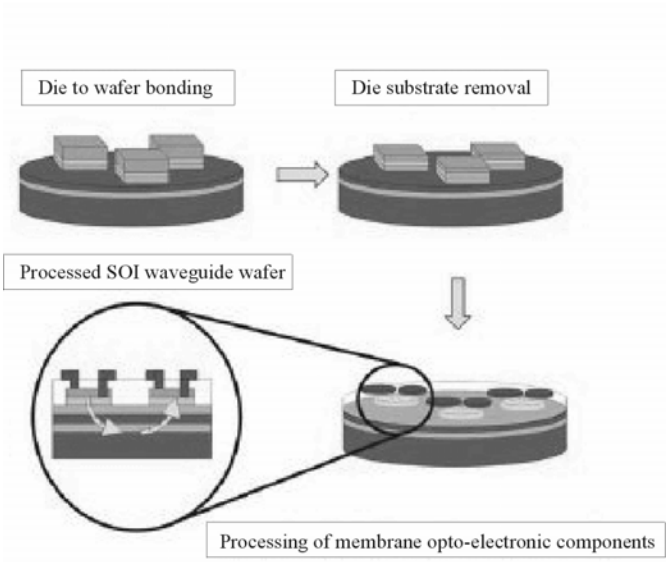

Fig. 1. Processing sequence for heterogeneous integration of III-V components and SOI waveguides

stringent. The processing sequence is shown in Fig. 1.

III. Coupling III-V and SOI

As different types of active devices need to be integrated in a general system, the coupling method will differ for each type of device. An important distinction is the direction of the optical path in the active component. If the optical path is perpendicular to the waveguiding direction in the SOI (e.g. a heterogeneously integrated VCSEL) a beam turning coupler is needed to couple light from III-V components to SOI and vice versa. In this paper however we focus on in-plane opto-electronic devices.

A usable coupling scheme needs to be efficient and compact, has a large optical bandwidth and is fabrication tolerant. Especially the tolerance on the bonding layer thickness is an important issue. Polarization independence is not required in a photonic interconnection layer application with on-chip sources, while a polarization diversity configuration can be applied for systems-on-a-chip for telecom applications [7]. In these configurations the incoming unpolarized light is split into two beams with orthogonal polarization state, both of which are subsequently independently processed in separate but identical devices and finally recombined.

Different ways of coupling light between the active components and the passive circuitry can be envisioned. The use of a grating structure to diffract guided waves to radiation modes and vice versa can result in very compact structures but has a reduced efficiency due to the limited directionality of the gratings and shows tight fabrication tolerances on both gratings due to the need for matching the grating angles and grating coupling lengths. The use of (grating assisted) vertical directional couplers can be highly efficient but is considered equally fabrication intolerant due to the periodic power exchange between both waveguides, resulting in a low bonding layer thickness tolerance, and the stringent requirement of phase matching two high index contrast waveguides in different material systems.

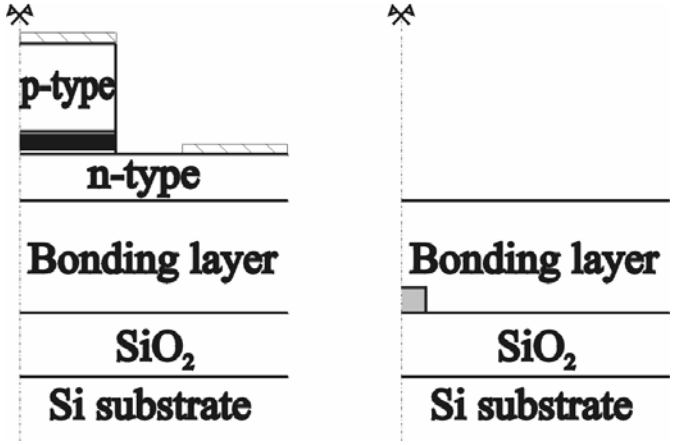

Fig. 2. InP membrane waveguide (left) and single mode high index contrast SOI waveguide (right).

In the following subsections two coupling schemes based on adiabatic tapers will be presented. The use of adiabatic tapers as mode transformers makes an efficient coupling with large optical bandwidth possible and allows a trade-off between fabrication tolerance and design compactness.

The first design is based on a thin film spin-on glass (SOG) adhesive bonding layer. Bonding layer thicknesses below 0.5μm have been shown in [8]. The second design is based on a thick film benzocyclobutene (BCB) bonding. Bonding layer thickness above 1μm is readily achievable [9]. Both materials are used in CMOS industry, respectively as metal isolation layer and passivation material. The coupling schemes are equally applicable to other transparent bonding materials, with comparable layer thickness and optical properties.

The active thin film layer structure consists of six 6.4nm thick 1% compressively strained $In_{0.76}Ga_{0.24}As_{0.79}P_{0.21}$ quantum wells separated by 5.5nm thick $In_{0.71}Ga_{0.29}As_{0.55}P_{0.45}$ barrier layers. The separate confinement layers are assumed 50nm thick $In_{0.83}Ga_{0.17}As_{0.37}P_{0.63}$ layers. The first and last barrier layer are 17nm thick [10]. The active waveguide is assumed 2.5μm wide. The thickness of the cladding layers depends on the coupling mechanism used.

The coupling schemes presented transform the fundamental mode of the active ridge structure to the fundamental mode of an SOI waveguide with a 220nm thick Si core layer. The bonded active ridge waveguide and a 600nm wide single mode SOI waveguide are shown in Fig. 2 on the same scale. Notice the large dimensional mismatch between both waveguides.

A. SOG bonding coupling scheme

The proposed coupling scheme is presented in Fig. 3. It consists of a double adiabatic taper structure to transform the fundamental waveguide modes. The first taper transforms the active waveguide mode to the fundamental mode of a passive InP membrane waveguide. This waveguide is formed in the n-

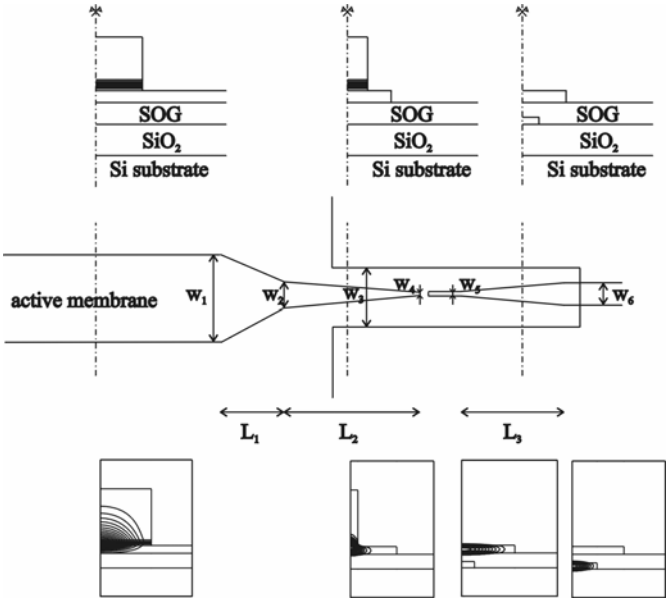

Fig. 3. SOG bonding coupling scheme – layout and mode transformation

type contacting layer, so propagation losses due to free carrier absorption are small. Subsequently, light is coupled from the InP membrane to the SOI waveguide using an SOI adiabatic taper coupler. This coupler is based on a phase matching condition of the fundamental modes of the SOI waveguide and the InP membrane. As the thickness of the SOI waveguide

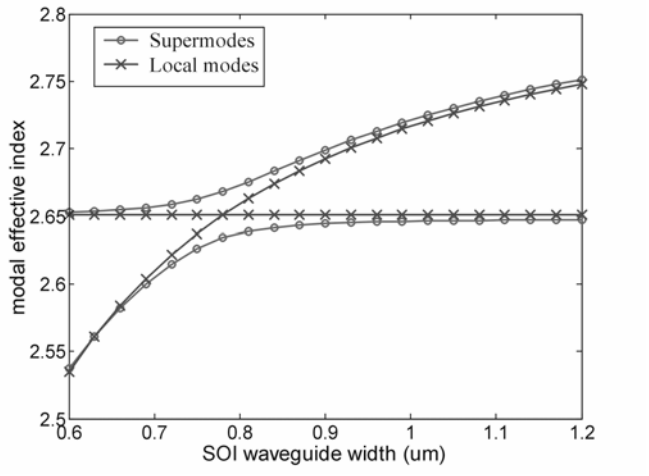

Fig. 4. SOI adiabatic taper operation principle – modal effective indices

is about λ/2n to be vertically single mode, the phase matching condition implies this is also needed for the InP membrane.

Fig. 4 shows the operation principle of the SOI adiabatic taper structure. TE effective indices of the supermodes of the taper structures as well as the effective indices of the local modes - these are the modes of the uncoupled waveguides - are plotted versus SOI waveguide width. A 275nm thick InP membrane is assumed (w_4=2.5μm) separated from the SOI waveguide by a 300nm thick SOG layer (n=1.4) . When one supermode is excited and that supermode is transformed adiabatically over the phase matching area, light is coupled from one waveguide to the other. The minimum adiabatic

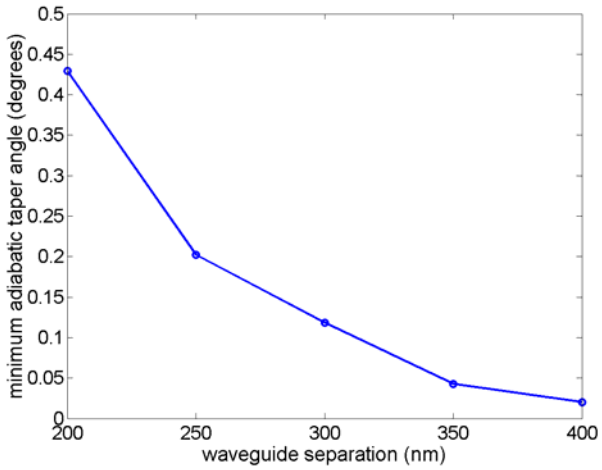

Fig. 5. Minimum adiabatic SOI taper angle versus waveguide separation for SOG bonding coupling scheme

taper angle is critically dependent on bonding layer thickness as shown in Fig. 5. While the exact taper length depends on taper waveguide shape – which is determined by the required tolerance of the design to fabrication variations - a waveguide separation below 0.4μm is needed to design compact, efficient couplers. Parameters for adiabatic InP waveguide mode transformation and for an adiabatic linear SOI taper are given in Table I for a waveguide separation of 300nm. The narrow InP taper tips can be defined using deep UV lithography. Simulations show less than 1dB coupling loss over the 1500nm-1600nm wavelength range. As this coupling scheme shows very low reflection it can be used for heterogeneous integration of semiconductor optical amplifiers and passive nanophotonics.

B. BCB bonding coupling scheme

Because of the critical dependence on the bonding layer thickness in the SOG bonding coupling scheme, an alternative coupling scheme that reduces this dependence is presented in

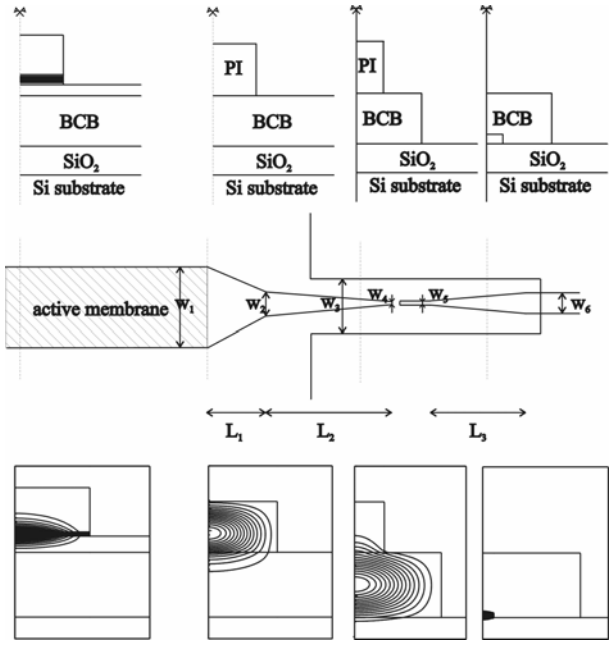

Fig. 6. BCB bonding coupling scheme - layout and mode transformation

Fig. 6.

The structure is based on bonding using BCB (n=1.55). Due to the higher refractive index of the BCB compared to the SiO_2 buffer layer (n=1.45), an additional waveguide is formed. The coupling mechanism is conceptually equivalent to the SOG bonding coupling scheme and transforms the waveguide mode using a double adiabatic taper structure. The first adiabatic taper is implemented in a polymer waveguide layer, which is butt-coupled to the active ridge waveguide [11]. This implies an intrinsic reflection at the semiconductor/polymer interface and a reduced efficiency due to butt-coupling loss. This loss is a function of the index contrast between the polymer core and BCB cladding layer because of the mode profile mismatch between the fundamental waveguide modes in the active membrane and polymer waveguide. Reflection and transmission at the semiconductor/polymer interface are shown in Fig. 7 for an optimized waveguide geometry.

Fig. 8 shows the dependence of the minimum adiabatic taper angle of the SOI waveguide as a function of bonding layer thickness. Compared to Fig. 5 this dependence is drastically reduced. Using the parameters noted in Table I the transmission loss of the double adiabatic taper structure is simulated to be below 0.5dB over the 1500nm-1600nm wavelength range. A refractive index difference between polymer core and cladding of 0.05 is assumed. The bonding layer is assumed to be 3μm thick (w_4=3.5μm), while the optimized polymer core thickness is 2.3μm. The narrow SOI taper tip is needed for low insertion loss. Definition of these taper tips requires e-beam lithography [12]. The intrinsic reflection at the semiconductor-polymer interface enables the heterogeneous integration of edge emitting lasers and passive nanophotonics. In applications where the reflection into the active waveguide has to be avoided angled facets can be used.

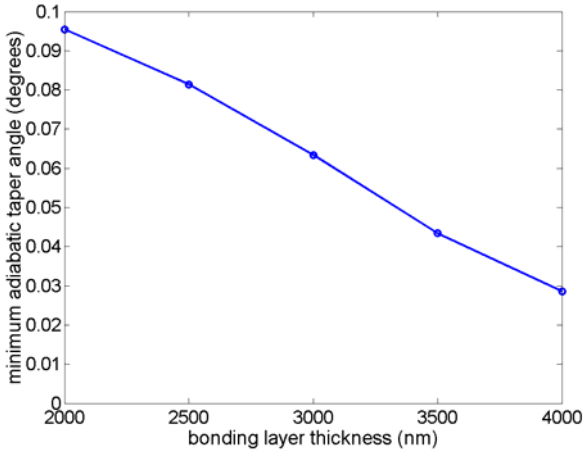

Fig. 8. Minimum adiabatic taper angle versus bonding layer thickness for BCB bonding coupling scheme

TABLE I
PARAMETERS WAVEGUIDE STRUCTURES
BCB BONDING VERSUS SOG BONDING

Parameter	Value	Parameter	Value
$w_{1,SOG}$	2.5μm	$w_{1,BCB}$	2.5μm
$w_{2,SOG}$	0.6μm	$w_{2,BCB}$	1.8μm
$w_{3,SOG}$	2.5μm	$w_{3,BCB}$	3.5μm
$w_{4,SOG}$	0.2μm	$w_{4,BCB}$	1.1μm
$w_{5,SOG}$	0.6μm	$w_{5,BCB}$	0.05μm
$w_{6,SOG}$	1.2μm	$w_{6,BCB}$	0.3 μm
$L_{1,SOG}$	80μm	$L_{1,BCB}$	80μm
$L_{2,SOG}$	50μm	$L_{2,BCB}$	180μm
$L_{3,SOG}$	160 μm	$L_{3,BCB}$	130μm

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IV. CONCLUSIONS

Two schemes to efficiently couple III-V active components and SOI photonic wires are presented. One bonding scheme requires a thin bonding layer (<0.4μm) and has no intrinsic reflections, which makes it useful for the heterogeneous integration of semiconductor optical amplifiers and passive nanophotonics. A second design is more tolerant to bonding layer thickness variation and has an intrinsic reflection, which makes it useful for the heterogeneous integration of edge emitting lasers.

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