Integration of Photonic Functions
in and with Silicon

Roel Baets, Wim Bogaerts, Pieter Dumon, Günther Roelkens, Ilse Christiaens, Kurt De Mesel,
Dirk Taillaert, Bert Luyssaert, Joris Van Campenhout, Peter Bienstman, Dries Van Thourhout,
Vincent Wiaux, Johan Wouters, Stephan Beckx

R. Baets, W. Bogaerts, P. Dumon, G. Roelkens, I. Christiaens, D. Taillaert, B. Luyssaert, J. Van Campenhout, P.
Bienstman and D. Van Thourhout are with the Department of Information Technology,
Ghent University-IMEC, Gent, Belgium E-mail: roel.baets@intec.ugent.be .
K. De Mesel is currently with AMI Semiconductor Belgium in Oudenaarde.
V. Wiaux, J. Wouters and S. Beckx are with the Silicon Process Technology Division of IMEC vzw, Leuven, Belgium

Abstract

Siliconis gaining importance in photonic systems on a chip, either because of the importance of integrating photonic functions with electronic functions or because of the potential of Silicon-based technology for photonics as such. In this paper we discuss two distinct developments. The first is the development of nano-photonic integrated circuits based on photonic crystals or photonic wires. The second is the development of heterogeneously integrated active photonic components on top of Silicon by means of wafer bonding.

1. Introduction

In the past Silicon has not been of major importance for photonic functions. Discrete photonic components were generally made in the most suitable material and - with the exception of detection of visible and near-infrared light - this was generally not Silicon but rather other materials such as compound semiconductors, ferroelectric crystals, glasses, polymers, liquid crystals etc.

This is now changing rapidly. The drive for integration of complex functions on a single chip is gaining importance in photonics. The rationale for integration is similar to what it is in micro-electronics: performance, economy of scale, compactness and reliability. In photonics there is an extra reason to integrate as many functions as possible on a chip: coupling light from one component to another typically requires accurate – and therefore expensive – alignment. When integrating functions this alignment is largely taken care of by means of lithography.

Given the call for more integration there are several reasons why Silicon comes into the picture. First of all many photonic functions need to be integrated with (Silicon) electronic circuitry and in a variety of cases it makes sense to build the photonic functions directly on top of the Silicon chip. To do so with high yield and low cost the processes involved should as much as possible be wafer-scale processes.

Secondly the technologies used in Silicon microelectronics are much more mature than those used for most other material systems. Therefore if a particular function can be realised by means of the Silicon material, there is an advantage to do so, certainly if the process steps involved are essentially no different from those used for CMOS-processing. This is the case when building passive waveguide-based circuits as needed for complex wavelength-dependent functions at fiber optic telecom wavelengths (1.3 and 1.55 micron) at which Silicon is transparant. What is more, one can in such cases take advantage of the high refractive index contrast between Silicon and its oxide Silica and use Silicon-on-Insulator (SOI) as a substrate for waveguide circuits. The high refractive contrast allows to make ultra-compact passive photonic circuits by exploiting photonic wire or photonic crystal waveguides [1].

Leaves the fact that, in spite of a lot of research, Silicon has never been – and may never become – a suitable material for particular photonic functions such as efficient and compact light emission, modulation or switching at high modulation rates. Therefore there is a need to develop technologies to heterogeneously integrate functions based upon other materials such as III-V semiconductors on Silicon which may contain electronic circuitry or passive photonic circuitry. This integration should, as much as possible, be done by wafer-scale technologies.

In this paper we describe research on two developments along the lines described above. The first is the development of passive nano-photonic circuits in SOI by means of standard CMOS-processes, in particular by means of deep UV optical lithography. The second is the development of active photonic devices based upon thin membranes of III-V materials bonded to Silicon.

2. Passive (nano)photonic circuits in SOI

Current photonic integrated circuits (PIC), such as those made in glass, are fairly large. This is because the on-chip optical waveguides typically have a low index contrast, and therefore the light is weakly confined in the large waveguide core (core diameter $>>$ µm). As a result, waveguides need a large bend radius, consuming valuable chip area only for interconnects. This is one of the reasons current PICs integrate only a small number of components onto a single chip, which is often many cm^2 in size.

Nanophotonic waveguides confine light into a submicron core area by using a very high refractive index contrast. So-called *photonic wires* are scaled-down versions of the conventional waveguides, with a much smaller core area and a higher refractive index contrast. Just as their large counterparts, they guide light by total internal reflection. Alternatively, one can use photonic crystals [2]. These are periodic structures with a high index contrast. An example, consisting of air holes etched into a Silicon layer, is illustrated in the left part of figure 2. Because of their wavelength-scale periodicity, photonic crystals can have a photonic band gap, i.e. a wavelength region where no light can penetrate the crystal. A defect in such a photonic crystal, made by changing or removing a row of holes, can sustain a guided mode in the photonic crystal. Light in the photonic band gap is bound to the waveguide defect because it is not allowed to propagate through the areas of photonic crystal on both sides of the waveguide. In the structure in the left part of figure 2, called a photonic crystal slab waveguide, light is guided in-plane by the photonic crystal, and in the vertical direction by total internal reflection.

(a) bare wafer (b) resist coating and soft bake (c) Top AR coating

(d) exposure (e) post-exposure bake (f) development

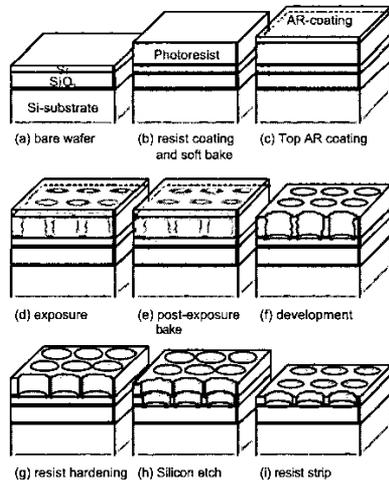(g) resist hardening (h) Silicon etch (i) resist strip

Fig. 1. The fabrication process based on CMOS Technology.

Silicon-on-Insulator (SOI) is an ideal material for nanophotonic waveguides operating in the spectral band for which Silicon is transparant. The top Silicon layer, in our case 220nm thick, has a refractive index of 3.45. The layer below is Silica (SiO_2) with an index of 1.45. If sufficiently thick, this buffer layer optically isolates the top layer from the Silicon substrate. This makes it

possible to make nanophotonic waveguides in SOI by etching only the top layer.

While most research work on nanophotonic waveguides – both in SOI and in other material systems – has been based on e-beam lithography, we have explored and demonstrated that with 248nm deep UV lithography we can define the small features needed for nanophotonic waveguides [1], [3].

The fabrication process is illustrated in figure 1. First, the wafer is coated with photosensitive resist and an anti-reflective coating, after which it is illuminated by the deep UV stepper with designs on a mask. After development, the resist is exposed to an optional plasma treatment, after which it is used as a mask for the Silicon etch. The process is described in more detail in [1].
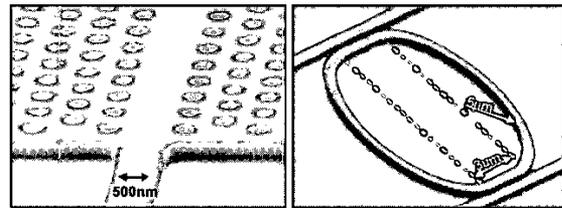

Fig. 2. A W1 photonic crystal waveguide and a photonic wire based racetrack resonator in Silicon-on-insulator.

We fabricated components based on both photonic wires and photonic crystal waveguides with deep UV lithography, as illustrated in fig. 2. These components were characterised using an end-fire technique. Light from a tunable laser source is coupled in a broad ridge waveguide in SOI using a lensed fibre. The broad ridge waveguide is then tapered down to a nanophotonic waveguide, either a photonic wire or a photonic crystal. The transmitted light is led out again through a taper and a broad ridge waveguide and collected by an objective onto a power detector. This way, we can measure the transmission of the component as a function of wavelength.
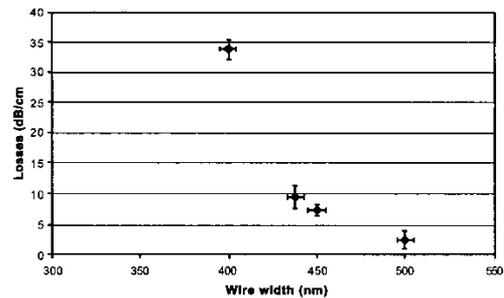

Fig.3. Propagation losses for photonic wires as a function of waveguide width.

In order to measure the propagation losses, photonic wires and photonic crystal waveguides of various length were put on the mask. For photonic wires, we measured propagation losses as low as 2.4dB/cm, for wires that are still single-mode [4]. These loss values are comparable with the best loss values obtained on similar waveguides

defined by e-beam lithography [5]. When the wires get narrower, *the effect of sidewall roughness increases the* losses, as illustrated in figure 3. With propagation losses this low, nanophotonic interconnects of several cm become realistic, allowing to integrate a large number of components onto a nanophotonic IC.

We also made ring and racetrack resonators based on photonic wires. A racetrack resonator, as illustrated in the right part of figure 2, couples light from the input waveguide to the drop waveguide only for the resonating wavelengths, i.e when the wavelength in the material fits an integer number of times in the circumference of the ring. In the other cases, light just continues its way along the input waveguide [7].
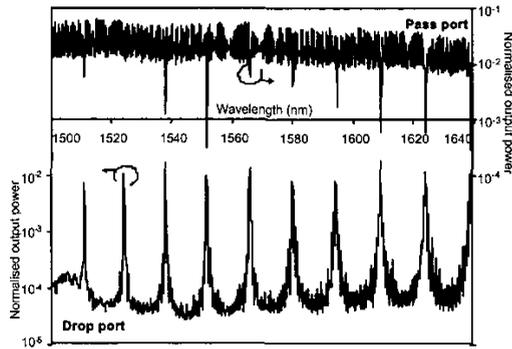

Fig. 4. Transmission spectrum of the racetrack resonator of figure 2. Top: pass port, Bottom: drop port.

Ring resonators can be used as wavelength selective filters. For a resonator of a certain size, the selectivity is mainly determined by the coupling efficiency between the waveguide and the ring and the losses in the ring. This is expressed in the quality factor. For wavelength-selective applications, Q's of several thousands are required. Figure 4 shows the transmission spectrum of the drop and pass port of the racetrack resonator illustrated in the right part of figure 2. The drop port has a strong wavelength selectivity, with a Q of over 3000. With a similar ring resonator, which has a shorter coupling section, we have already attained a Q of 8000 [4].

For single-mode photonic crystal waveguides, in particular W1 waveguides (waveguides consisting of a line defect in the photonic crystal where a single row of holes is removed), we measured significant transmission through a $1mm$ long waveguide. Fig. 5 shows the transmission losses of a W1 photonic crystal waveguide with a lattice pitch $a = 500nm$ and a hole diameter of $320nm$. These results are obtained by measuring the transmission through waveguides of various length, after filtering out the oscillations due to the multiple cavities formed by the facets and the interfaces between the photonic wires and the photonic crystal waveguides. Around $1525nm$, the odd mode is guided and has a propagation loss as low as $7.5dB/mm$. These results are among the best reported for photonic crystal waveguides made by optical lithography, but are still considerably worse than the best results from e-beam lithography,

where values down to 1.5 dB/mm have recently been obtained for similar SOI photonic crystal waveguides [5]-[6].
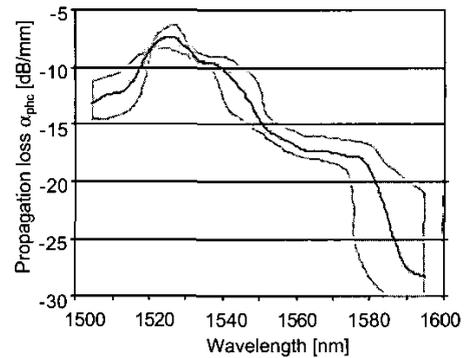

Fig. 5. Propagation losses of a W1 photonic crystal waveguide. The lattice has a pitch of $500nm$ and the holes a diameter of $320nm$.

3.   Active III-V photonic devices on Silicon

A variety of approaches is being studied that combine active photonic functions and Silicon-based functions – either electronic or photonic - into a single chip.

A first approach is so-called monolithic integration where all functionality is combined on one chip, using a single substrate. For example one may fabricate the optoelectronic devices directly into Silicon. Light detection with CMOS is feasible, but only for a limited spectral range (~400nm to ~1000nm). Light generation from Silicon is much more difficult, due to the indirect bandgap of Silicon. Recently, very impressive improvements were reported, among others by using advanced Silicon nanocrystals. The main disadvantage remains the slow modulation speed and the relatively limited efficiency of light generation. A different approach towards monolithic integration is through the epitaxial growth of III-V semiconductor layers directly on the Silicon wafer. Unfortunately, in general there is a large lattice mismatch between Silicon and the III-V semiconductors, leading to a serious degradation of the characteristics of the optoelectronic component. Currently attempts are being made to grow GaAs on Ge-substrates, which could incorporate both electronic and photonic devices [9]. However, this work is still in the "basic research" phase and application will take many years from now. Furthermore, all monolithic approaches have the drawback of a limited fill factor and often the sub-components (electronic/photonic) have to be fabricated in non-optimised substrates.

Various hybrid integration technologies have also been developed. The standard approach for this type of integration is flip-chip mounting. This technique is used for industrial applications, such as focal plane arrays, or two-dimensional parallel optical interconnect modules, or in (non-optical) flip-chip ball grid array packages.

However, flip-chipping is not a wafer-scale technology: it requires back-end processing, and a complex

processing scheme (deposition of wettable/non-wettable metal interfaces, deposition of the solder, positioning of the opto-component, underfilling, ...).

Therefore, various groups are working on heterogeneous integration approaches, where the optoelectronic component – or only its layer structure - is bonded on the Silicon host substrate. After substrate removal the opto-electronic component consists only of a thin membrane bonded to and interfacing to the Silicon wafer. Depending on the application there can be a need for electrical and/or thermal and/or optical interfacing to the underlying Silicon. The structuring of the opto-electronic components can be done prior to bonding or after substrate removal (or a combination of both).

A large variety of wafer bonding methods exists, each with their own benefits and disadvantages. Wafer bonding procedures can roughly be divided into two categories: direct and indirect bonding. Direct bonding means joining two very smooth and clean semiconductor interfaces without using intermediate layers. To ensure the formation of a strong bond the two wafer surfaces normally have to be annealed at a high temperature. Work is being done on low temperature direct bonding procedures though. The main disadvantages of the direct bonding process are the use of high temperature, the need for very flat surfaces, delicate and demanding process technology and the need for specialized equipment.

Indirect bonding covers a wide range of processes where an intermediate layer of some sort (polymers, spin-on-glasses, metals, ...) is used to bond the two wafers.

While most papers in literature report on full wafer bonding (either directly or indirectly) there is also a strong rationale to use die to wafer bonding processes. The rationale is twofold. As the size of the available III-V wafers (50-150mm) is smaller than that of industrial CMOS wafers (200-300mm) the full wafer bonding of III-V wafers onto Silicon wafers is not industrially viable. Even if the size of the wafers is the same the population density of opto-electronic devices will typically be much lower than that of VLSI CMOS, which implies that full wafer bonding would result in high cost systems due to the inefficient use of III-V material.

Our work focuses on the indirect bonding of III-V dies using the polymer benzocyclobutene (BCB) as a bonding agent. The advantages of BCB bonding include excellent thermo-mechanical stability over time, no detectable outgassing at room temperature, low processing temperatures - lower than fusion bonding - and a fairly simple processing scheme that only requires basic cleanroom equipment. BCB is also a low-k dielectric which is chemically inert and resistant to chemical etching. It allows to bond different materials, structured wafers, full wafer bonding and die to wafer bonding. While die to wafer bonding using direct bonding technology can be problematic for small dies due to edge effects, in our opinion this is not the case using an adhesive like BCB.

A problem with the use of BCB is its very low thermal conductivity. This can be an advantage for thermo -optic tuning or modulation but more often it is a problem if the heat generated in the active opto-electronic devices needs to be sunk to the Silicon chip. This calls for proper thermal design. As an example one can use the metal vias needed to connect the opto-electronic component to metal tracks on the underlying Silicon also as thermal vias [10].

In literature there are only very scarce reports of the use of BCB bonding for active opto-electronic components on Silicon [11]. In the remainder of this paper some of our experiments to develop BCB-bonded active opto-electronic components will be described. The details of the bonding technology as such will be reported elsewhere [10].

Three kinds of devices have been fabricated using BCB wafer bonding: microring resonators, LEDs and lasers. We will discuss each of them in somewhat more detail.

A. Microring resonators
Microring resonators consist of a circular waveguide and two straight waveguides which serve as input and output. The basic functionality is that of a wavelength filter. Microring resonators can be fabricated in two ways: laterally coupled and vertically coupled. In the horizontally coupled approach the straight waveguides are in the same plane as the ring waveguide, in the vertically coupled approach they are underneath the ring. In the latter approach wafer bonding is required. This allows to access both sides of the epitaxial layer and perform double-sided processing [8], [12], [13]. The fabrication process is illustrated in Fig. 6.
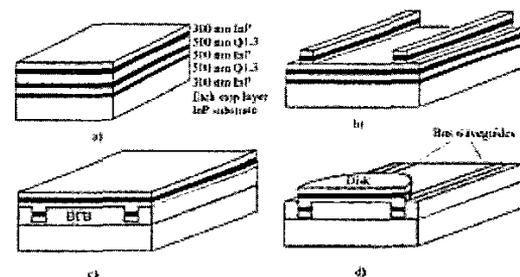

Fig. 6 Fabrication sequence of a vertically coupled InP microring resonator

We start off (Fig. 6a) with an epitaxial layer-structure containing two waveguide core layers and an etchstop layer. Next the straight bus waveguides are defined (Fig 6b). This whole structure is flipped upside down and bonded onto a transfer substrate (Silicon or GaAs so as to allow for easy cleavage of the research samples) with the polymer benzocyclobutene (BCB). The original InP substrate is removed by a combination of mechanical polishing and chemical selective wet etching to the etch stop layer (Fig. 6c). This etch stop layer is also removed. The disk or ring resonator is then etched, the component is cleaved and AR-coated (Fig. 6d).

Fig. 7 shows a typical measurement of the drop and pass port of a microring resonator. This particular microring resonator was a disk with a radius of 30 μm. The achieved Q-value was around 10000.
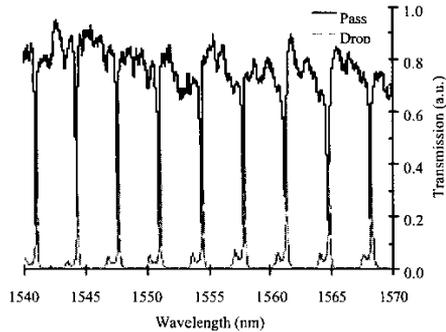

Fig. 7 Pass and drop-port transmission of the InP bonded microring resonator

deposited on one of the samples proved to be no problem either. Next the original InP substrate and the etch stop layer are removed (Fig 8b). In Fig. 8c we can see how the active device is etched in the InP membrane. Then a polyimide layer is deposited through which contact openings are defined and contacts are deposited (Fig. 8d).The contacts in Fig. 8 are ring contacts to allow the LED to emit to the top.
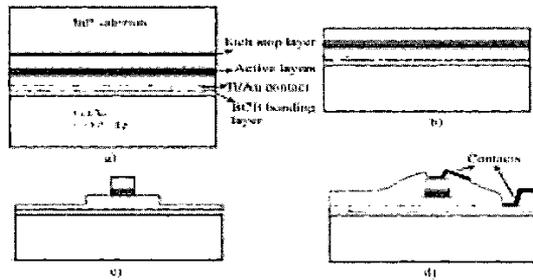
Fig.8 Fabrication sequence of the bonded LED

Continuous wave operation was achieved for the bonded LEDs. This is illustrated in Fig. 9 which plots the measured optical power versus device current. LEDs with different sizes were measured showing the strong temperature dependence of the LEDs. Small area devices showed higher temperature sensitivity than large area devices due to the lower current density of the latter.

C. Lasers
Two sets of lasers were fabricated. The processing sequence of the first batch of lasers was similar to the one of the LEDs. The second batch of lasers had electrical contacts through the BCB-layer to metal pads on the underlying substrate. This is interesting from an integration point of view because the III-V component could be connected to underlying Si-circuitry. The added contacts could also serve as a thermal heat sink allowing

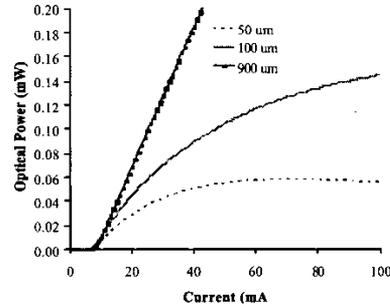the   laser   to   function   in   CW-operation.

Fig. 9 Power-current relation for bonded LEDs of different diameter

The processing sequence starts by metallising both the InP-sample and the transfer substrate. Then they are bonded with BCB. Next the InP substrate is removed. Then stripes are etched by a combination of dry etching and selective wet etching. Polyimide is spun on the sample, openings are defined on top of the ridges and n-contacts are deposited and plated. The metal patterns are then used as a mask in the next etching step that removes the polyimide and the remaining III-V semiconductor on both sides of the metal pattern. An opening is also defined next to the structure. This structure is then buried in a second polyimide layer and an opening is defined above the ridge, above the opening in the BCB and in the region where the p-contact is to be defined. Finally a metal bridging structure is defined that contacts the ridge metal with the Ti/Au layer on the transfer substrate and also the p-contact is defined. These contacts are then deposited and further plated. The fabricated structure can be seen on Fig. 10 which shows an SEM picture with indication of the different regions and contacts.
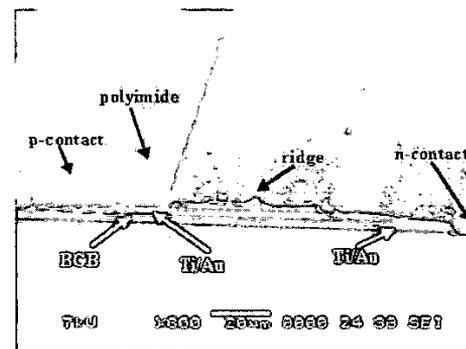

Fig. 10 SEM picture of bonded laser diode

Edge emitting lasers (length = 1mm, width = 7.5 μm) were demonstrated in pulsed regime with threshold current densities around 2.65 kA/cm² which is about double the threshold current density of standard lasers that were processed on the same wafer.
To assess the quality and reliability of the BCB-wafer bonding we have performed damp-heat tests on the

lasers. The devices were subjected to tests at 85 C and 85 % relative humidity (RH). The PI-curves and electrical characteristics of the devices were measured before the tests and after 48, 100, 250 and 500 hours of degradation. The characteristics stay nearly constant and form a clear indication of the BCB-bonding quality.

4.   Conclusion and outlook

This paper has discussed two distinct fields of research in which Silicon technology plays a prominent role for photonic systems-on-a-chip. In the case of passive nanophotonic circuits in SOI it was shown that standard CMOS technologies are suitable for the fabrication of ultra-compact waveguide circuits with low loss. In the case of active opto-electronic components on Silicon it was shown that bonded membrane III-V components allow to make a variety of opto-electronic components with reasonable performance and reliability. This opens the way to a third application: the integration of active opto-electronic components with passive SOI waveguides. For this to happen methods need to be developed allowing for efficient light coupling between bonded III-V components and passive SOI-waveguides. This is a challenging research task for the future.

5.   Acknowledgement

6.   References

[1] W. Bogaerts, D. Taillaert, B. Luyssaert, P. Dumon, J. Van Campenhout, P. Bienstman, D. Van Thourhout, R. Baets, V. Wiaux, S. Beckx, Basic structures for photonic integrated circuits in Silicon-on-insulator, Opt. Expr. 12 (8) (2004) 1583–1591.

[2] J. D. Joannopolous, R. Meade, J. Winn, Photonic Crystals - Molding the Flow of Light, Princeton University Press, Princeton, N.J., 1995.

[3] W. Bogaerts, V. Wiaux, D. Taillaert, S. Beckx, B. Luyssaert, P. Bienstman, R. Baets, Fabrication of photonic crystals in Silicon-on-insulator using 248-nm deep UV lithography, IEEE J. Sel. Topics. Quant. Electron. 8 (4) (2002) 928–934.

[4] P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. Van Campenhout, D. Taillaert, B. Luyssaert, P. Bienstman, D. Van Thourhout, R. Baets, Low-loss SOI photonic wires and ring resonators fabricated with deep UV lithography, IEEE Photon. Technol. Lett. 16 (5) (2004) 1328–1330.

[5] S. J. McNab, N. Moll, and Y. A. Vlasov, "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides," Opt. Express, vol. 11, no. 22, pp. 2927–2939, Nov. 2003.

[6] M. Notomi, A. Shinya, S. Mitsugi, E. Kuramochi, and H. Ryu, "Waveguides, resonators and their coupled elements in photonic crystal slabs," Opt. Expr., vol. 12, no. 8, pp. 1551–1561, April 2004.

[7] B. Little, J. Foresi, G. Steinmeyer, E. Thoen, S. Chu, H. Haus, E. Ippen, L. Kimerling, and W. Greene, "Ultra-compact Si-SiO2 microring resonator optical channel dropping filters," IEEE Phot. Technol. Lett., vol. 10, no. 4, pp. 8212–8222, 1998.

[8] P.P. Absil, J.V, Hryniewicz, B.E. Little, F.G. Johnson, K.J. Ritter, P.-T. Ho : 'Vertically coupled microring resonators using polymer wafer bonding', IEEE Photonics Technology Letters, vol 13, no 1, January 2001, p 49

[9] Y. Chriqui, L. Largeau, G. Patriarche, G. Saint-Girons, S. Bouchoule, I. Sagnes, D. Bensahel, Y. Campidelli, O. Kermarrec: 'Direct growth of GaAs-based structures on exactly (001)- oriented Ge/Si virtual substrates: reduction of the structural defect density and observation of electroluminescence at room temperature under CW electrical injection', Journal of Crystal Growth, vol 265, 2004, p 53-59

[10] Ilse Christiaens, Günther Roelkens, Kurt De Mesel, Dries Van Thourhout and Roel Baets, "Adhesive wafer bonding with benzocyclobutene", to be published

[11] Katsnelson, V. Tokranov, M. Yakimov, M. Lamberti, and S. Oktyabrsky, "Hybrid integration of III-V opto-electronic devices on Si platform using BCB," in MRS conference proceedings, ser. Nano- and micro-electro-mechanical systems and molecular machines, vol. 1, MRS, 2003.

[12] Ilse Christiaens, D. Van Thourhout, R. Baets, "Low power thermo-optic tuning of vertically coupled microring resonators", IEE Electronics Letters, 40(9), p.560-561 (2004).

[13] Ilse Christiaens, D. Van Thourhout, R. Baets, "Vertically coupled InP/InGaAsP microring resonators fabricated with polymer wafer bonding", to be published