Nanophotonic Waveguides in Silicon-on-Insulator Fabricated With CMOS Technology

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***Abstract*—High-index-contrast, wavelength-scale structures are key to ultracompact integration of photonic integrated circuits. The fabrication of these nanophotonic structures in silicon-on-insulator using complementary metal–oxide–seminconductor processing techniques, including deep ultraviolet lithography, was studied. It is concluded that this technology is capable of commercially manufacturing nanophotonic integrated circuits. The possibilities of photonic wires and photonic-crystal waveguides for photonic integration are compared. It is shown that, with similar fabrication techniques, photonic wires perform at least an order of magnitude better than photonic-crystal waveguides with respect to propagation losses. Measurements indicate propagation losses as low as 0.24 dB/mm for photonic wires but 7.5 dB/mm for photonic-crystal waveguides.**

***Index Terms*—Nanophotonics, photonic crystal, waveguides, silicon-on-insulator (SOI).**

I. Introduction

INTEGRATION of a multitude of photonic functions onto a single chip can bring the same advantages to photonics as what integration has done for microelectronics: a serious reduction of costs through high-yield wafer-scale processes, increased performance, compact components with complex functionality, etc. In photonic integrated circuits (PICs) on-chip integration has the added benefit of automatically meeting the critical alignment tolerances of subcomponents through the lithographic processes. This reduces the need for active alignment methods, which are notorious for dominating the cost of discrete optoelectronic components. Today's photonic components, however, are typically too large to allow much integration. Many components have a length scale of several hundred micrometers to several millimeters and, in some cases, even several centimeters, and this is not only true for active functions, but also for simple passive components such as filters, (de)multiplexers, and even simple interconnecting waveguides with bends, couplers, and splitters.

In many cases, these large dimensions are needed because one uses waveguides with a low refractive index contrast. By increasing this index contrast, the confinement can be improved, but this also means that the waveguide core should be reduced in size to keep the waveguide single mode. Then, however, the geometrical features not only become very small but have to be very accurately fabricated, with an accuracy in the range of 1 to 10 nm. Therefore, we can call these waveguides *nanophotonic waveguides*. To confine light in a nanophotonic waveguide, one can use total internal reflection, as in conventional waveguides, creating so-called *photonic wires*. However, it is also possible to use a high-contrast periodic structure, a *photonic crystal*, to confine light by the *photonic bandgap* (PBG) effect [1], [2].

A consequence of the higher lateral index contrast is that the waveguides become more sensitive to scattering at roughness on the core–cladding interface [3]. Therefore, high-quality, high-resolution fabrication tools are required for these nanophotonic waveguides. For research purposes, nanophotonic components are traditionally fabricated using e-beam lithography. While this is a very accurate technique, it is a serial writing process, making it slow and unsuitable for mass fabrication. Alternatively, conventional optical lithography, with illumination wavelengths down to 300 nm, is used for the fabrication of current photonic integrated circuits (ICs) but lacks the resolution to define dense nanophotonic structures like photonic crystals and photonic wires. Deep ultraviolet (UV) lithography, the technology used for advanced complementary metal–oxide–seminconductor (CMOS) fabrication, offers both the required resolution and the throughput needed for commercial applications. However, technology development for 248, 193, and recently 157 nm is driven by the CMOS industry, and processes are therefore not always suited for nanophotonic structures.

In this paper, nanophotonic waveguides will be demonstrated in silicon-on-insulator (SOI) fabricated with deep UV lithography. For this purpose, standard CMOS fabrication processes were adopted to improve their capability for fabricating photonic nanostructures, like photonic crystals and photonic wires. This fabrication process is described in detail in Sections II–V. A number of nontrivial obstacles that had to be overcome in order to migrate the process from CMOS to nanophotonics are also

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discussed. Then, a number of fabricated waveguide components and measurements of the propagation losses are discussed in Section VI and VII. Finally, Section VIII will offer some examples of other nanophotonic structures fabricated with this technique.

II. SOI Nanophotonic Waveguides

In nanophotonic integrated circuits, waveguides are an extremely crucial component. Not only are they necessary for interconnects, but many functional elements are also based on waveguides. Therefore, good waveguides are a prerequisite for further integration.

A. General Properties

For waveguides that guide light through total internal reflection, the confinement is largely determined by the contrast in the refractive index between the waveguide core and the surrounding cladding. A high refractive index contrast in the lateral direction (2:1 or higher) makes it possible to confine the light tightly to the waveguide core. In semiconductor material systems, this can be achieved by etching the waveguides deeper into the semiconductor substrate. However, as the index contrast increases, the waveguide will support more guided modes, which is an unwanted effect in most PICs. To obtain a single-mode waveguide with a high refractive index contrast, the waveguide's cross section must be reduced, to the order of $(\lambda/n_{\mathrm{core}})^2$, with λ the wavelength of the light in vacuum, and n_{core} the refractive index of the waveguide core. For very high contrasts, like semiconductor $(n = 3.45)$ to air $(n = 1.0)$ or semiconductor to silica $(n = 1.45)$, waveguides have widths smaller than 500 nm, with features that can be as small as 100 nm when operating at telecom wavelengths between 1.3 and 1.6 μm. The use of the high refractive index contrast implies that the geometrical features not only become very small (100–500 nm) but also have to be very accurately fabricated, sometimes down to 1 nm.

There are two techniques to confine light in nanophotonic waveguides, which are commonly known as *photonic wires* and *photonic crystals*. A photonic wire is basically a conventional waveguide with a high index contrast and a small cross section, typically with a width of 300–500 nm. The light is guided by total internal reflection. The tight confinement allows for compact elements, like sharp bends, corner mirrors [4], and ring resonators [5]. However, the performance is limited by the scattering at sidewall roughness, so these waveguides require very good processing. Alternatively, light can be guided in a photonic-crystal slab. Photonic crystals are periodic structures with a high refractive index contrast and a period of the order of the wavelength of the light in the material [1], [6]. Because of this strong contrast and the periodicity, photonic crystals have peculiar optical properties, including a PBG [2]. A line defect in a photonic crystal then effectively creates a waveguide, as the light cannot leak away into the crystal.

B. Material Choice: SOI

We can use a variety of materials for photonic-crystal slabs, as long as the refractive index contrast is sufficiently high. Semiconductors, with refractive indexes typically larger than 3, are ideally suited. For the majority of this work, we chose SOI. The main reasons for this choice are its very good optical properties at optical fiber communications wavelengths and its compatibility with CMOS fabrication processes, which is discussed in Section III.

SOI consists of a thin silicon layer on top of an oxide cladding layer carried on a bare silicon wafer. With its silicon core $n = 3.45$ and its oxide cladding $(n = 1.45)$, it has a high vertical refractive index contrast. In addition, both the silicon and the oxide are transparent at telecom wavelengths of 1.3 and 1.55 μm.

To reduce leakage of the guided mode in the top layer to the silicon substrate, we chose an oxide thickness of 1 μm [7]. The thickness of the core was chosen to be 220 nm in order to keep the slab waveguide single mode for the transverse-electric (TE) polarization.

C. Photonic Crystals

Photonic crystals are periodic structures with periods of the order of the wavelength of the light and a very high refractive index contrast within each period [2], [6]. For telecommunications, where infrared light with wavelengths in the range 1.3–1.6 μm are used, the photonic-crystal period a is typically 0.5 μm or less. The periodicity can extend in one, two, or three dimensions. Because of this high refractive index contrast, light will be scattered very strongly throughout the structure, and the scattered waves from each period can either add up or cancel out, depending on the wavelength of the light. For a well-chosen geometry and a unit cell with sufficiently high refractive index contrast, the scattering from each cell can interfere in such a way that all light inside the crystal within a certain wavelength range is canceled out, so no propagation is possible in the structure [1], creating a PBG.

As already mentioned, a defect can introduce localized states in the PBG, binding the light in a specific location in the crystal. In a line defect, light has no other option than to follow the defect, which defines a perfect waveguide. The light cannot leak away through the surrounding photonic crystal because of the PBG. Therefore, if reflection is controlled, bends in such photonic-crystal waveguides can, in principle, be very abrupt.

Although three-dimensional (3-D) photonic crystals can control light in all directions, they are very difficult to fabricate for optical and infrared wavelengths. An alternative to full 3-D photonic crystals is the combination of a conventional waveguide structure and a photonic crystal. Here, a two-dimensional (2-D) photonic crystal is created by etching holes or rods in a semiconductor layer structure. In the horizontal direction, the photonic crystal controls the flow of light, while in the vertical direction the light is confined in the layer with the higher refractive index. These photonic crystal slabs also provide 3-D control of light while they are much easier to fabricate, using lithography and etching techniques. The bottom row of Fig. 1 shows examples of a single-line-defect waveguide (a so-called W1 waveguide) in a photonic-crystal slab made in SOI. Unlike 3-D photonic crystals, the confinement in the vertical direction is not necessarily perfect, which can result in out-of-plane scattering and can cause leakage of light [8], [9].

When the concept of photonic-crystal waveguides was introduced, the design of a waveguide seemed as simple as removing

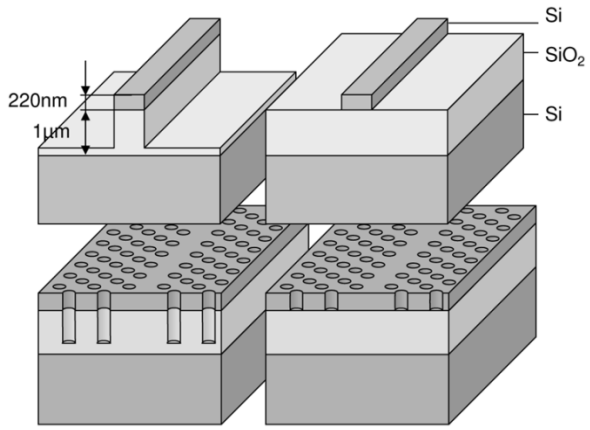

Fig. 1. Nanophotonic waveguides in SOI. Top: Photonic wires. Bottom: W1 photonic-crystal waveguide. Left: Deep ething. Right: Silicon-only etch.

a row of holes, creating a so-called W1 waveguide. While this design has indeed a guided-waveguide mode, its properties are ill-suited for pure waveguiding. A simple W1 waveguide in SOI is not a very good waveguide. It is not single mode, and the guided modes have a narrow bandwidth below the light line. However, by removing the oxide cladding in SOI, and thus creating a membrane, the light line of the cladding is shifted to higher frequencies. In this way, a W1 waveguide with sufficient bandwidth is possible, and waveguides with very low propagation losses (less than 1 dB/mm) have been demonstrated both in silicon membranes [10], [11] and in GaAs membranes [12].

Without oxide removal, Notomi *et al.* have already demonstrated low propagation losses by reducing the optical volume of the core. In such a W0.7 waveguide, the width of the waveguide has been decreased by shifting the lattice regions on both sides [11], [13], making the waveguide single mode. However, the shifted lattice makes it more difficult to implement bends or splitters. Alternative ways to reduce the optical volume of the waveguide core without shifting the lattice, like introducing defect holes or a defect trench, or increasing the size of the border holes, invariably introduce additional sidewall surface, increasing the possibility of scattering at sidewall roughness [3].

Apart from pure waveguiding, photonic-crystal slabs can also be used for other purposes. One significant aspect of periodic structures is the appearance of wavelength regions with a very flat dispersion curve, and therefore a low group velocity, especially near the band edges [14]. In these regions, light is coupled strongly between the backward- and forward-propagating direction and travels slowly through the waveguide. If the waveguide has active properties, like gain or nonlinear effects, the interaction time of the light with the material is significantly enhanced when using slow waves.

D. Photonic Wires

The principle of photonic wires is the same as of conventional optical waveguides: light is confined in a narrow core of high index material surrounded by a cladding of lower index material. For photonic wires, the index contrast between core and cladding is very high. This gives rise to very strong confinement, which makes it possible to make very sharp bends without radiation losses in the bend. However, there is no PBG to stop light from radiating away once it escapes the confinement of the wire.

Photonic wires are not periodic, and therefore their dispersion relation is far less exotic than photonic crystals. This makes them more predictable and easy to design. Moreover, they are broad-band with a fairly linear dispersion, making them very well suited for waveguiding.

E. Deep or Shallow Etching

When we want to fabricate nanophotonic components in SOI, we can choose between two etch procedures, each with its merits and drawbacks. Fig. 1 illustrates both procedures for a photonic-crystal slab and a photonic wire. When we etch both the top silicon and the underlying oxide, we increase the refractive index contrast even more, because we replace the oxide $(n = 1.45)$ with air $(n = 1)$. In addition, the bottom of the photonic-crystal holes are far removed from the guided mode, eliminating a possible source of scattering. An additional advantage is that the vertical layer structure becomes more symmetric, reducing the interaction between TE and transverse-magnetic (TM) modes. However, as we will illustrate in Section III, this approach introduces significantly more sidewall roughness, which is a principal source of propagation losses.

When listing all these advantages of deep etching, is there any reason to etch only the silicon, as illustrated in the right part of Fig. 1? When we etch only the silicon, the sidewall roughness due to etching can be significantly reduced. In addition, in order to eliminate the interaction between TE and TM, oxide can be deposited on top of the silicon core after etching. This deposition, briefly discussed in Section III, works better with shallow holes than with deep holes.

A third option is to remove the oxide substrate altogether. This lowers the refractive index of the lower cladding significantly, and increases the design flexibility for photonic-crystal waveguides. However, this *membrane* approach has a major drawback. Because the waveguide structure has to be free-standing, this can only be used on a limited area. Photonic crystals, with their interconnected network, are much better suited for this approach than photonic wires.

F. Conclusion

The reduced size and the high index contrast make the design of nanophotonic waveguides a nontrivial issue. While photonic crystals offer a wide selection of strong dispersive properties, it is not straightforward to design a simple waveguide. On the other hand, the dispersive properties, together with the strong confinement, make the structures very promising for wavelength-selective functionality.

For simple waveguides, photonic wires are better suited. Their behavior is very predictable, and it is easy to make compact elementary waveguide components, like bends and splitters. However, wires are sensitive to sidewall roughness, more so than photonic crystals. Therefore, very good fabrication quality is needed.

III. Fabrication With Advanced CMOS Processes

In this section, we will describe the fabrication of nanophotonic waveguides with deep UV lithography and dry etching. These techniques are based on advanced CMOS processes, like the ones used in the high-end semiconductor industry.

A. Differences Between CMOS and Nanophotonic Structures

While deep UV lithography is capable of printing features with the dimensions of photonic wires and photonic crystals, there are some significant differences between nanophotonic components and typical CMOS components: CMOS components are layered structures. Each layer contains only critical structures of a certain type (transistor gates, contact holes, etc.), so the process can be optimized for each layer individually. In planar nanophotonics, all structures are fabricated on the same level, and small alignment tolerances require that all structures are fabricated in the same lithography step. Photonic crystals and photonic wires are very different structures, and the optimal process conditions differ between them. Therefore, process optimization for nanophotonic components will have to make different compromises than for CMOS structures. As we will see further, it is not straightforward to fabricate both photonic wires and photonic crystals on target at the same time.

In addition, the types of structures can differ significantly. For example, the optimal photonic-crystal lattice for TE polarization is a triangular lattice of air holes where the holes have a large fill factor, i.e., the hole diameter is a significant fraction of the pitch [2]. We call these *superdense* lattices, i.e., where the hole diameter is larger than the spacing in between. This type of structure is not used in electronics, where the best equivalent in CMOS is a 1:1 *dense* (i.e., hole diameter equal to the spacing in between) array of contact holes used to connect the different metal interconnect layers. However, these contact holes are typically arranged in a square lattice, and the hole diameter never exceeds half of the pitch.

In addition, the requirements for sidewall roughness are very different in nanophotonics and in CMOS. In the former, all sidewalls should be kept smooth to reduce scattering, while in CMOS structures, the effect of line-edge roughness is felt only in narrow lines in the electrical resistance of the line. This has only recently become an issue for CMOS fabrication.

B. SOI Wafers

Apart from being a good material for photonic waveguides, SOI is also compatible with CMOS processes and commercially available in 200 mm wafers. High-quality SOI wafers are typically fabricated using wafer bonding. For our experiments, we used commercial wafers from SOITEC fabricated with the UNIBOND process [15]. First, a wafer is oxidized to create the buried oxide layer. Then, hydrogen ions are implanted at a well-controlled depth, creating a Smart Cut. This wafer is bonded to a clean silicon wafer. The substrate of the first wafer can now be separated along the Smart Cut interface and then annealed and polished.

First experiments with standard UNIBOND wafers (a buried oxide of 400 nm and a top silicon layer of 205 nm) showed that the oxide was too thin, causing optical leakage to the substrate

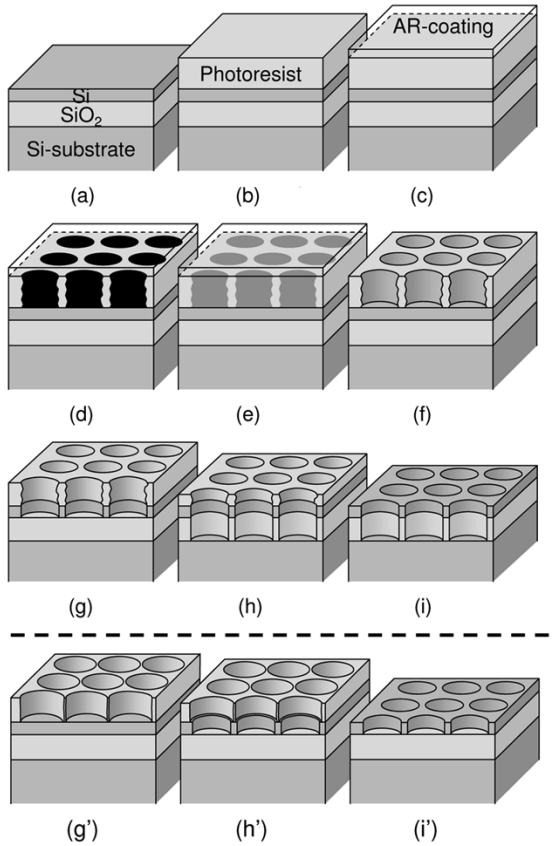

Fig. 2. Process flow for the fabrication of nanophotonic structures in SOI. The third and fourth row illustrate two options for the etching of the structures, either through both silicon and oxide, or only the silicon layer. (a) Bare wafer, (b) resist coating and soft bake, (c) top AR coating, (d) exposure, (e) postexposure bake, (f) development, (g) silicon etch, (h) oxide etch, (i) resist strip, (g') resist hardening, (h') silicon etch, and (i') resist strip.

[7]. Therefore, we switched to custom-made wafers with a silicon thickness of 220 nm and an oxide layer of 1 μm. This buffer thickness provides adequate isolation from the substrate for the TE polarization.

C. Overview of the Fabrication Process

The fabrication process with deep UV lithography is similar to that of conventional optical projection lithography. The basic process flow is illustrated in Fig. 2. First, the photoresist is coated on top of a 200-mm SOI wafer and then prebaked. On top of the resist, an antireflective (AR) coating is spun to eliminate reflections at the interface between the air and the photoresist. These reflections could give rise to standing waves in the photoresist, and therefore inhomogeneous illumination. Then, the wafer is sent to the stepper, which illuminates the photoresist with the pattern on the mask. As a 200-mm wafer can contain many structures, the die with the pattern is repeated across the wafer. This can be done with varying exposure conditions, which makes it possible to do detailed process characterization. After lithography, the resist goes through a postexposure bake and is then developed. For our experiments, we used Shipley UV3 resist.

Depending on whether we want the bottom oxide-etched or not, we can use different processes. If we want to etch the underlying oxide, the developed photoresist can be used directly

as an etch mask (third row of Fig. 2). The top silicon layer and the oxide are then etched subsequently in different etch chambers but without exposing the structures to the atmosphere in between the etch processes.

However, to reduce the sidewall roughness, our optimized fabrication process does not include the oxide etch (bottom row of Fig. 2). Instead, an additional plasma treatment of the developed photoresist is needed, called *resist hardening*, before the etching (see Section V). Then, the photoresist is used directly as a mask for the silicon etch. In addition, a number of postprocessing steps are possible, including thermal oxidation or oxide deposition.

IV. Deep UV Lithography

For research purposes, e-beam lithography is the workhorse for the fabrication of photonic nanostructures. Unfortunately, this technique is not suitable for commercial application. Therefore, we explored the possibilities of using deep UV lithography. For our experiments, we had access to the CMOS fabrication equipment of IMEC (the Inter University Microelectronics Center), Leuven, Belgium. Because lithography at a wavelength of 248 nm is now the mainstream fabrication tool for high-end CMOS, we chose this wavelength for the majority of our fabrication runs. We used an ASML PAS5500/750 stepper connected to an automated track for preprocessing (coating and baking) and postprocessing (baking and developing).

A. Resolution

In optical projection lithography, like deep UV lithography, the resolution is largely determined by the illumination wavelength λ and the numerical aperture (NA) of the projection system [16]. The most critical structures are the dense periodic ones, where the smallest period $a_{\min}$ that can be imaged is given by

$$a_{\min} = \frac{\lambda}{\mathrm{NA}} \tag{1}$$

when the first diffraction order of the periodic structure is still passed through the projection system. The loss of the higher diffraction orders will result in a fuzzy image. The final quality of the resist patterns is therefore determined by the threshold of the photoresist and the exposure dose. For example, when printing holes, the hole diameter will increase when a larger exposure energy is used in the stepper. In practice, this means that with 248-nm lithography and an NA $= 0.63$, we can make structures with a period down to 400 nm.

B. Lithography of Nanophotonic Structures

Early experiments with CMOS masks, discussed in [7], show how we can use this exposure dose to print holes larger than originally designed. Using this overexposure, we could print superdense lattices with a mask containing just 1:1 dense patterns. After these successful tests, masks were designed with nanophotonic test structures and components. Fig. 3 shows the feature size of typical nanophotonic waveguide structures as a function of exposure dose. As we can see, the hole diameters of the triangular lattices increases with the exposure dose, while the linewidth of a photonic wire decreases. The range of exposure energies where the structure is still within specification is called the *exposure latitude*.

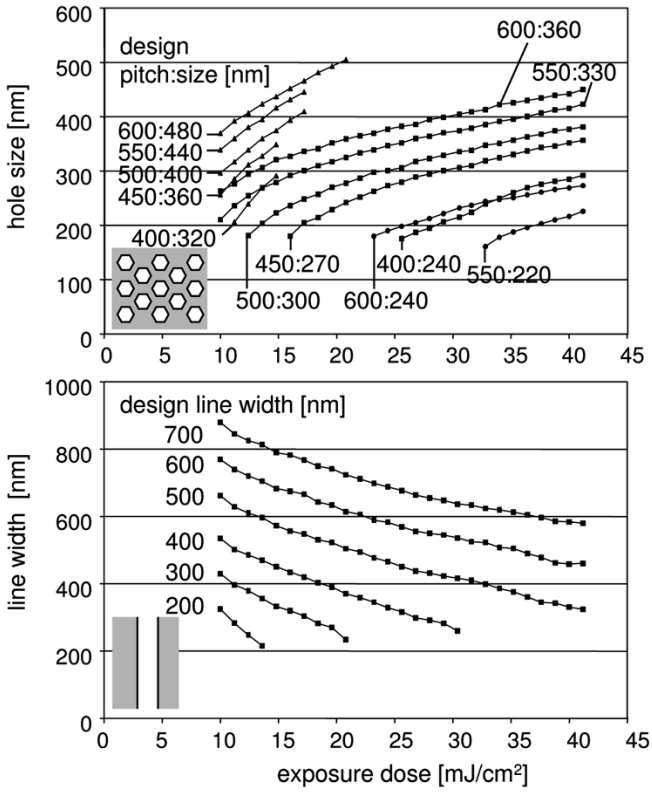

Fig. 3. Size of nanophotonic structures as a function of exposure dose. Top: Triangular lattices of holes with different design pitches and diameters (on the mask). Designed diameter: Pitch ratio is 0.4 (circles), 0.6 (squares), and 0.8 (triangles). Bottom: Isolated lines with different design linewidth.

On the other hand, with a given feature size on the mask, we can print a wide range of feature sizes on the wafer. As the exposure conditions can be changed by the stepper from die to die, we can fabricate a wealth of different features on a single wafer.

C. Combining Lines and Holes

One of the difficulties of fabricating nanophotonic components is the requirement to print both photonic wires (isolated lines) and photonic crystals (superdense lattices of holes) together in the same lithography step. As we can deduce from the graphs in Fig. 3, the dose-to-target for lines and holes is quite different. Therefore, when targeting to fabricate a lattice of holes correctly, there will always be a bias on the isolated lines, which will be overexposed and therefore too narrow.

In order to print the lines correctly, a bias needs to be applied in the design to either the holes or the lines to print both together on target [7]. Because it is easier to change the design size of an isolated structure, the bias is best applied to the lines. For example, at the dose of 25 mJ, where 300-nm holes with 500-nm pitch print correctly, a 50-nm bias needs to be applied to a 500-nm line to print it correctly. This correction should be known in advance, because it needs to be applied directly on

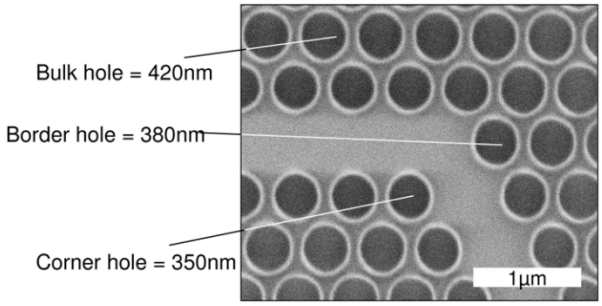

Fig. 4. Example of optical proximity effects. The holes near the photonic-crystal defect are printed smaller than the holes in the bulk of the lattice. The lattice pitch is 530 nm.

the mask. With detailed process characterization, we could establish the correct bias and apply it successfully to subsequent mask design.

D. Optical Proximity Effects

Photonic crystals are superdense periodic structures with feature sizes close to the illumination wavelength. This causes the images of neighboring holes to overlap during lithography. Because of this, holes in a photonic crystal may interfere constructively and print larger or interfere destructively and print smaller than semi-isolated holes. In uniform lattices, this effect is not noticeable, as the illumination energy will be chosen to print the holes in the lattice on target. However, at the boundaries of the lattice, or near defects like a waveguide or cavity, some holes lack neighbors and will therefore print differently than their counterparts in the bulk of the lattice. This phenomenon is called *optical proximity effect* (OPE). An example is given in Fig. 4: the holes near the line defect are 40 nm smaller than the holes in the bulk, and in the corner this effect is even worse, with the corner hole being 70 nm smaller.

The functionality of photonic-crystal waveguides and related components is largely determined by the holes near the (line) defects. Fig. 5 illustrates the effect of OPE on the guided mode of a simple W1 photonic-crystal waveguide. It shows a detail of the band diagrams of a W1 photonic-crystal slab waveguide in SOI, with a hexagonal lattice with a 500-nm period and a bulk hole size of 300 nm. In the left part of Fig. 5, there are no proximity effects at the border holes. The middle and the right part of the figure show the band diagram of the same structure, but with the border hole size $\oslash_{\mathrm{border}}$ increased by 10 and 20 nm, respectively. Even for such a small change, the characteristics of the guided mode change considerably. This can be easily noticed by the position of the mini-stop band (MSB) between the vertically odd and even mode. For a change of 10 nm in the border hole, the MSB center wavelength shifts by almost 20 nm.

Note that proximity effects are not only a problem of optical lithography. With e-beam lithography, scattering electrons will also cause proximity effects in closely packed structures. However, because e-beam lithography is a serial writing process, the proximity effects just add up, and are therefore easier to model [17]. With optical lithography and deep UV lithography, the effect is coherent and more difficult to predict.

As with the line-hole bias, to correct for OPE, the features on the mask should be altered. This is illustrated in Fig. 6. Holes

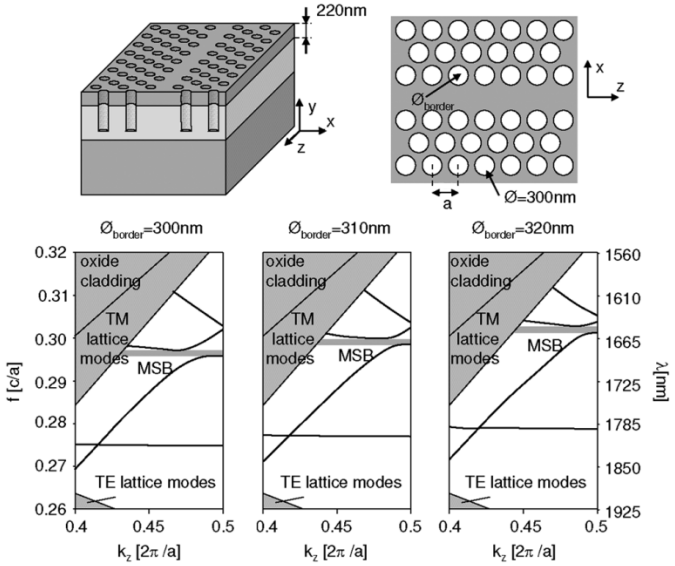

Fig. 5. Impact of OPE on the band diagram of a W1 waveguide: The increase in the diameter of the border hole $\oslash_{\mathrm{border}}$ causes a significant shift of the guided modes, which can be observed in the position of the MSB.

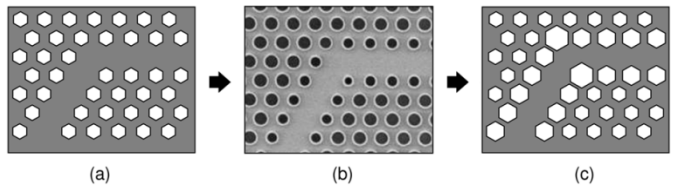

Fig. 6. Principle of OPCs for photonic-crystal structures. When uncorrected, (a) the design on the mask will print the defect holes differently than the bulk holes (b) due to optical proximity effects. (c) To correct this, the design on the mask should be altered in advance. The effect in the scanning electron microscope (SEM) is exaggerated.

near a lattice defect are printed smaller and are therefore enlarged on the mask. It is evident that a good understanding of the OPE is necessary to design the structures with optical proximity correction (OPC).

To characterize optical proximity effects and the needed corrections in photonic crystals, we have designed a mask with structures consisting of various photonic-crystal waveguides along with a large number of bends, cavities, and other possible components. We then repeated this structure on a mask with many variations of bulk hole sizes, and corrections on corners and borders. This makes it possible for us to measure the OPEs and the required corrections directly. Fig. 7 shows the OPEs for the holes in a 60° bend in a W1 waveguide. Such graphs are an interpolation from the OPE measured on our test structures and allow us to apply the necessary OPC on future mask designs. In practice, this is done numerically instead of visually on the graph. For new structures, similar data can be measured on our test structures as the need arises.

V. Etching

Following lithography, the structures defined in photoresist should be transferred to the underlying SOI substrate. As we have seen, keeping the refractive index of the bottom cladding as low as possible by etching the holes deep into the buried oxide

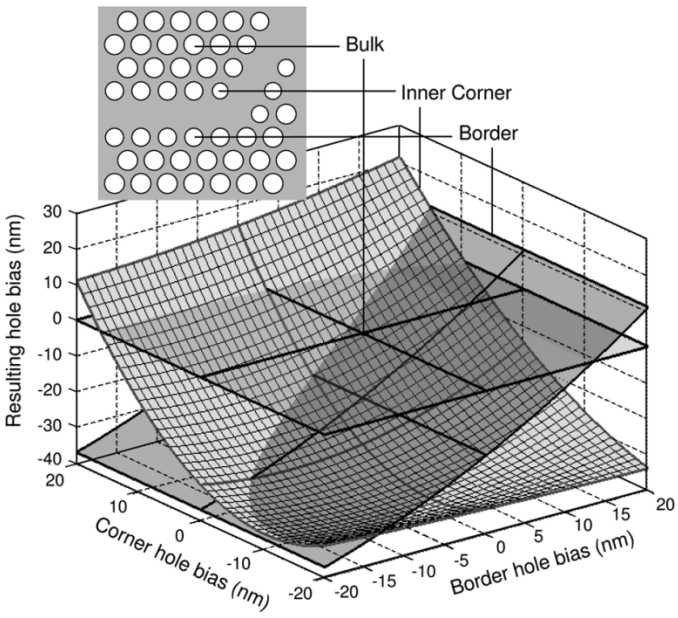

Fig. 7. OPEs for a hexagonal lattice of holes with a pitch of 500 nm. Design size of the bulk holes is 300 nm, overexposed to 320 nm. The graph shows the hole size for the border and inner corner holes when a bias (OPC) is applied on the mask.

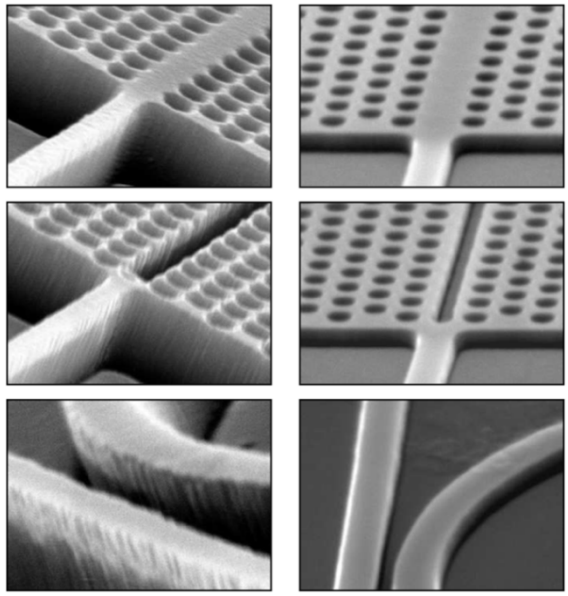

Fig. 8. Structures fabricated with deep UV lithography. Left: With deep etching. Right: With silicon-only etch. Top: W1 photonic-crystal waveguide. Middle: W1 photonic-crystal waveguide with a center trench. Bottom: Detail of the coupling section between a photonic wire and a ring resonator.

yields better optical properties. Another rationale for deeply etched holes is that the light in the top silicon layer will hardly feel the bottom of the holes and will not be scattered. However, as we will show, this deep etching causes substantial sidewall roughness. After trying several techniques for roughness reduction, we found that the best results could be achieved by not etching the oxide altogether.

The etching for the top silicon layer and the underlying oxide is performed in two separate steps: first the top silicon layer is etched, and then the underlying oxide. The equipment used for etching is a LAM_A6 platform with four process modules. For the silicon etch, a TCP9400 module is used with a Cl_2/O_2/He/HBr chemistry. The etch recipe consists of a breakthrough etch and a main etch, with different chemistry. After the silicon etch, the wafer is transferred to an *Exelan* module without exposure to the atmosphere. The oxide etch is done with a CF_4/O_2 chemistry. The etch depth can be controlled with the etch time.

First, etching experiments with SOI wafers with a top silicon layer of 205 nm and an oxide of 400 nm are described in [7]. Because of the limited oxide thickness, we can completely etch through the oxide cladding, while the sidewalls stay relatively smooth, even with the deep etch [7].

A. Deep Etching

We then developed a deep-etch process for the wafers with a thicker oxide buffer. Because the resist is used directly as an etch mask, only a limited etch depth is possible before the remaining resist breaks down. In addition, such deep-etch processes for small features in a multilayer substrate are seldom required in CMOS devices. This made the process development a difficult task. The left column of Fig. 8 shows structures fabricated with a deep-etch process. The main significant side effect of the deep etching is the appearance of sidewall roughness. For deeply etched structures, as the photonic wires illustrated in the bottom left of Fig. 8, the sidewall becomes very irregular. Because sidewall roughness causes scattering of light as it propagates through the waveguide, this has to be avoided.

B. Roughness Reduction

To reduce the sidewall roughness, one can partially oxidize the top silicon layer to smooth the roughness. It has already been shown that thermal oxidation of SOI waveguides can smooth the sidewalls of both photonic-crystal waveguides [18] and photonic wires [19]. As the rate of oxidation is well documented and can be controlled quite accurately with the temperature, this is a reliable way of reducing roughness.

In Fig. 9 we see an example of a photonic-crystal hole with different amounts of oxidation. The first impression is that the oxidation increases the amount of roughness on the sidewalls, blowing up the existing irregularities. However, because the new roughness is on an oxide–air interface instead of on a silicon–air interface, the impact is less dramatic. Although this is hard to establish experimentally, we can assume that the underlying silicon–oxide interface is smoother, due to the diffuse nature of the oxidation process. We can also see that the volume of the top layer increases after oxidation, creating a rounded core layer in cross section.

While oxidation can improve the roughness in the top silicon layer, it has little or no effect on the underlying oxide layer. Therefore, light will still be scattered by the roughness in the cladding. A solution to that problem would be to remove the cladding layer, creating a freestanding membrane. While this is a valid option for small areas of photonic-crystal structures, it is more difficult to achieve for photonic wires, as the line waveguides are unsupported by the substrate.

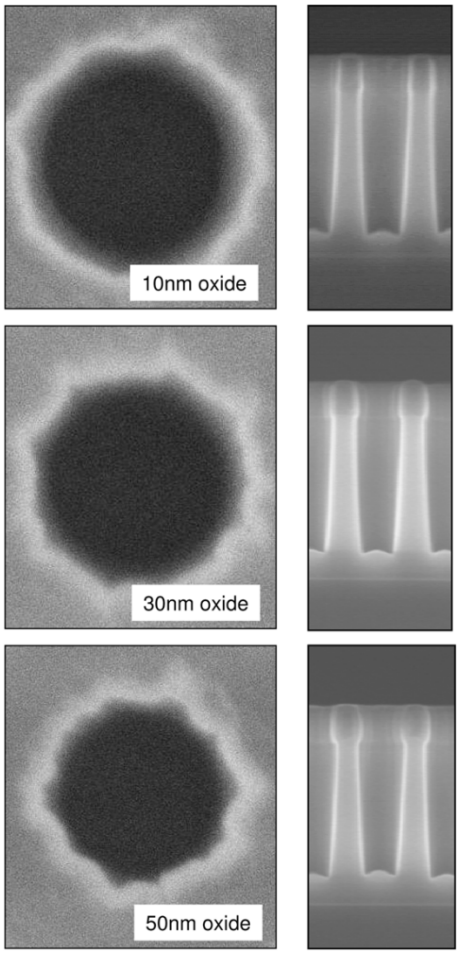

Fig. 9. Photonic-crystal holes with roughness reduction through oxidation. Top to bottom: with 10, 30, and 50 nm of oxidized silicon. Note that the visible roughness is now on the interface between the oxide and the air.

C. Silicon-Only Etch

The most obvious approach is to abandon deep etching altogether and only etch the top silicon layer. By leaving out the second etch step, the sidewall roughness was drastically reduced. This can be seen in the right-hand side of Fig. 8. The residual sidewall roughness of the photonic wire is of the order of 5 nm or less.

D. Resist Hardening

The silicon-only etch process, however, gives rise to a considerable bias between lithography and etch, i.e., the etched holes were typically 50–70 nm smaller in diameter than the holes after lithography. This can be compensated by lithographic overexposure for isolated structures, but with the densely packed photonic-crystal holes, this bias is too large. Experiments with a resist-hardening plasma treatment showed that we could successfully reduce the bias to less than 30 nm. This is sufficiently small to be compensated by overexposure during lithography.

E. Oxide Deposition

While etching only the silicon can reduce the roughness, we end up with an asymmetric layer structure. However, we can make the layer structure symmetric again by adding a top cladding with the same refractive index as the underlying oxide. After a silicon-only etch, which causes little sidewall roughness of its own, we do a short thermal oxidation. Then, we deposit oxide, which makes the structure symmetric in the vertical direction. This is beneficial as it reduces the coupling between TE and TM modes.

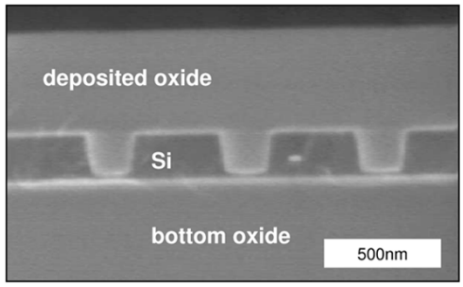

Fig. 10. Cross section of photonic-crystal holes with 500-nm pitch after 5-nm oxidation and oxide deposition. Note that there are no voids in the deposited oxide and that the top surface is completely planarized.

We used a *chemical vapor deposition* technique with a chemistry based on $SiO_4(C_2H_5)_5$ (TEOS). With an optimized process, even deep and narrow holes can be filled without creating voids. An example is shown in Fig. 10. We can see that the oxide deposition creates a smooth, planar top cladding and no artefacts, like voids, in the photonic-crystal holes. A side effect of this technique is that the SOI structure is sealed from the outside world. While this can be advantageous for commercial components, for research purposes it makes close inspection of the structures with a scanning electron microscope (SEM) impossible.

VI. Characterizing Propagation Loss

To characterize the propagation losses of nanophotonic waveguides, we measure the transmission of light through the component as a function of wavelength. The most used technique for this purpose is the cutback method with end-fire incoupling.

As a light source, we use a computer-controlled tunable laser with a wavelength range of 1500–1640 nm. Light is launched into optical waveguides through a cleaved facet using a lensed fiber, and the transmitted light is collected at the opposite side of the sample by an objective.

To facilitate the coupling through a cleaved facet, we used a standard 3-μm-wide (and therefore multimode) ridge waveguide. This waveguide is tapered down using a linear adiabatic taper down to 500 nm, filtering out the spurious higher order modes. For outcoupling, the reverse structure is used, and the relevant nanophotonic waveguide is located in between.

The propagation losses can be calculated by measuring the loss of the light for various lengths of the waveguide. When this loss (in decibels) is plotted as a function of waveguide length (in millimeters), the measured points should be on a straight line, of which the slope is the propagation loss of the waveguide in deciebels per millimeter.

The loss of a single waveguide can be determined directly (by measuring the transmitted power), but this approach is sensitive to fluctuations in incoupling and outcoupling. Moreover,

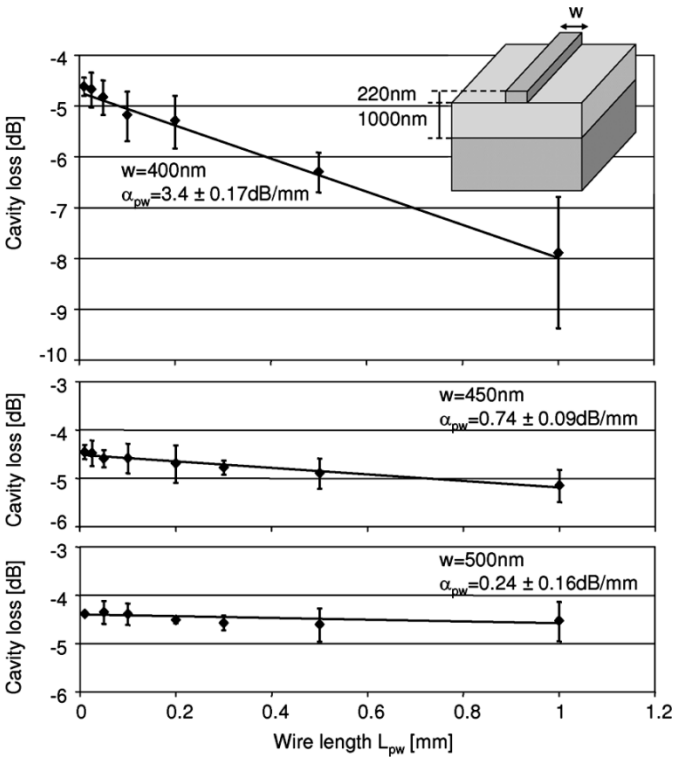

Fig. 11. Extraction of wire losses from the transmission of a Fabry–Pérot cavity formed by the incoupling and outcoupling facet. The cavity loss was measured for different wire lengths. From the slope of the fitted line, the propagation loss of the wire can be extracted. We did this for different wire widths $w_{\rm core}$. Top to bottom: $w_{\rm core} = 400$ nm, $w_{\rm core} = 450$ nm, and $w_{\rm core} = 500$ nm.

the transmission can be wavelength dependent due to cavity effects in the sample or the measurement setup.

Instead, one can use these cavity effects to extract the losses. With the end-fire method, a Fabry–Pérot cavity is formed by the two reflecting cleaved facets of the sample. The transmission of this cavity will be a periodically peaked function (so-called *fringes*). From the ratio between the maximum and the minimum of this oscillating function, the losses inside the cavity can be extracted [20]. The cavity is larger when the nanophotonic waveguide section is longer. This method is independent of the incoupling efficiency but is only suitable when the losses inside the cavity are not very high.

VII. Measurement Results

A. Photonic Wires

Because of their small core and high confinement, photonic wires are an ideal structure to test the fabrication quality. For the deeply etched photonic wires, we measured propagation losses of 34 dB/mm for 500-nm-wide wires and 6 dB/mm for 600-nm-wide wires. At that width, however, the wires become multimode and unsuitable for nanophotonic ICs.

When we etch only the silicon, matters improve dramatically. Fig. 11 shows the cavity loss as a function of wire length of the Fabry-Perot cavity between the incoupling and outcoupling facet, and this for three different wire widths. The slope of the fitted line gives us the propagation loss of the photonic wires.

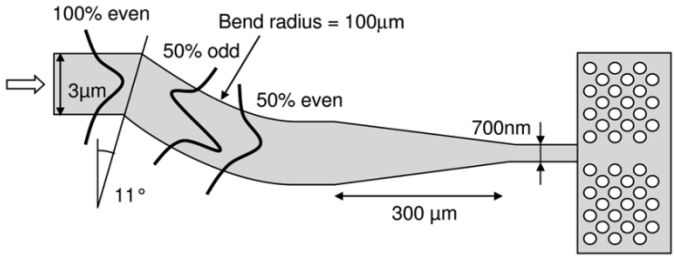

Fig. 12. Mode mixer to excite asymmetric photonic-crystal modes. At the 11° tilt, the ground mode is converted into a 50%/50% combination of the ground mode and the asymmetric first-order mode.

For 500-nm-wide wires, we now measure 0.24 dB/mm, an improvement of 25 times with respect to the deeply etched structures. When the wire gets narrower, losses increase exponentially, with 0.74 dB/mm for 450-nm wires and 3.4 dB/mm for 400-nm wires. We expect to reduce the losses even more when we apply a thermal oxidation step to smooth the sidewalls.

B. Photonic-Crystal Waveguides

Photonic-crystal waveguides are more difficult to characterize. There is the additional reflection at the interface with the wire, and they are more dispersive and sometimes multimode. In addition, many waveguide designs also have a first-order guided mode in the PBG. To excite these antisymmetric modes with our symmetric incoupling spot from the lensed fiber, we have designed a mode converter. Fig. 12 shows how an 11° abrupt bend in the broad ridge waveguide mixes the even ground mode into a $= 50\%/50\%$ combination of the ground mode and the first-order mode. Of course, the incoupling wire should also be somewhat broader to support both modes.

We have implemented a large number of photonic-crystal waveguide designs, with different defect size and geometry. These were implemented with straight incoupling waveguides to excite the ground mode, and with the 50% mode mixer.

Measurement on the deeply etched structures yielded propagation losses as low as 21 dB/mm for a simple W1 waveguide. The dominant loss mechanism is sidewall roughness, as the etch quality of the deeply etched structures is rather poor. Waveguides with different defect geometries invariably had a larger sidewall surface area, which resulted in even higher propagation losses.

For the structures with a silicon-only etch, the sidewall roughness is strongly reduced, with a positive effect on the propagation losses. Fig. 13 shows the propagation losses of a W1 photonic-crystal waveguide with a lattice pitch $a = 500$ nm and holes of 320 nm. Around 1525 nm, the odd mode is guided and has a propagation loss of 7.5 dB/mm, which is much lower than the propagation losses of the deeply etched structures.

Fig. 14 shows another photonic-crystal waveguide, this time a W1 with little defect holes with a diameter $\oslash_{\rm def} = 200$ nm. Again, we used the mode mixer for incoupling. For this structure, we have simulated the exact band structure, and we can match the regions of low propagation losses exactly to the guided modes in the band diagram. However, the lowest losses in this structure are still of the order of 40 dB/mm. This larger propagation loss is consistent with scattering at the sidewall

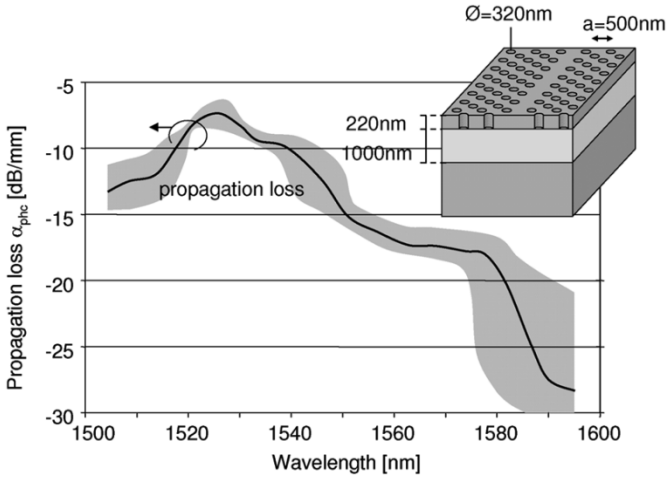

Fig. 13. Propagation losses of a W1 photonic-crystal waveguide with silicon-only etch. The lattice has a pitch of 500 nm, and the holes a diameter of 320 nm. Around 1525 nm, the asymmetric first-order mode has a propagation loss of approximately 7.5 dB/mm.

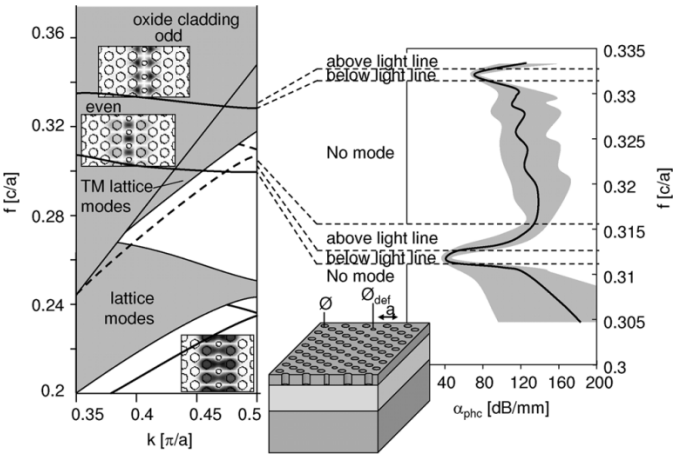

Fig. 14. Propagation losses of a W1 waveguide with small defect holes matched to the calculated band diagram. We can see that the regions of low propagation loss match exactly the guided modes below the light line. The lattice constant $a = 500$ nm, the hole diameter $\varnothing$ in the bulk of the lattice is 320 nm, and the defect hole diameter $\varnothing_{\rm def} = 200$ nm.

roughness, as the total amount of sidewall surface is larger due to the additional defect holes.

VIII. Other Fabricated Nanophotonic Structures

Apart from straight waveguides, we have made a large variety of components. As an example, we briefly discuss ring resonators in photonic wires [21] and surface gratings for coupling to fibers [22], [23].

A. Ring Resonators

Ring resonators can provide building blocks for a large number of functional components on a photonic IC, including various types of filters [5]. A fabricated example of a ring resonator and a racetrack resonator (i.e., a ring resonator with a longer coupling section) is shown in Fig. 15. We fabricated ring and racetrack resonators, symmetrically coupled to straight input and output waveguides.

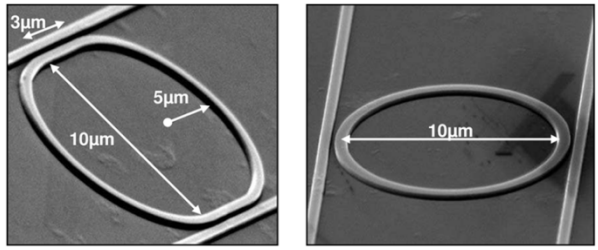

Fig. 15. Racetrack and ring resonator with silicon-only etch.

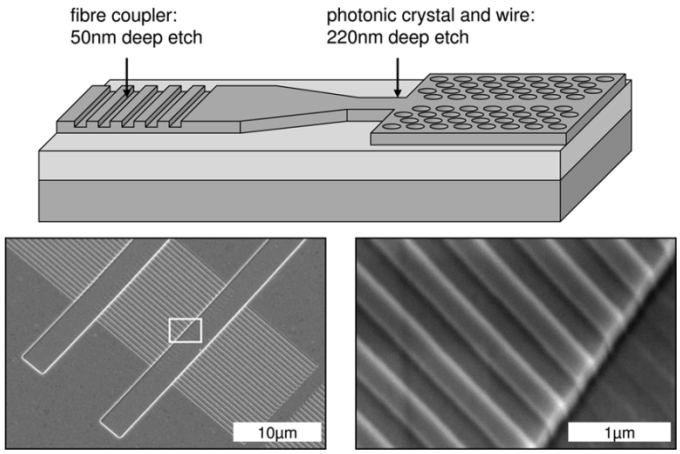

Fig. 16. Fiber coupler gratings in SOI fabricated with a two-step process. The fiber couplers need another etch depth than the nanophotonic waveguides.

The racetrack resonator in Fig. 15 with a radius $r_{\rm ring} = 5\ \mu$m and a coupling section of $L_{\rm coup} = 3\ \mu$m has a quality factor $Q > 3000$ and an add–drop crosstalk of around -20 dB [21]. The coupling section in a ring resonator is much shorter than in a racetrack resonator, so the coupling efficiency of the wire to the ring will be much lower. This translates into a higher Q (because the ring loses less light to the wire) but a lower overall coupling efficiency to the drop port. We have measured ring resonators with a Q of 8000 but a drop efficiency of only 1%. This is discussed in detail in [21].

The most critical feature of these structure is the narrow gap in the coupling section, which has a very strong impact on the coupling efficiency. This gap has to be fabricated with very high precision. However, because of the proximity of the ring and the straight waveguide, there will be optical proximity effects which have to be corrected.

B. Waveguide Gratings for Fiber Coupling

Apart from waveguide components, we have also fabricated gratings on top of waveguides with the purpose of coupling light from a fiber into a nanophotonic waveguide and back out [22]. Unlike photonic crystals and photonic wires, the fiber couplers are not etched completely through the top silicon layer. Depending on the type of grating and the duty cycle, the optimal etch depth is between 40 nm and 80 nm. To use the fiber couplers with deeply etched waveguides, the gratings should be fabricated in a separate step, as shown in Fig. 16.

Because deeply etched structures can cause a problem for the lithography (as the wafer will have too much topography and

the resist layer will not have a homogeneous thickness), the shallowly etched fiber couplers should be fabricated first. In order to align both types of structures, we can rely on the alignment tools available in the deep UV stepper. Instead of providing alignment features on the individual dies, the stepper takes care of aligning the dies to alignment markers on the wafer. Knowing the absolute position of the different structures on the reticle, it carries out the necessary alignment with submicrometer accuracy. This is much faster than die-based alignment, as alignment needs to be done only once per wafer. We have demonstrated such fiber couplers with a coupling efficiency of over 20% [22], [23].

IX. Conclusion

It has been shown that advanced CMOS technology, and more specificly, deep UV lithography, is capable of fabricating nanophotonic structures. However, the need to fabricate all structures in a single lithographic step can introduce a considerable mismatch between the different types of components, as the dose-to-target for holes, lines, and other structures can vary. Therefore, detailed process characterization is required to determine the correct bias for each individual structure. In addition, the dense nature of photonic crystals gives rise to optical proximity effects that are difficult to model. Test structures have been fabricated to experimentally measure optical proximity effects and the necessary corrections to apply on the mask.

For the fabrication, photoresist was used as the etch mask. Because the deep etching, through both the silicon and the oxide layer, caused a large amount of sidewall roughness, roughness reduction techniques were needed. In the end, the most promising proved to be not to etch the oxide, but only the top silicon layer.

This process has made nanophotonic waveguides of very high quality. For the photonic wires, this translates directly into low propagation losses, as low as 0.24 dB/mm for single-mode wires of 500-nm width. Photonic-crystal waveguides are still considerably more lossy than photonic wires, but 7.5 dB/mm loss in a W1 photonic-crystal waveguide has also been shown.

Acknowledgment

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