Fabrication of ultra-compact photonic structures in Silicon-on-Insulator (SOI) using 248nm deep UV lithography

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ABSTRACT

We demonstrate the use of deep UV lithography for the fabrication of wavelength-scale photonic structures. Mass-fabricating ultra-compact structures like photonic crystals is not a straightforward process. Serial writing techniques like e-beam lithography are too slow, while standard optical lithography lacks the required resolution. Deep UV lithography, as used today in the CMOS industry, promises to deliver the accuracy together with the high volume capacity. In this paper, we will show photonic crystal-based structures fabricated with deep UV lithography. We will discuss the fabrication process, and how the differences of these structures with typical CMOS structures make the application of this technology anything but straightforward.

Keywords: Deep UV Lithography, Photonic Integrated Circuit, Photonic Crystal

1. INTRODUCTION

Photonic Crystals (PhC) are optical structures with wavelength-scale periodic variations of the refractive index. The fabrication of 2-D photonic crystals for optical and near-infra-red wavelengths is therefore a challenging task. From the moment of their conception [1] these structures promised to scale down the size of optical componentssignificantly. However, wavelength-scale photonic structures for telecom wavelengths (1.55μm or smaller) cannot be fabricated as easilyas their larger counterparts. Most of the PhCs for research purposes are fabricated with e-beam lithography. This is a very accurate but extremely slow pattern-definition technique, and therefore not suitable for wide-scale fabrication. Conventional optical lithography offers the possibility to process large production volumes, but lacks the resolution required to print the small details and periodicity of PhCs.

Deep UV lithography is an optical lithography technology using excimer lasers at wavelengths of 248nm and shorter and is being introduced in the top-of-the-line CMOS foundries all over the world. This widespread adoption provides a huge potential manufacturing base when the need for ultra-compact photonic ICs (PIC) should emerge. In this paper we will present experiments for the fabrication of PhC-based structures using 248nm Deep UV lithography, and we will discuss some of the issues that arise due to the differences between these structures and CMOS ICs. In the next section, we will briefly discuss photonic crystal slabs. Section 3 gives an advantages and drawbacks of the current manufacturing techniques for photonic crystal slab components and discusses our approach with deep UV lithography. In section 4 we take a look at the experiments. Section 5 discusses briefly the problems that arise when using deep UV lithography for ultra compact PICs.

2. PHOTONIC CRYSTAL SLABS

Photonic crystals are periodic structures with a high refractive index contrast within the unit cell. With periods of the scale of the wavelength of light, these structures have very strong diffractive properties, including photonic band gaps (PBG). These are wavelength ranges in which the light cannot propagate through the PhC. These PBGs make PhC very attractive as a lossless cladding for waveguides or cavities, as the light is forbidden to penetrate the PhC. An important requirement for the existence of a PBG is a sufficiently high refractive index contrast, generally 2 to 1. This limits the possible material systems to be used for optical waveguides. Semiconductors, with refractive indices of 3 and higher, are ideally suited for this purpose.

3-D photonic crystals control light in all directions, but are hard to make for optical wavelengths. Alternatively, we can use a combination of a 2-D PhC with slab waveguide [2], [3]. In these photonic crystal slabs light is controlled in plane by the PhC and confined by total internal reflection in the vertical direction. As discussed further, these structures can be fabricated with existing high-definition lithography and dry etching techniques.

3. FABRICATION OF ULTRA-COMPACT PHOTONIC CIRCUITS

The techniques of the fabrication of ultra-compact photonic ICs are similar to those used in the CMOS industry: The patterns of the structures are defined in a photoresist layer on the wafer and then transferred into the semiconductor using an etching process. However, when the feature size of the structures grows smaller, the manufacturing process is being tailored more and more to suit the structure. Therefore, the manufacturing techniques for CMOS cannot be ported to any other type of structure in a straightforward way.

3.1 Pattern definition

For the fabrication of ultra-compact photonic ICs we need to write features of submicron size with a precision of tens of nanometers. For experimental purposes, e-beam lithography is best suited for this purpose. With this technique, every structure is written directly into a photoresist by a narrow electron beam. Structures with a size down to 50nm can be defined in this manner. However, each structure is written one after the other, i.e. in a serial way, making the overall process slow. It can take several hours to write not even a very complex PIC.

For mass fabrication, a parallel process is needed that can print all patterns at the same time. Optical lithography has always been the workhorse for this purpose, but it is limited by optical diffraction. Features smaller than the optical wavelength become fuzzy or don't print at all. Therefore the next generation of optical lithography employs excimer lasers with wavelengths in the deep UV, starting at 248nm and 193nm with research being conducted at 157nm. At these wavelengths it is possible to fabricate certain isolated structures with dimensions below 100nm [4].

For periodic structures, like photonic crystals, optical lithography imposes a limit on the periodicity. The period of the smallest periodic structure that will still print is defined by the illumination wavelength divided by the numerical aperture (NA) of the lens system used [5]. With NAs of 0.6 or larger now common in high-end deep UV steppers, the smallest usable period for 248nm lithography is therefore about 400nm.

The facilities we used at IMEC for the experiments described in this paper were consist of an ASML PAS 5500/300 deep UV stepper with an illumination wavelength of 248nm. The stepper uses 8" wafers and is attached to an automated wafer-processing track.

3.2 Silicon-on-Insulator as a material system

There are many available materials for photonic ICs: from polymers or glass to III-V semiconductors and silicon. For these experiments with deep UV lithography we opted for silicon-on-insulator, a material system consisting of a silicon wafer with a layer of silica (SiO_2) and a layer of silicon on top. For our purposes, this material has multiple advantages. First, it is optically transparent at 1.55μm. There is also a strong refractive index contrast between the top silicon layer (n = 3.45) and the buried oxide (n=1.45), making the top silicon a good optical waveguide. Furthermore, the high refractive index of silicon makes it possible to use the material for photonic crystals, which require a high refractive index contrast. The combination of the high vertical contrast and the photonic crystal makes it possible to design lossless photonic crystal waveguides in this material, especially when removing the buried oxide near the photonic crystal [6]. However, the deciding factor in our material choice was the availability of SOI as 8" wafers that were compatible (both in for factor as in chemical composition) with the processing equipment. The SOI wafers we used were standard Unibond wafers purchased from SOITEC, with a buried oxide of 400nm and a top silicon layer of 205nm.

3.3 Photonic crystals versus contact holes

PhCs are dissimilar to any structure used in CMOS. Planar photonic crystals with a PBG for TE consist of triangular lattices of holes with an radius/pitch ratio (*r/a*) of 0.3 or even larger. In contrast, contact holes used in CMOS circuits are designed square, and are never packed as dense as PhCs. Fabrication rules valid for contact holes can therefore not be applied to photonic crystals in a direct way. Nevertheless, the first fabrication tests were performed using a CMOS process evaluation mask with dense contact holes. The mask consisted of square lattices of holes of various size and pitch, with an *r/a* ratio of 0.25 or smaller. To make superdense lattices similar to photonic crystals, we overexposed these structures to print the holes larger with the same pitch.

4. EXPERIMENTAL RESULTS

4.1 Square lattices

The first lithography tests were conducted with promising results. The tests were carried out using this CMOS process evaluation mask. We manufactured lattices with pitches from 400nm to 600nm, and reached *r/a*

ratios of 0.25 to 0.35 using overexposure. For each target we had an adequate budget in both focus and exposure dose.

The etching process of these structures was evaluated on a-SOI wafers. These are wafers with a similar layer structure as the commercial SOI wafers we used, but the top silicon layer is replaced by an layer of amorphous silicon. These wafers can be fabricated in-house from ordinary silicon wafers. Although the a-SOI layer structure is different from crystalline SOI from the viewpoint of optical components, it has comparable etch properties at a substantially lower cost per wafer. Etch tests on these a-SOI wafers show holes with straight sidewalls in both the a-Si layer and the oxide layer, with no discernible discontinuities between the different layers. Sidewalls have little deviation from the vertical and show very little roughness. We also performed the same test on a standard SOI wafer. This showed similar quality of sidewall smoothness.
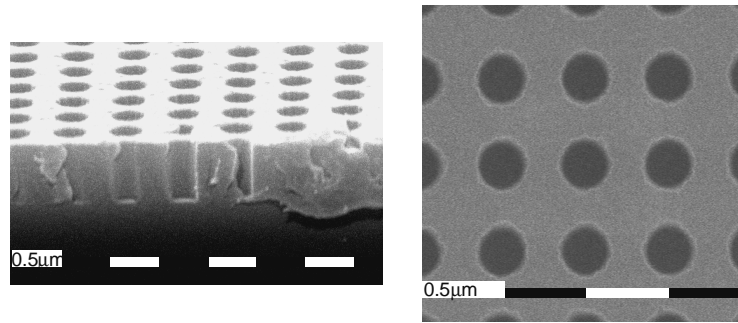

Figure 1. 250nm densely packed holes with a pitch of 500nm (r/a=0.25) in a-SOI. The a-Si top layer is 200nm thick, the buried oxide 400nm.

4.2 Superdense hexagonal lattices

From these first tests we can conclude that it is possible to fabricate superdense lattices of holes. For further tests, a process evaluation mask for photonic crystal-like structures was designed. This mask contains triangular lattices with various pitch and hole size, both for inspection in top-down view as cross-section. It also contains some photonic crystal designs described in literature, where necessary adapted to the SOI layer structure [7], [8].

Lithography tests on these structures show well defined resist patterns for the holes. The holes on the reticle are defined as hexagons in a triangular lattice, but they are rounded by the lithography process. For the various pitches and *r/a* ratios the holes are very uniform throughout the lattice (Figure 3a-b). Only for the extremely dense (*r/a* > 0.4) holes at the smallest pitches (400nm, 450nm) the resist between the holes is broken down (Figure 3c). This is mainly due to the strong effect of sidelobes from the hole's image in the resist.
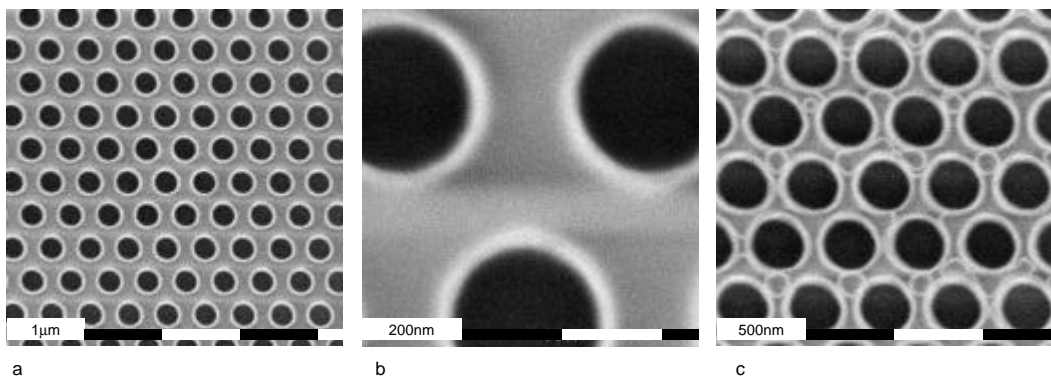

Figure 3: Resist patterns of a triangular lattice of holes. (a,b) Holes of 300nm diameter at a 500nm pitch (r/a=0.3) at various magnification. (c) Holes of 320nm diameter at 400nm pitch (r/a=0.4), showing broken down resist patterns between the holes.

5. FABRICATION ISSUES

Although the first experiments discussed above gave rise to promising prospects for the fabrication of photonic ICs with deep UV lithography, there are some issues that need to be addressed. First, there is the problem that not all structures require the same illumination energy to print on target. Another problem is

proximity effects: the shape and size of a structure is changed with the presence or absence of a neighbouring structure.

5.1 Different structures need different energy

A lot of passive PICs can be fabricated in a single lithography steps: All the structures are on the same layer and require the same etch depth. However, as the structures shrink, it becomes more difficult to print all elements with the same exposure energy. Narrow lines (e.g. waveguides) require far less energy than small holes (e.g. photonic crystals) . Using different lithography steps for each type of structure could solve this issue, but this requires submicron alignment of the different lithography steps. A more flexible way is to apply a bias to the structures on the reticle so they need the same exposure energy to print on target. To model this bias correctly is very difficult, and experiments are planned to establish the correct bias for various optical structures so they can be printed together with photonic crystals.

5.2 Optical proximity corrections

Photonic crystals are dense periodic structures. When printing these structures, neighbouring structures tend to influence each other. This is true for e-beam lithography, where scattered electrons add to the exposure of other holes. The effect is more profound with optical lithography, as the image of each hole exhibits sidelobes that overlap with the neighbouring holes. Because all the holes are illuminated simultaneously, the effects interfere coherently, so holes can influence each other either positively (i.e. adding to the hole's exposure and therefore increasing the hole size) or negatively (decreasing the hole size). This is called optical proximity effects (OPE).

In the bulk of a PhC lattice, one does not notice OPE, because the symmetry makes all holes equal, and the illumination energy is chosen to print these holes on target. However, at the boundaries of the crystal holes lack one or several neighbours, changing the OPE. Therefore these holes might print different from those in the bulk. As the functionality of PhC-based components is often determined by the defects in the lattice, OPE at the crystal boundaries has a profound effect. As an illustration, we exaggerated the OPE in Figure 3. The holes on the reticle are designed identical, but print differently after lithography. Therefore, to print these holes correctly, optical proximity corrections (OPC) have to be applied at the boundaries. These OPCs need to be included in the mask design. Experiments with optical proximity corrections for photonic crystals are now being conducted.
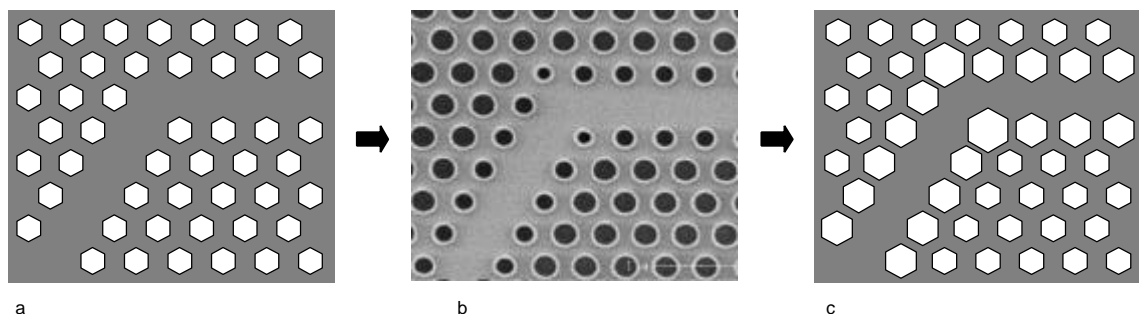
Figure 3. Exaggerated illustration of Optical Proximity Effects (OPE). Although the holes on the reticle are all of the same size (a), the holes in the bulk of the lattice print different than the holes near the waveguide (b), so to correct for this optical proximity corrections (OPC) should be added to the mask (c).

6. CONCLUSIONS

Our first experiments show that ultra-compact PICs, including photonic crystals, can be made with deep UV lithography. First lithography and etching experiments with photonic crystals in SOI showed well-defined holes with very little edge roughness. However, different structures (like holes and lines) may need widely different illumination conditions, and optical proximity effects for PhCs should be corrected at the mask design stage.

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