Micro-Transfer-Printing of III-V Semiconductor and Silicon-Germanium Photodetectors on Silicon Photonic Integrated Circuits

Micro-transfer-printen op silicium fotonische geintegreerde circuits van fotodetectoren op basis van III-V-halfgeleiders en silicium-germanium

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Dankwoord

Dit is het einde. C'est finis.

This is the end of my four years of PhD life.

I think that doing a PhD in photonic engineering is a real mental test as you are always first in something, specifically, in process development. There were many experiments that failed miserably (some are described in this thesis), and in some situations, it seems that your work is doomed. But the beauty of the failed experiment is that it can teach you much more in comparison to a successful experiment and, therefore, it helps you not only to succeed but also to grow into a mature person.

It was not all doom and gloom, however. There were plenty of cool, memorable moments and people to who I am extremely grateful and will certainly remember.

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Gent, August 2019
Grigorij Muliuk

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List of Acronyms

A

AC	Alternating Current
ALD	Atomic Layer Deposition
AMP	Amplifier
APD	Avalanche Photodiodes
A-Si	Amorphous Silicon
AWG	Arbitrary Waveform Generator

B

BDEAS	Bis(diethylamino)silane
BER	Bit-Error Rate
BHF	Buffered Hydrofluoric Acid
BOX	Buried Oxide

C

CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CPU	Central Processing Unit
c-Si	Crystalline silicon
CW	Continuous Wave

D

DBR	Distributed Bragg Reflector

DC	Direct Current
DML	Directly Modulated Laser
DSP	Digital Signal Processing
DVS-BCB	Divinylsiloxane-bis-Benzocyclobutene

E

EDFA	Erbium Doped Fiber Amplifier

F

FDTD	Finite Difference Time Domain
FF	Fill Factor
FIB	Focused Ion Beam
FSR	Free Spectral Range
FTTH	Fiber-To-The-Home

G

GBP	Gain-Bandwidth Product
GC	Grating Coupler
GSG	Ground Signal Ground

H

HCl	Hydrochloric Acid
HF	Hydrofluoric Acid
HD-FEC	Hard Decision-Forward Error Correction

I

IC	Integrated Circuit
ICP	Inductively Coupled Plasma

IPA	Isopropyl Alcohol

K

KOH	Potassium Hydroxide

L

LED	Light-Emitting Diode
LPIN	Lateral P-I-N

M

MF-SiNx	Mixed Frequency Silicon Nitride
MSM	Metal Semiconductor Metal
MUTC-PD	Modified Uni-Travelling-Carrier Photodiode
MZM	Mach Zehnder Modulator

N

NRZ	Non-Return-Zero

O

OOK	On-Off Keying

P

P2P	Point-to-Point
PC	Polarization Controller
PD	Photodiode

PDL	Polarization Dependent Losses
PDK	Process Design Kit
PDMS	Polydimethylsiloxane
PECVD	Plasma Enhanced Chemical Vapour Deposition
PIC	Photonic Integrated Circuit
PR	Photoresist
PRBS	Pseudo-Random Bit Sequence

R

RF	Radio Frequency
RIE	Reactive Ion Etching
RRC	Root-Raised Cosine

S

SD-FEC	Soft Decision-Forward Error Correction
SEM	Scanning Electron Microscopy
SOI	Silicon-on-Insulator

T

TE	Transverse Electric
TIA	Trans-Impedance Amplifier
TL	Tunable Laser
TP	Transfer Printing

U

UTC-PD	Uni-Travelling-Carrier Photodiode

V

VPIN	Vertical P-I-N
VNA	Vector Network Analyzer
VOA	Variable Optical Attenuator

W

WDM	Wavelength Division Multiplexing
WGPD	Waveguide Coupled Photodiode
WPIN	Waveguide Coupled P-I-N
WWW	World Wide Web

Z

ZB	Zettabytes

Nederlandse samenvatting –Summary in Dutch–

In dit werk hebben we transferprinttechnologie ontwikkeld om germanium en III-V halfgeleider fotodetectoren met fotonische geïntegreerde schakelingen te integreren.

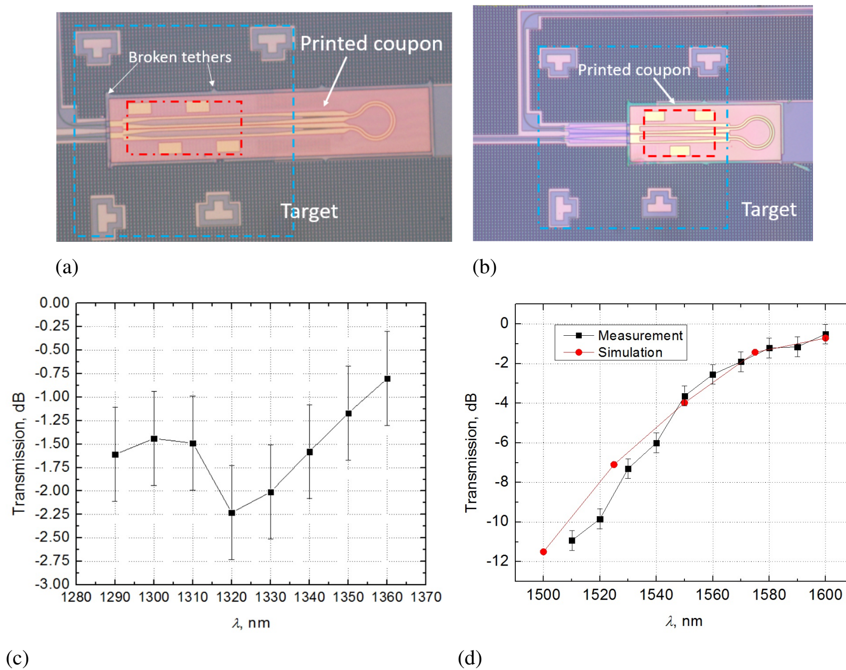
Het internet is een van de snelst groeiende sectoren ter wereld. Het vormt een ultrasnel communicatiekanaal dat vrijwel overal ter wereld toegankelijk is. Met de recente explosie van sociale netwerkplatformen, cloud computing en video-on-demand services bereikte het wereldwijde dataverkeer een volume van 11.6 Zettabytes (ZB) in 2018 en naar verwachting zal dit tegen het jaar 2021 nog bijna verdubbelen tot 20.1 ZB [1]. Naarmate de gegevenssnelheden in het centrale vezelnetwerk omhoogschieten, wordt het echter steeds moeilijker om de gegevensoverdracht op andere plaatsen in het netwerk, zoals in datacenters, te faciliteren.

Het is al lang duidelijk dat met de steeds toenemende gegevenssnelheden elektrische interconnecties niet voldoen, ook niet voor korte afstanden, omdat ze te veel vermogen verbruiken, een beperkte bandbreedte hebben en last hebben van overspraak. Optische interconnecties kunnen daarentegen een hoge bandbreedte, lager stroomverbruik en kleinere vertraging bieden. Daarom kunnen inter- of intra-chip optische verbindingen een mogelijke oplossing zijn voor deze bottleneck. In deze optische interconnecties worden de zender en ontvanger typisch geïntegreerd in één fotonische gentegreerde schakeling (PIC). De voordelen van siliciumfotonica bij het bouwen van deze systemen zijn aanzienlijk: siliciumfotonica heeft een hoge mate van volwassenheid bereikt en een aantal producten gebaseerd op deze technologie zijn ondertussen op de markt verschenen.

Silicium PIC-technologie is echter niet perfect en er zijn nog een aantal belangrijke uitdagingen. De monolithische integratie van Germanium op een Si fotonica platform is bijvoorbeeld een duur en soms inefficint proces. Ge-epitaxy verhoogt het aantal processtappen voor het realiseren van een Si fotonische chip gevoelig. Dit heeft een aanzienlijke impact op de turnaround-tijd en dus de ontwikkelingstijd voor nieuwe productgeneraties. Ook wafer-schaal integratie van III-V halfgeleider componenten zoals efficiënte lasers, versterkers, modulatoren en fotodetectoren op het Si-fotonica platform is moeilijk.

Transferprinting is een nieuwe heterogene integratietechnologie die een oplossing kan bieden voor deze problemen. Het is een technologie waarbij (arrays van) geprefabriceerde componenten selectief van een bronwafer worden opgepikt

en verplaatst worden naar een doelwafer, waar ze geprint worden op de gewenste plaats. Succesvol printen vereist echter een intensieve procesoptimalisatie, en de ontwikkeling van het release-proces en de juiste houders (tethers) voor de broncomponent (de coupon) is essentieel. In deze thesis presenteren we de resultaten van deze procesontwikkeling en de resultaten van het printen van SiGe en III-V fotodetectoren.

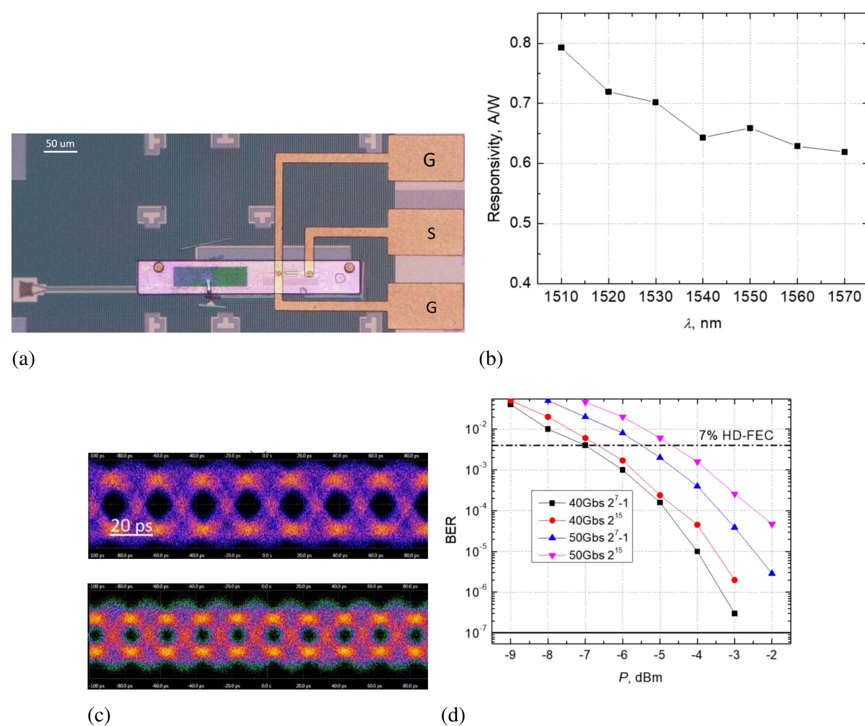


Figuur 1: Transfer printen van uitlijningstolerante koppelingsstructuren. Adiabatische structuur die werkt bij 1310 nm (a), directionele koppelaar die werkt bij 1600 nm (b), en transmissiemeetresultaten per koppelaar voor adiabatische structuur (c) en voor directionele koppelingsstructuur (d).

Alignatie-tolerante koppelingsstructuren

We ontwikkelden een aantal alignatie-tolerante koppelingsstructuren: een adiabatische taper (Figuur 1 (a)) en een directionele koppeling (Figuur 1(b)) die beide efficiënt het licht kunnen koppelen, zelfs bij een alignatiefout van $\pm$ 1 μm, en dat zowel bij golflengtes rond 1310 nm als 1600 nm. We ontwikkelden een process om SOI-gebaseerde componenten van hun substraat los te maken gebruikmakend van waterstoffluoride (HF). We optimaliseerden het ontwerp van de zogenaamde tethers, die de coupon vasthouden boven het substraat. Het koppelverlies van een enkele interface bedroeg 1.5 $\pm$ 0.5 dB voor de adiabatische taperkoppeling (Fi-

guur 1(c)) bij 1310 nm en 0.5 ± 0.5 dB voor de directionele koppelaar bij 1600 nm (figuur 1, onder d)).



(a) (b)

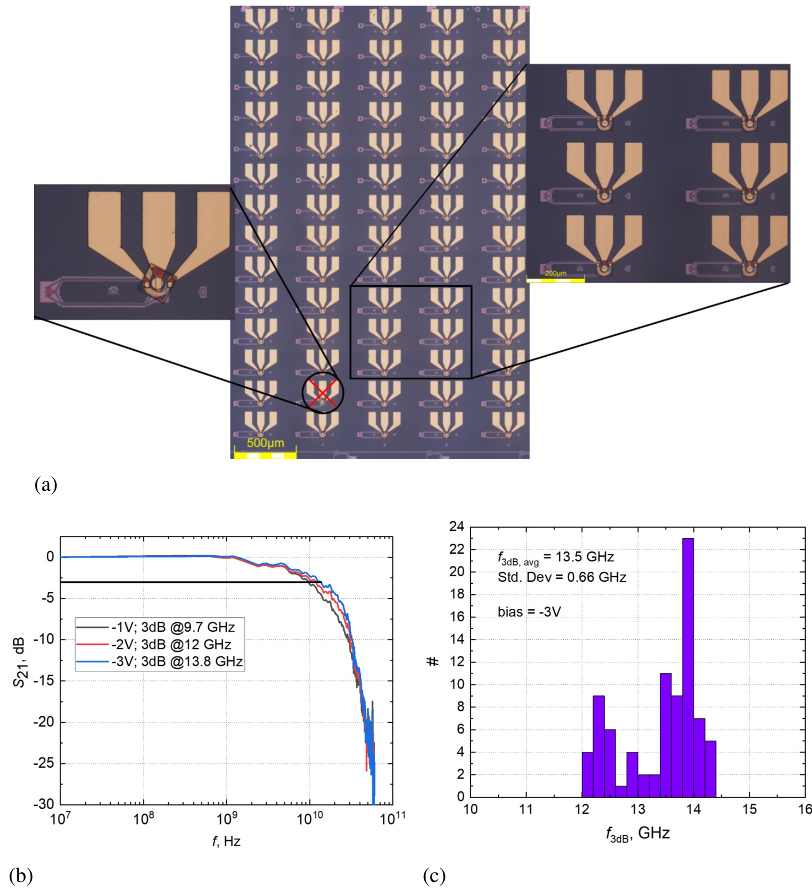
(c) (d)

Figuur 2: Microscoopafbeelding van een geprinte iSIPP25G SiGe-photodetector (a), de responsiviteitsmeting (b), oogdiagrammen bij 40 Gbit / s voor een PRBS 2^7-1 patroonlengte (boven) en bij 50 Gbit/s voor een PRBS $2^1$5 patroonlengte (c), de bitfoutmetingen voor 40 Gbit/s en 50 Gbit/s voor 2^7-1 en $2^1$5 PRBS-patroonlengtes (d).

Transfer-printen van iSSIP25G SiGe fotodetectoren

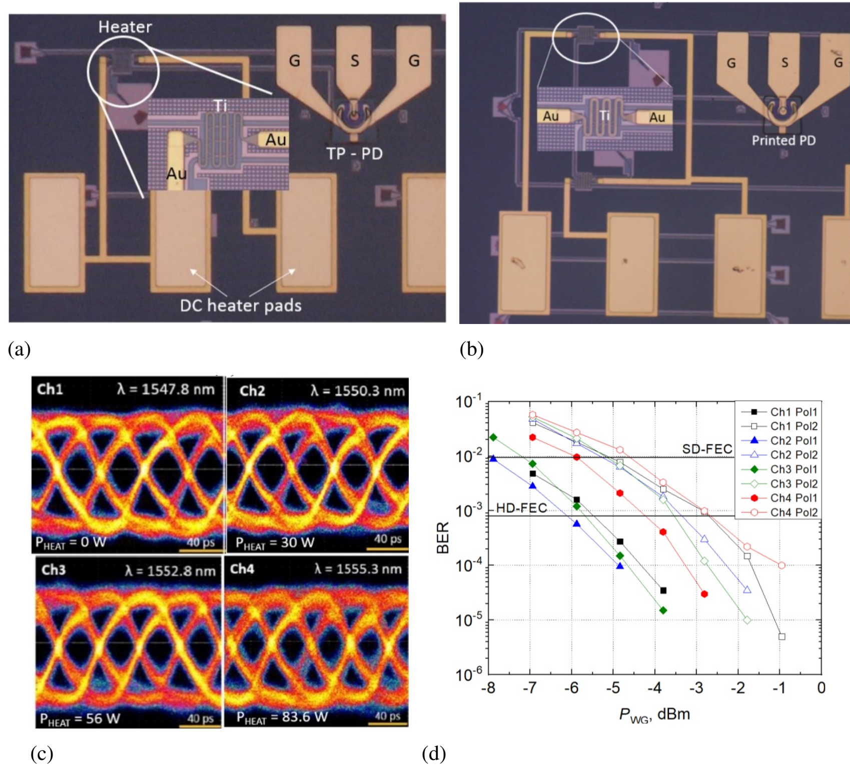
We hebben gebruikmakend van het ontwikkelde release-proces en het geoptimaliseerde tetherontwerp, aangetoond dat het mogelijk is germanium fotodiodes met hoge bandbreedte op passieve silicium golfgeleiders te printen. Dankzij het alignatie-tolerante ontwerp en het geoptimaliseerde proces maten (Figuur 2(a)) we een responsiviteit van 0.66 A/W bij 1550 nm, een heel goede waarde (Figuur 2(b)). Ook open oogdiagrammen (Figuur 2(c)) en transmissie bij 50 Gbit/s werden gedemonstreerd (Figuur 2(d)).

Parallel transfer-printen van in-huis gefabriceede InP/InGaAs fotodetectoren



Figuur 3: Microscoopafbeelding van parallel geprinte III-V fotodiodes. (a). Kleinsignaalmeetresultaat van één component (b). Histogram van kleinsignaalkarakteristieken van alle 83 geprinte componenten (c).

In dit werk ontwikkelden we de transfer van langs het substraat belichte III-V C-band fotodetectoren. De fotodetectoren werden gefabriceerd en van het substraat vrijgemaakt met behulp van een $FeCl_3$ oplossing. We ontwikkelden opnieuw de vereiste tethers, ditmaal in een fotoresistlaag, en konden aantonen dat deze inderdaad op de verwachte plaats breken bij het oppikken van de coupons. We gebruikten daarbij de automatische transferprinting en alignatieprocedure om de reproduceerbaarheid en betrouwbaarheid van het proces te demonstreren. Van de 84 componenten, werden er 83 goed geprint. Een van de verkeerd gedrukt componenten vertoonde een opvallende draaiing (Figuur 3(a)). Vervolgens werd de bandbreedte van deze componenten opgemeten. Een typisch resultaat voor een component met bandbreedte 13.8 GHz (-3V bias) wordt getoond in Figuur 3(b).



(a) (b)

(c) (d)

Figuur 4: Microscoopbeelden van kanaal 1 van de ontvangers voor enkele polarisatie (a) en polarisatie-diversiteit (b) met de geprinte fotodetectoren. Oogdiagrammetingen voor de ontvanger met enkele polarisatie, die de resonantie afstemt met behulp van microscopische verwarmingselementen (c). Bit-error-rate metingen voor de polarisatie-diversiteitsontvanger voor orthogonale polarisaties (d).

Figuur 3(c) toont een histogram voor de bandbreedte van alle 83 opgemeten componenten. De gemiddelde bandbreedte was 13.5 GHz met een standaarddeviatie van 0.66 GHz (Figuur 3c)).

Transfer-printen van fotodetectoren met een lage donkerstroom voor III-V/Si WDM ontvangers

Tot slot demonstreerden we de integratie van deze detectoren met een demultiplexer bestaande uit 4 afstembare ringresonatoren. Zowel een polarisatiegevoelige (Figuur 4(a)) als een polarisatie-ongevoelige (Figuur 4(b)) versie werden gedemonstreerd. Open oogdiagrammas toonden aan dat beide types ontvangers in principe tot 25GBit/s per kanaal kunnen worden gebruikt, voor een totale bandbreedte van 4×25 Gbit/s (Figuur 4(c)). De polarisatie-ongevoelige ontvanger

vertoonde polarisatie afhankelijke verliezen van 2.5 dB. Bit error metingen demonstreerden dat foutvrije transmissie mogelijk is voor beide polarisatietoestanden (Figuur 4(d)).

Conclusies

In dit doctoraatsonderzoek hebben we de mogelijkheden van een nieuwe heterogene integratietechnologie, transferprinten, onderzocht en het gebruik ervan aangetoond in diverse toepassingen. We ontwikkelden de nodige processen voor de fabricage en het printen van zowel germanium als III-V halfgeleider fotodetectoren op silicium-fotonische gentegreerde schakelingen. De resultaten van dit proefschrift demonstreren de mogelijkheden van de transferprinttechnologie voor de kost- en tijdsefficiënte realisatie van complexe fotonische geïntegreerde schakelingen.

Referenties

[1] Cisco Global Cloud Index. *Forecast and Methodology, 2016 2021 White Paper*. https://www.cisco.com/c/en/us/solutions/collateral/service-provider/global-cloud-index-gci/white-paper-c11-738085.html.

English summary

In this work we developed transfer printing technology to heterogeneously integrate silicon-germanium and III-V photodetectors on silicon photonic integrated circuits.

The Internet is one of the fastest-growing sectors in the world. Although it was slow in the beginning, today it has become an ultra-fast, huge data-rate traffic communication channel accessible virtually anywhere in the world. With the recent explosion of social network platforms, cloud computing, and video-on-demand services, a world data traffic of 11.6 Zettabytes (ZB) was estimated in 2018 and this number will nearly double by the year 2021 to about 20.1 ZB [1]. As data rates skyrocket, however, it has become more and more difficult to accommodate the data transfer in other places in the network, such as inside data centres.

It has quickly become clear that with the ever-increasing data rates, electrical interconnects cannot do an adequate job as they are power hungry, have limited bandwidth, and suffer from cross-talk. In contrast, optical interconnects can provide advantages of high bandwidth, low power consumption, and low latency. Therefore, rack-to-rack, board-to-board, chip-to-chip or intra-chip optical interconnects could be a possible solution to the data problem. In these optical interconnects, the transmitter and receiver can be integrated in one chip and built in the form of photonic integrated circuits (PICs). The advantages of silicon photonics when building these devices are quite considerable, with silicon photonics reaching a high level of maturity and a number of silicon optical transceivers appearing on the market.

Si PIC technology is not perfect, however, and comprises several key challenges. For example, monolithic Ge integration on a full Si photonics platform is an expensive and sometimes inefficient process. Ge processing increases the number of processing steps for the full iSSIP50G platform. This significantly impacts the turnaround time and hence the development time for new device generations. Also, wafer-scale integration of III-V devices, which includes efficient lasers, amplifiers, modulators, photodetectors, etc. on the Si photonics platform is still limited.

Micro-transfer-printing is a novel heterogeneous integration technology for opto-electronic devices on a Si photonics platform and can provide a compelling solution to these problems. It is a technology whereby (arrays of) prefabricated devices can be selectively picked from a source wafer and transferred to a target wafer, maintaining a constant pitch. Successful transfer printing requires process

optimization, however, and development of the release process and proper tethering of the coupon is key. In this work, we present the results of micro-transfer-printing of SiGe photodetectors and III-V photodetectors.

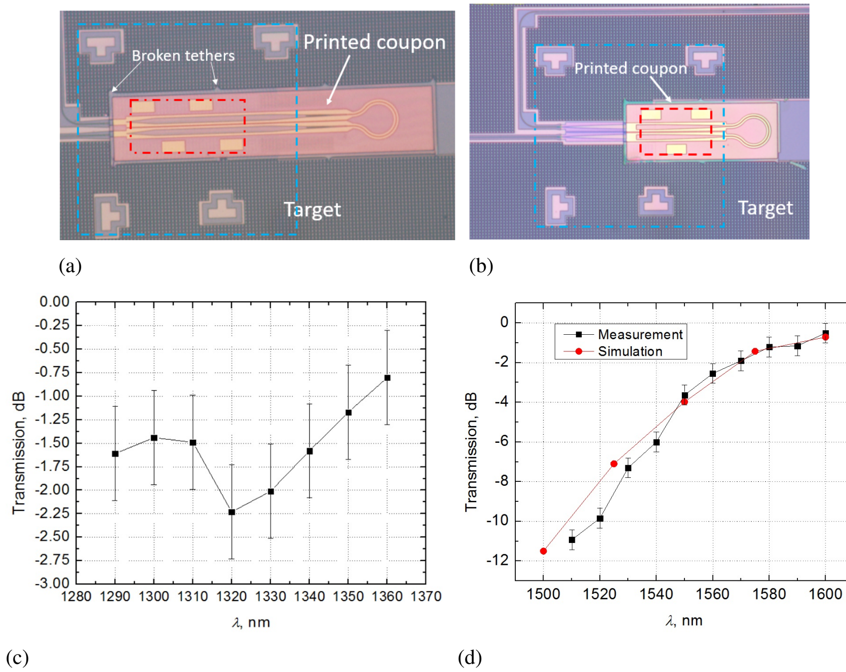


Figure 5: Transfer printing of alignment tolerant coupling structures. Adiabatic taper structure operating at 1310 nm (a), directional coupler operating at 1600 nm (b), and transmission measurement results per coupler for the adiabatic taper structure (c) and for the directional coupler structure (d).

Micro-transfer-printing alignment tolerant coupling structures

We developed an SOI release scheme to demonstrate micro-transfer-printing of passive silicon photonic devices on a silicon photonic target waveguide substrate. We designed compact alignment tolerant coupling schemes: an adiabatic taper (Figure 5(a)) and a directional coupler (Figure 5(b)) structure that can efficiently operate at ± 1 μm misalignment in the 1310 nm and 1600 nm wavelength range, respectively. An SOI coupon release scheme was developed by underetching the buried oxide layer using hydrofluoric (HF) acid and we optimized a triangular tether design. The coupling loss of a single interface was - 1.5 $\pm$ 0.5 dB for the adiabatic taper (Figure 5(c)) coupler at 1310 nm and - 0.5 $\pm$ 0.5 dB for the directional coupler at 1600 nm (Figure 2(d)).

Micro-transfer-printing iSSIP25G SiGe photodetectors

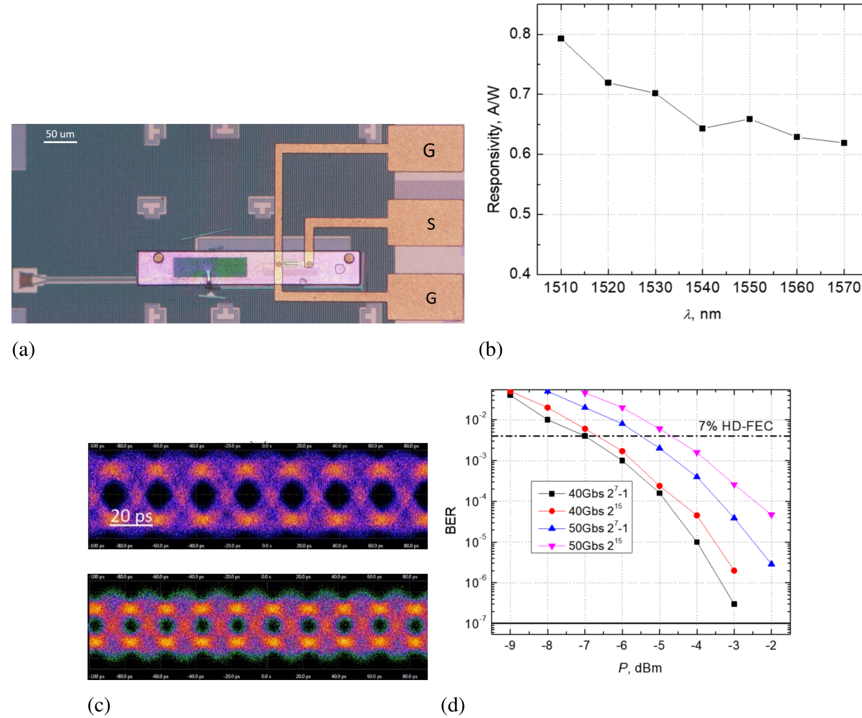


Figure 6: Microscope image of a transfer printed iSIPP25G SiGe photodetector (a), its responsivity measurement (b), eye diagrams at 40 Gbit/s and PRBS 2^7-1 pattern length (top) and at 50 Gbit/s (PRBS 2^{15} pattern length) (c), the bit-error-rate measurements for 40 Gbit/s and 50 Gbit/s for 2^7-1 and 2^{15} PRBS pattern lengths (d).

We exploited the SOI release scheme and triangular tether design to demonstrate the micro-transfer-printing of high-speed silicon-germanium photodiodes on a silicon-on-insulator passive waveguide circuit. We managed to successfully release the devices, while leaving the back-end stack intact. After successful transfer printing and post-processing (Figure 6(a)) we obtained 0.66 A/W responsivity at 1550 nm (Figure 6(b)), open eye diagrams (Figure 6(c)), and sub HD-FEC data reception at 50 Gbit/s (Figure 6(d)).

Parallel micro-transfer-printing of in-house fabricated InP/InGaAs substrate-illuminated photodetectors

We demonstrated parallel transfer printing of in-house fabricated substrate-illuminated III-V C-band photodetectors. We released these using a 3°C $FeCl_3$ solution and we developed the photoresist tethers, which broke in the correct places when picked. We exploited the automated mode of transfer printing to demonstrate

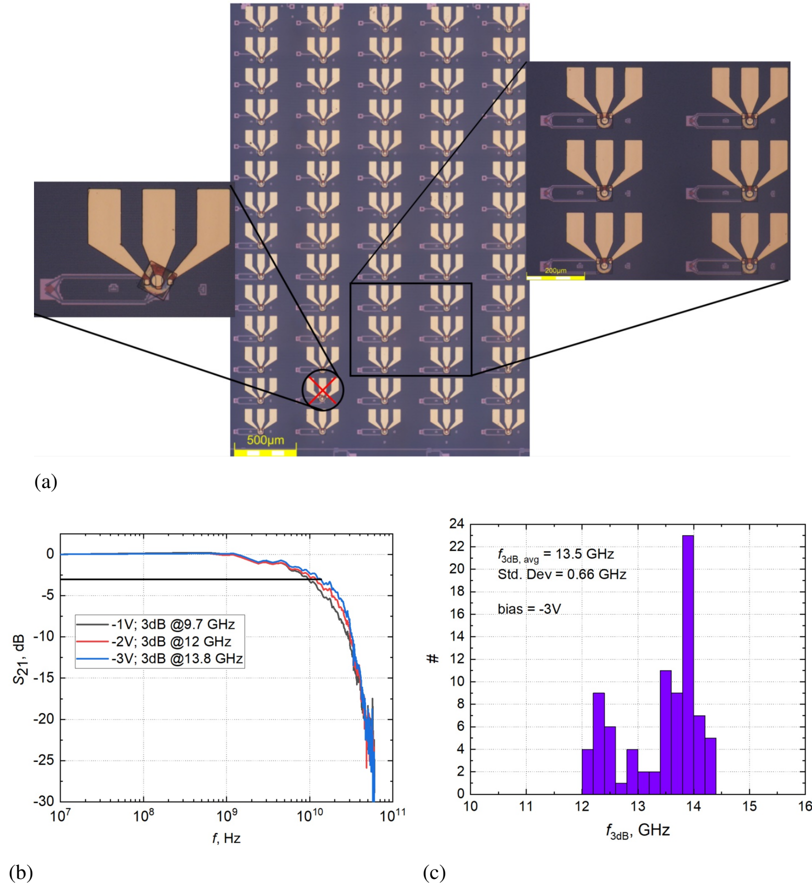
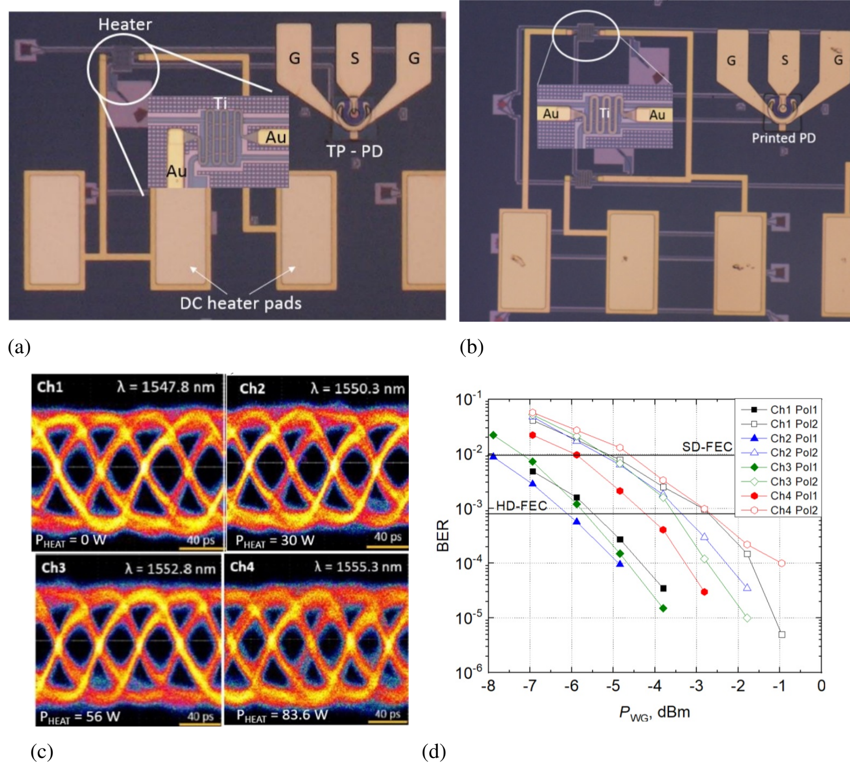


Figure 7: Microscope image of the parallel transfer-printed substrate-illuminated in-house-fabricated III-V PDs (a). Small signal measurement result of one device (b). Histogram of small signal characteristics of all 83 transfer-printed devices (c).

high-yield arrayed transfer printing. Eighty-three out of 84 devices printed well, with one device printed with a noticeable rotational misalignment (Figure 7(a)). Small signal measurements indicated a 3dB bandwidth of 13.8 GHz at -3 V for one device (Figure 7(b)). A histogram of all 83 transfer-printed devices indicated that 13.5 GHz was the average bandwidth with a standard deviation of 0.66 GHz (Figure 7(c)). Uniform operation indicated that the printing yield was above 98%.

Micro-transfer-printing of low dark current photodiodes for III-V/Si WDM receivers

Finally, we demonstrated a single-polarization (Figure 8(a)) and a polarization-



(a) (b)

(c) (d)

Figure 8: Microscope images of channel 1 of the single-polarization (a) and polarization-diversity receivers (b) with the transfer-printed photodiodes. Eye diagram measurements for the single-polarization receiver tuning the resonance using the heaters (c). Bit-error-rate measurements for the polarization-diversity receiver for both states of polarization (d).

diversity (Figure 8(b)) tunable ring resonator receiver transfer-printing similar III-V p-i-n photodetectors on silicon photonic WDM circuits. Eye diagrams showed 4×25 Gbit/s operation can be obtained for both receivers (Figure 8(c)). The polarization-diversity receiver showed 2.5 dB polarization-dependent losses and bit-error-rate measurements showed transmission below HD-FEC for both polarization states (Figure 8(d)).

Conclusion

In this doctoral research, we presented the merits of a novel heterogeneous integration technology - micro-transfer-printing, and demonstrated its use in fabricating, releasing, and transfer-printing of silicon-germanium and III-V photodetectors on silicon photonic integrated circuits. The results of this thesis showcase

the potential of micro-transfer-printing technology for cost- and time-efficient realization of complex photonic integrated circuits.

References

[1] Cisco Global Cloud Index. *Forecast and Methodology, 2016 2021 White Paper*. https://www.cisco.com/c/en/us/solutions/collateral/service-provider/global-cloud-index-gci/white-paper-c11-738085.html.

1
Introduction

In the first chapter, we will introduce the main theoretical aspects and the motivation for this PhD work. We will start from the basics of optical communication and move on to the main concepts of silicon photonics and available technologies. Then we will introduce integrated photodiodes, their most important metrics and the current state-of-the-art of these. We will give an overview of the available heterogeneous integration technologies and the rationale why the development of micro-transfer-printing technology is the choice for this work. We will conclude the chapter by describing the basic physical principles of micro-transfer-printing and introducing the lab-scale printer that was used for printing devices in this work.

1.1 Fiber-optic networks

The Internet is one of the fastest-growing sectors in the world. Developed initially as a military communication channel [1] in the 1980s, it became accessible to the public as the World Wide Web (WWW) [2]. In the beginning, it was often slow during online communication or gaming and had limited capacity, but soon grew into an ultra-fast, huge data-rate traffic communication channel, accessible virtually anywhere in the world. With the recent explosion of social network platforms (e.g. Facebook, Instagram), cloud computing (e.g. Amazon), video-on-demand services (e.g. YouTube, Netflix), a world data traffic of 11.6 Zettabytes (ZB) in 2018 was estimated. Moreover, CISCO predicts that this number will nearly double by the year 2021 to about 20.1 ZB [3].

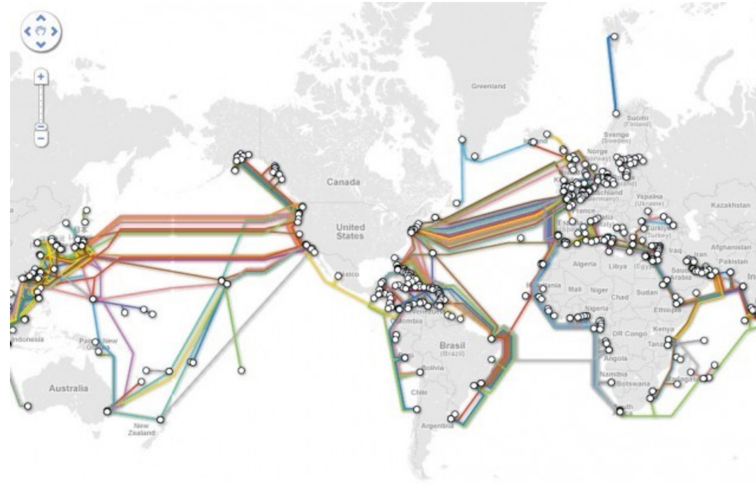


Figure 1.1: Fiber optics connectivity on the bottom of seas and oceans [4].

These impressive numbers were mainly achieved by the development of optical fiber technology. Switching from lossy electrical copper connections to low-loss, high-bandwidth optical fiber networks enabled intercontinental reach and data-stream multiplexing [5]. Figure 1.1 shows fiber optic cables at the bottom of seas and oceans. Nowadays, a link between San Francisco and Tokyo can operate with a capacity of up to ∼60 Tb/s [4]. However, as data rates skyrocket, it becomes more difficult to accommodate the data transfer in other places in the network, such as inside data-centers. Energy-efficient and high-speed communication between servers inside a data-center became a new research problem.

1.1.1 Interconnects

The endless need for data led to warehouse-like data centers (Figure 1.2), which consist of hundreds of thousands of servers. It quickly became clear that with the ever-increasing data rates, electrical interconnects cannot do the job as they are power-hungry, have limited bandwidth, and suffer from cross-talk [6].

Optical interconnects can provide advantages of high bandwidth, low power consumption and low latency, and solutions are already being applied in short-haul (up to 80 kilometers, between data-centers) and very-short-haul (up to 2km, inside the data-center: rack-to-rack, server to server, board to board) communication. Chip-to-chip or intra-chip optical interconnects are still in a research phase. Nonetheless, an all-optical interconnect roadmap is already set with stringent requirements of high bandwidth and low power consumption [8]. The latter sets important ecological measures as high electricity usage increases greenhouse gas

Figure 1.2: Data center with optical interconnects [7].

emissions [9].

1.1.2 Optical communication link

A simplified optical communication link is schematically displayed in Figure 1.3. The heart of the transmitter is a laser that generates a continuous-wave (CW) optical signal at particular wavelength λ and an external modulator that converts the CW optical laser signal to the modulated digital bit sequence generated by e.g. a central processing unit (CPU). The CPU digital signal can be applied directly on the laser without the need for external modulators: for example, a high-speed, directly-modulated laser (DML) operating up to 56 Gbit/s has recently been demonstrated [10], [11] [12]. The modulated optical signal couples to the optical fiber and traverses the long distance. At the other end of the link, the receiver consists of a photodiode, which converts the optical signal to the electrical domain. Usually, when the optical signal arrives to the other end of the optical fiber, distorted and attenuated, the amplifier and equalizer restore the original shape of the signal sent by the transmitter and thereafter the digital signal processing (DSP) continues to process the signal.

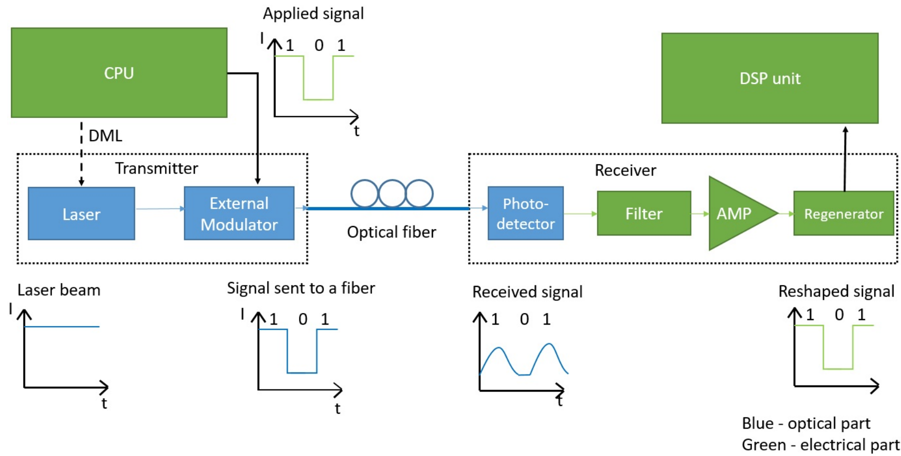


Figure 1.3: Schematics of an optical communication link.

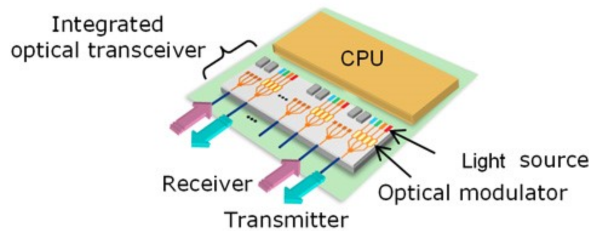


Figure 1.4: Schematic image of integrated optical transceiver proposed by Fujitsu [13].

1.1.3 Optical transceivers

In current optical interconnects, the transmitter and receiver can be integrated in one chip (hence it is called a transceiver) and built in the form of a photonic integrated circuit (PIC). An example is shown in Figure 1.4 [13]. Here, arrays of lasers and modulators are integrated to send different signals at different wavelengths. The circuit multiplexes these in order to increase the capacity of the communication channel. Similarly, the receiver part can demultiplex and read out the signal for each single wavelength.

The integrated transceiver is a compact and elegant solution for optical interconnects and many complex functionalities can be built into a small-sized chip.

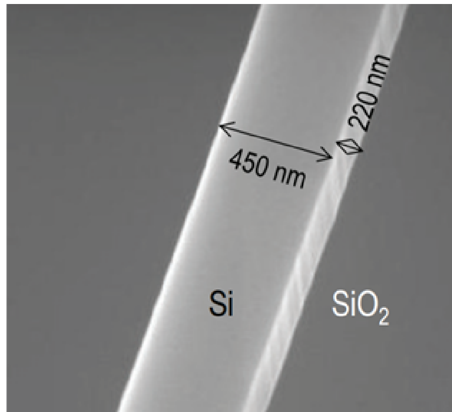


Figure 1.5: Scanning electron microscopy (SEM) image of a silicon waveguide implemented in the silicon-on-insulator material system.

1.2 Silicon photonics

A number of material platforms can be used for realizing PICs for integrated transceivers, such as III-V semiconductors or silicon. However, the advantages of silicon photonics (using silicon-on-insulator (SOI) wafers) over others are quite considerable [14]. The main component of a PIC is a waveguide: for silicon photonics this is a high refractive index silicon (n = 3.45) wire with a surrounding lower refractive index silicon oxide cladding (n = 1.45). The oxide acts as the buffer layer to prevent the mode leakage to the silicon substrate. The refractive index contrast allows the optical mode to be tightly confined and guided in the silicon waveguide between the different elements on the chip. Moreover, silicon is transparent in the telecom C- and O-bands, because of its bandgap of 1.12 eV. The high index contrast allows building very compact waveguides as one can see in Figure 1.5: the typical dimensions of a silicon wire waveguide is 220 nm height (310 nm, 400 nm and 500 nm height is also widely used) and a width of 450 nm. Silicon is abundant on Earth (it is found in sand, rocks, clays and soils, and is one of the most widespread elements in the Earths crust [15]); the developed complementary metal oxide semiconductor (CMOS) electronics industry enables the inexpensive fabrication of these photonic devices in large volumes.

Excellent small-footprint passive optical functionality has been developed over years of research. These demonstrations include high confinement low-loss waveguides [16], [17] with several micron radius waveguide bends [18], low-loss waveguide crossings [19], Bragg gratings [20], high Q-ring resonators [21], arrayed waveguide gratings [22], grating coupler structures [23], etc. By employing selective doping of silicon and epitaxial growth of germanium, one can add active

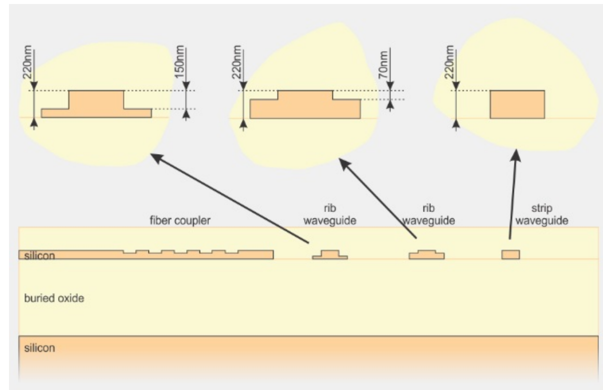


Figure 1.6: Schematics of the imec Si photonics passive technology platform [27].

functionalities in PICs, namely carrier-based modulators [24] and high-speed photodetectors [25].

Silicon photonics has reached a high level of maturity, and a number of silicon optical transceivers have appeared on the market [26]. This could not have been achieved without the development of Si photonics technology platforms in CMOS fabs.

1.2.1 Imec silicon photonics technology

Imec, one of the silicon photonics technology leaders, offers two types of silicon technology platforms, implemented on 200mm wafers: passive waveguide circuits and a Si photonics full platform technology called iSIPP50G.

1.2.1.1 Imec passive platform

The Si photonics passive technology platform consists of 200 mm wafers with Si substrates, a 2-micrometer-thick silicon buried oxide layer and a 220 nm silicon top layer (Figure 1.6) [27]. Three different Si etching steps are offered on the platform defined using 193 nm lithography: 70 nm shallow etch, 150 nm socket etch, and the full 220 nm etch. Moreover, one can choose different top claddings: air cladding or a high-density plasma oxide cladding which is chemically-mechanically polished (CMP) to make a no-topography side-oxide cladding, and 1-micrometer-thick top oxide cladding. Grating coupler structures are also available for efficient fiber interfacing.

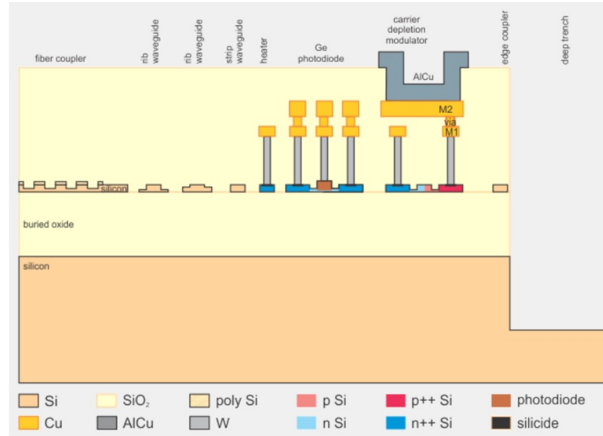


Figure 1.7: Schematics of the iSIPP50G full platform [28].

1.2.1.2 Imec iSIPP50G platform

Imec also offers an iSIPP50G full plafrom technology on 200 mm wafers. A cross-section is presented in Figure 1.7. In addition to the passive silicon structures with the different etching steps described above, it offers four p- and n-type doping levels, an additional poly-Si layer, a Ge epitaxial layer, and two levels of metal interconnects (M1 and M2). This enables the fabrication of high-speed carrier-depletion Si modulators, Ge electro-absorption modulators and Ge photodetectors (Figure 1.7). Together with efficient grating couplers, also efficient edge couplers are offered in the platform [28].

1.3 State-of-the art photodetectors integrated on silicon PICs

A key component for optical transceivers are high-speed photodetectors. Being positioned at the end of the optical link, their sensitivity determines the required laser power at the transmitter to close the link, and hence the power consumption of the link. Their bandwidth can also be the limiting factor determining the capacity of the link. On silicon photonic integrated circuits either Ge photodiodes or III-V photodiodes are integrated.

1.3.1 Photodetector metrics

The key photodetector metrics are responsivity (R, in A/W), dark current (I_D, in nA), response speed (or a 3 dB bandwidth - f_{3dB}, in GHz) and bias voltage

(V_{BIAS}).

Responsivity. This is the ratio of the generated photocurrent to the incident optical power (units A/W). The attributed figure of merit is the quantum efficiency or converted electrons per incident photon [29].

$$R = \eta \frac{q}{hf} \tag{1.1}$$

Here, η is the quantum efficiency, hf is the photon energy, and q is the elementary charge. The formula could be simplified to

$$R = \eta \frac{\lambda}{1.24} \tag{1.2}$$

A photodetector with a quantum efficiency of 1 has a responsivity of 1.25 A/W at a wavelength of 1550 nm. Typically, the generated photocurrent has a linear dependency on the applied optical power.

Dark Current. The dark current is defined as the small current flowing through the photodiode when there is no incident optical power when reverse biasing the diode. Typical dark current values are in the nA range.

Response speed. The ability of the photodetector to respond to the fast modulated optical signal and it is quantified by a 3dB bandwidth of the photodiode. The response speed is mainly determined by RC constant, the carrier transit time, and the diffusion of the generated photo-carriers [30]. Typically, smaller mesa sizes lead to lower capacitance and thus higher 3dB bandwidths. However there is a trade-off as attempting to reduce the mesa size can lead to the bandwidth and responsivity reduction under high input power. Current state-of-the-art integrated photodetectors have 3dB bandwidths beyond 67 GHz.

Bias voltage. This is the voltage which is applied to sweep all generated carriers out of the absorption region. Photodetector operates in reverse bias. Typical reverse voltage values are -1 V to -3 V. At high reverse bias voltages avalanche multiplication can occur, which increases the quantum efficiency and hence the sensitivity of the receiver (possibly at the expense of a bandwidth reduction).

1.3.2 Ge photodiodes

Figure 1.8 shows the Ge material absorption and compares it with Si [31]. One can see that germanium has strong absorption in the C-band (1.55 micron) and O-band (1.3 micron), which makes it an ideal candidate for photodetector applications at these telecom wavelengths.

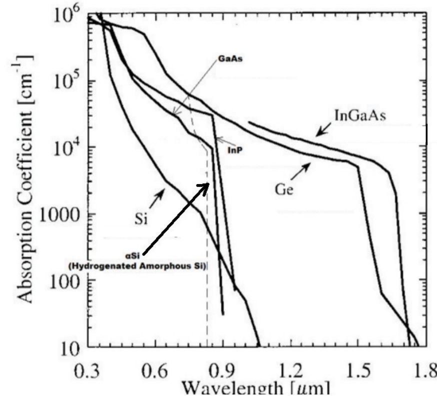


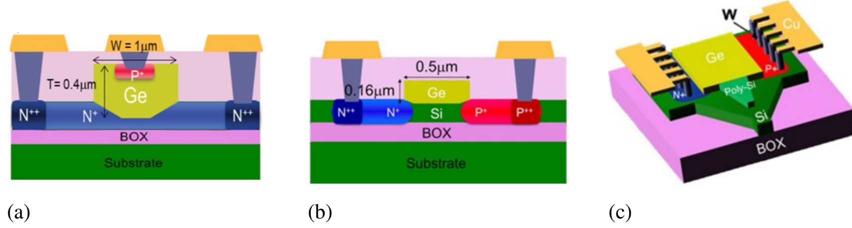
Figure 1.8: Absorption coefficient as a function of wavelength in selected semiconductor materials [31].

We will focus on state-of-the-art Ge p-i-n photodiodes and also discuss avalanche multiplication and state-of-the-art of these devices.

1.3.2.1 Ge p-i-n photodiodes

Ge photodetectors can be either surface-illuminated or waveguide-coupled p-i-n (WPIN) photodetectors [29]. More attention is paid to WPINs as they combine higher absorption lengths and high bandwidth [32]. An example of this is the so-called vertical p-i-n (VPIN) waveguide-coupled germanium photodiode, a cross-section of which is displayed in Figure 1.9(a). The light couples from the silicon waveguide to the photodetector using an adiabatic taper and gets absorbed in the Ge intrinsic layer. The absorbed light in the intrinsic layer generates electron-hole pairs. By applying a bias voltage, the generated carriers drift toward the highly doped areas: electrons move to the bottom N+ layers and holes traverse to the upper P+ contact, which is what creates the photocurrent in the circuit. 56 Gbit/s operation was demonstrated using VPINs [33].

However, the response speed limiting factors of the VPIN photodiode are its larger capacitance due to the wide mesa (1 μm) and higher contact resistance to the P+ Ge. This was improved by implementing state-of-the-art lateral p-i-n (LPIN) photodetectors, a cross-section of which is displayed in Figure 1.9(b) and 1.9(c). The light couples to the photodiode through an additional poly-Si taper (Figure 1.9(c)), and by employing lateral contacts on highly doped silicon N+ and P+ layers, the contact resistance decreases. Furthermore, using a narrower Ge mesa, the carrier-transit time is reduced as well as capacitance. These effects significantly decrease the RC constant, and this contributes to the increased response speed of the Ge photodiode: 100 Gbit/s operation was demonstrated using the LPIN



(a) (b) (c)

Figure 1.9: State-of-the-art Ge photodetector technology. (a) cross-section of the vertical p-i-n Ge photodiode; (b) cross-section of the lateral p-i-n Ge photodiode ; (c) cross-section of the lateral p-i-n Ge photodiode coupling structure [29].

photodetectors [29] [34].

1.3.2.2 Ge avalanche photodetectors

Integrated Ge photodetectors can also significantly improve the receiver sensitivity and reduce the cost of passive optical networks by implementing avalanche multiplication [35]. These devices are called avalanche photodetectors (APDs).

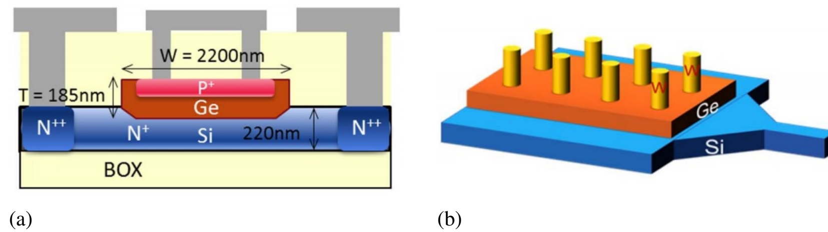
The architecture of such devices exploits an engineered doping profile. This means that a strong electric field is locally created so that when generated photoelectrons (and holes) in the intrinsic area are accelerated by the high electric field they collide with the bound electrons in the material, creating more charge carriers collected by the electrodes. This effect is called impact ionization or avalanche multiplication [36]. Therefore, the device enables carrier multiplication or gain close to the breakdown voltage [37] [38]. Both gain and the multiplication noise are important metrics of these devices, as germanium APDs suffer from excess noise.

Surface-normal Ge APDs were demonstrated with a Ge absorption layer and, a Si as the multiplication layer showing an impressive 340 GHz gain-bandwidth product (GBP) and -28 dBm receiver sensitivity at 10 Gbit/s. The issue with the device is that the avalanche voltage is -25 V, which falls outside the CMOS voltage range [39]. Smaller -3 V avalanche voltages were achieved using metal-semiconductor-metal (MSM) devices, but the large dark current limited the receiver sensitivity of the device [40].

The state-of-the-art approach is the 400-nm-thick Ge VPIN structure as already discussed in subsection 1.3.2, the cross-section of which is depicted in Figure 1.9(a). At a voltage of -6.2 V, a gain of 10.2 is obtained. The APD was wire-bonded to a 0.13 μm SiGe BiCMOS low-noise transimpedance amplifier (TIA). 10 GHz operation was demonstrated, producing a GBP value of 102 GHz with a 17 nA dark current and a primary responsivity of 0.6 A/W [29] [37].

It is clear that the desired operational features of the APD are to decrease the

avalanche voltage and to increase the GBP. In order to improve the performance further, a thinner 185 nm Ge layer is used with a wider 2.2 μm absorption region. The cross-section is shown in Figure 1.10. The thinner layer means that this device has a lower breakdown voltage [41]. The gain is lower (7) but 25 Gbit/s operation at the avalanche voltage of -5 V is obtained with the receiver sensivity of -14.8 dBm at 1×10^{-9} BER. This device demonstrates a GBP of 140 GHz.



(a) (b)

Figure 1.10: (a) Cross-section of the 185-nm-thick Ge avalanche photodetector. (b) Cross-section of the coupling structure [41].

1.3.2.3 Discussion

Ge-on-Si photodetector technology has achieved a high level of maturity over the years with a variety of devices, performance characteristics and applications. However, the monolithic Ge integration on a full Si photonics platform is an expensive and sometimes inefficient process, as the germanium photodetector density is typically small in a photonic integrated circuit.

Moreover, the Ge processing increases the number of processing steps for the full iSSIP50G platform. This impacts the turn around time and hence the development time for new device generations.

1.3.3 III-V photodiodes

A completely different material platform available for the fabrication of efficient high-speed photodiodes is III-V compound semiconductors. These materials are known to show excellent lasing performance, and therefore the co-integration of lasers and photodiodes on the Si photonics platform using one single or two separately optimized epitaxial layer stacks is an attractive solution.

InGaAs grown lattice-matched on InP substrates makes an appealing photodetector material for the telecom wavelength range. As shown in Figure 1.8, one can see that the InGaAs absorption curve extends to about 1.7 μm wavelength [31]. Moreover, one can tune the absorption cut off wavelength of the material by selecting x while growing the $In_xGa_{1-x}As$ alloy. For example, one can extend the

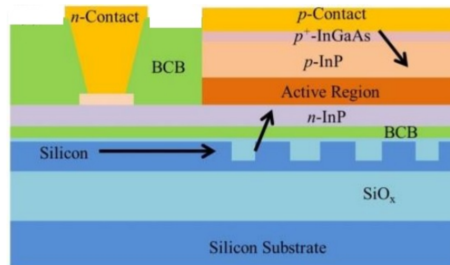


Figure 1.11: Cross section of the grating-assisted photodiode [48].

InGaAs material cutoff wavelength up to 2.5 μm (at the expense of a lattice mismatch with the InP substrate [42]).

By growing quaternary materials and incorporating Sb in the crystal lattice, one can push the cutoff wavelength even further. For example, by choosing an InGaAsSb quaternary layer, the bandgap can cover 1.7 - 4.3 μm, making it a compelling mid-infrared detector for sensing applications [43]. By choosing InGaAsP, one can set the cutoff wavelength at e.g. 1.37 μm, making a photodetector transparent in the C-band and absorbing in the O-band. This is particularly interesting for fiber-to-the-home (FTTH) point-to-point (P2P) full-duplex communications, and some interesting results have been demonstrated [44].

All this proves that III-V semiconductor materials provide a very versatile platform to realize photodetectors tailored to particular applications. We will focus on state-of-the art of the most common types of III-V photodetector integrated on a silicon photonic platform.

1.3.3.1 Grating-assisted p-i-n photodetectors

Integrating a III-V photodetector on top of a Si photonics grating coupler is one of the approaches (Figure 1.11). The grating directs the light propagating in a silicon waveguide upwards, where it gets absorbed by the intrinsic layer of the photodetector. Moreover, the additional photon reflection from the top p-metal contact can further increase the responsivity [45] [46] [47]. The advantage of this approach is that one can fabricate very compact photodiodes without requiring sophisticated structures for optical coupling.

1.3.3.2 Grating-assisted metal-semiconductor-metal photodetectors

A very different type of photodetector is a metal-semiconductor-metal (MSM) structure. The cross-section of a grating-assisted MSM is displayed in Figure 1.12. The device comprises two interdigitated comb-like metal contacts that are deposited on top of the flat III-V epitaxial material structure [49]. This is one of

the advantages of this device - the flat epitaxial layer stack makes fabrication of the device relatively simple, as it consists only of an absorption and contact layer [50].

Another advantage of the planar MSM photodiode structure is small parasitic capacitance, which enables a high-speed performance. Typically, the RC constant and carrier transit time are the two main factors limiting the speed. The capacitance of the MSM is [51]:

$$C = \frac{K(k)}{K(k')}\epsilon_0(1+\epsilon_r)(1+N)L \tag{1.3}$$

Here ϵ_0 is the dielectric constant in free space, ϵ_r the dielectric constant of the absorbing material, L the length of the active region, and N the number of the interdigitated fingers. K is the elliptical integral denoted as

$$K = \int_0^{\pi/2} \frac{1}{\sqrt{1-k^2\sin^2\phi}}\,d\phi \tag{1.4}$$

with k and k' being

$$k = \tan\frac{\pi f_w}{4(f_s+f_w)} \tag{1.5}$$

$$k' = \sqrt{1-k^2} \tag{1.6}$$

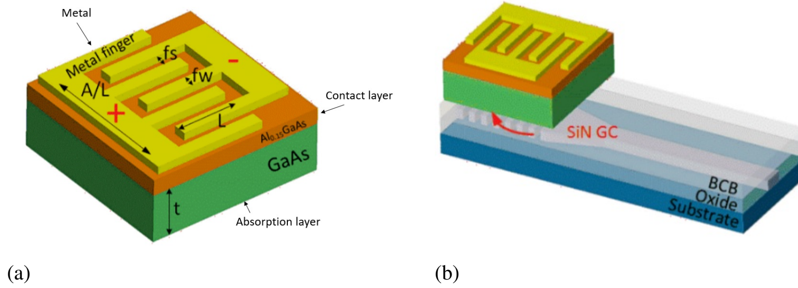
where f_s is the finger spacing and f_w is the finger width. Considering finger widths of about 1.5 to 2.5 μm, and a finger spacing of 1.5 μm, capacitance values below 30 fF are obtained for smaller devices (30 μm $\times$ 30 μm) and up to 90 fF for larger devices (70 μm $\times$ 70 μm) [49].

This device shows a lot of potential for applications in inter-chip (especially when multimode fiber links are considered) communications. The example displayed in Figure 1.12 is a GaAs MSM photodetector integrated into a silicon nitride photonics platform using a grating coupler interface (Figure 1.12(b)). It operates at near-infrared wavelengths (850 nm) and can be co-integrated with vertical cavity surface emitting lasers [52]. Compact visible/near-infrared light detectors integrated on a silicon nitride photonics platform can be also useful in sensing applications [53].

The drawback of this device is that it is sensitive to processing imperfections.

1.3.3.3 III-V waveguide photodiodes

One of the most significant drawbacks using the grating-assisted coupling method is limited responsivity, as a grating coupler diffracts the light upwards to the integrated detector, but also downwards to the substrate, as shown in Figure 1.13. This way, for a standard grating coupler structure $\simeq 70\%$ of the light propagating



(a) (b)

Figure 1.12: (a) Schematic cross-section of grating-assisted MSM. (b) Grating-assisted MSM integrated into a silicon nitride platform [49].

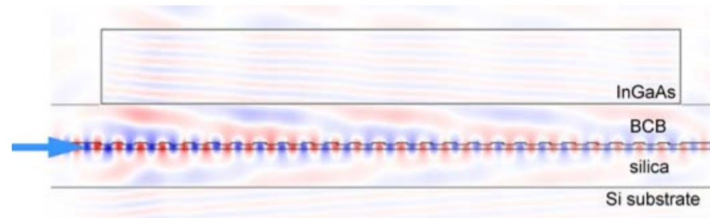


Figure 1.13: Cross-section of the simulation of the light difraction using a silicon photonics grating coupler [51]

in the Si waveguide is directed towards the detector, while another $\simeq 30\%$ is lost in the substrate. This is not ideal for telecommunications, where in many applications receiver sensitivity is of upmost importance. Sophisticated solutions, such as employing bottom metal mirrors or distributed Bragg reflector (DBR) layers [54], could be applied to improve the efficiency [55].

Another way to obtain higher photodetector responsivities is to use evanescent coupling techniques. Schematically, this is displayed in Figure 1.14. When the optical mode propagates in the silicon waveguide and encounters an integrated III-V waveguide on top, because the refractive indices of silicon and III-V are closely matched, phase matching can be achieved, meaning that optical power can be completely transferred to the integrated III-V waveguide where it is being absorbed by the active layer of the detector. 93% of light was absorbed in this example [51], as shown in Figure 1.13. By correctly engineering the coupling structure, a theoretical efficiency of 100% could be obtained.

An additional disadvantage of a grating-coupled photodetector is the trade-off between responsivity and bandwidth, as a thick absorption region (needed for high responsivity) inreases the carrier transit time and hence reduces the bandwidth of

Figure 1.14: Cross-section of the simulation of the evanescent coupling [51]

the device.

Waveguide-coupled p-i-n and MSM photodetectors can be used to overcome these issues. The waveguide-coupled p-i-n photodetector is shown in the example in Figure 1.15. The light propagating in the 220 nm × 500 nm silicon waveguide evanescently couples to the phase-matched n-InP waveguide using a directional coupler. This layer is also used as a n-contact of the photodetector. The 700-nm InGaAs intrinsic absorption layer then absorbs the light coupled from the n-InP waveguide layer and a 70-nm p-InGaAs layer is used as a p-contact [56].

The device with a 50 μm^2 mesa shows a dark current of 1.6 nA, responsivity of 0.45 A/W and a 3dB bandwidth of 35 GHz. The poorer responsivity of the device can be attributed to the InP coupler loss and the intrinsic quantum efficiency of the photodetector.

The advantage of III-V photodetector processing is that it is also compatible with integrated laser fabrication. In fact, some demonstrators involve reverse-biased lasers used as photodetectors, and such integrated p-i-n photodetectors yield responsivities up to 1.1 A/W at λ = 1580 nm [57] [58].

The cross-section of a waveguide-coupled MSM is shown in Figure 1.16 [59]. The device consists of an InGaAs absorption layer, an InAlAs contact layer and a lattice-matched InAlAs/InGaAs digitally graded superlattice to decrease the carrier trapping effect, which is sandwiched between the absorption and contact layer. The light is fed using a phase-matched InGaAs/Si directional coupler. Two 3-μm spaced co-planar Ti/Au Schottky contacts help to reduce the carrier transit time by introducting an electric field in the structure and improve the lateral optical confinement of the detector, which helps to increase the absorption efficiency. A responsivity of 1.0 A/W for a 25-μm-long device at 1550 nm was demonstrated [59].

The drawback of the waveguide-coupled photodiodes is that responsivity becomes dependent on the light coupling scheme and optimization of an efficient Si-to-III-V coupling transition is essential. Moreover, the coupling becomes dependent on III-V-to-Si waveguide alignment accuracy [51]. In case of heterogeneous integration (discussed later) using an adhesive bonding layer, thickness variation of this layer can impact the coupling efficiency.

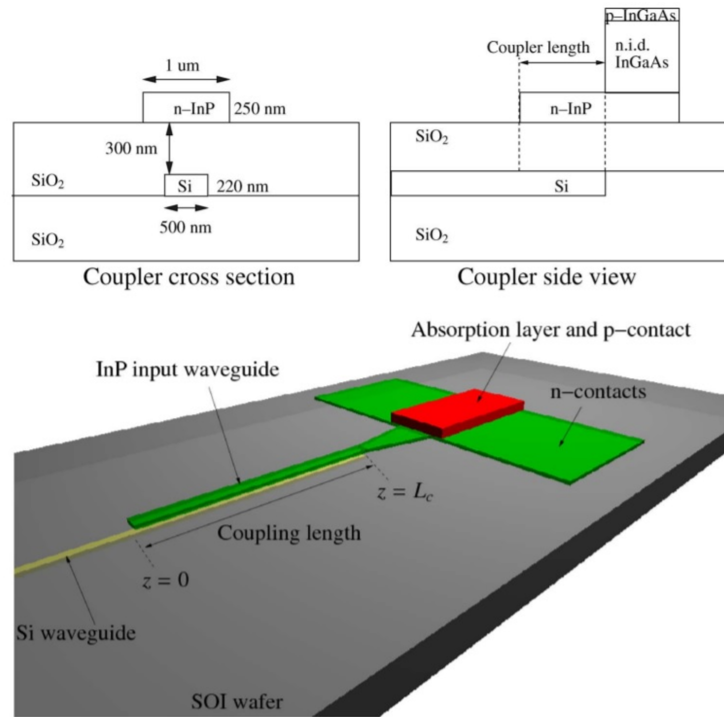
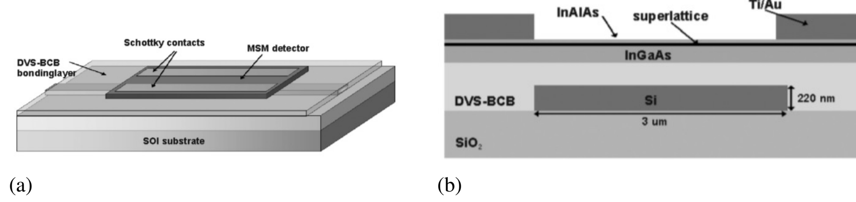


Figure 1.15: Schematics and cross-section of a waveguide-coupled integrated III-V p-i-n photodetector. [56]

1.3.3.4 Waveguide-coupled uni-travelling carrier photodiodes

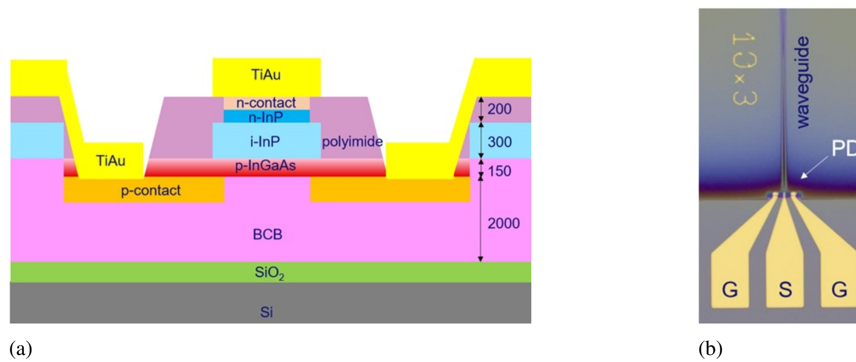
The drawback of the p-i-n photodetectors is that these devices rely on generated electron and hole transit. Holes are heavy particles and their mobility is low, which limits the speed of these photodiodes [60]. A compelling way to make a high-speed III-V photodetector is to use only electrons as the active carriers in the depletion area. Such photodetectors are called uni-traveling-carrier photodetectors (UTC-PDs). Using only electrons as active carriers leads to a higher velocity, thus lowering transit time and reducing space charge effects. III-V materials are desirable for designing UTC-PDs, as they exploit the bandgap engineering and velocity overshoot effects [61] [62].

An example of such a photodetector is shown in Figure 1.17. The III-V photodetector was integrated on a silicon carrier wafer using wafer bonding technique and is butt-coupled to a passive InP membrane waveguide. The absorption layer here is the thin bottom p-InGaAs. The bottom p-contacts were pre-processed on the bottom side before the bonding. These bottom electrodes enable direct hole collection, whereas the fast-moving electrons travel through an i-InP layer



(a) (b)

Figure 1.16: Schematics of an integrated waveguide-coupled MSM photodetector: (a) Side view (b) Cross-section [59].



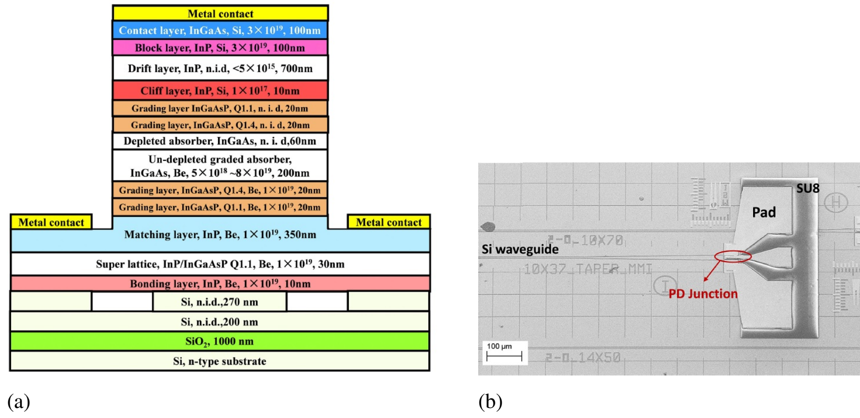
(a) (b)

Figure 1.17: Cross-section of a butt-coupled uni-traveling-carrier photodiode [62].

to the top n-contact. The 3×10 μm^2 device heterogeneously integrated on Si demonstrated >67 GHz of 3-dB bandwidth and a responsivity of 0.7 A/W at 1.55 μm [62].

The UTC-PDs are useful components in high-power, high-frequency applications, such as analog photonic links, low-phase noise microwave generator, fiber-optic antennas that transmit and receive wireless signals and in coherent digital optical communication systems [63]. An InP material system is desired for this, predominantly because of the bandgap engineering properties, as the epitaxial material stack with the desired electronic properties can be engineered.

This is demonstrated by integrating a so-called modified UTC-PD or MUTC-PD on a silicon waveguide [65], the cross-section of which is displayed in Figure 1.18. Here, the undepleted absorber layer is made thinner (200 nm) to improve the electron transit time and sandwiched between two thin (40 nm) bandgap-graded InGaAsP layers, which smoothen the abrupt band barrier and helps to prevent the carrier pile-up effect. On top, the PD uses a 10-nm-thick, highly doped n-type cliff layer to enhance the electric field and to assist the electron transport across the heterojunction interface at high powers, as well as a 700-nm drift layer, which helps to further decrease capacitance. An important layer to the device performance



(a) (b)

Figure 1.18: (a) Cross-section of a modified uni-traveling-carrier photodiode integrated on a silicon waveguide; (b) top view [64].

is the highly doped bottom n-type InP layer, which decreases series resistance, as well as the InP/InGaAsP superlattice, which prevents defect propogation during the bonding process [64]. The PD is directly bonded onto the SOI and has a waveguide coupling interface. 10×21 μm and 10×35 μm-long photodetectors were integrated. Shorter diodes (10×21 μm) yielded a poorer responsivity (0.64 A/W) but provided a higher 3dB bandwidth of 48 GHz. The 10×35 μm device provided a 3dB bandwidth of 31 GHz but yielded higher responsivity (0.95 A/W). The produced RF power output of this device is 12 dBm at 40 GHz and the devices have a saturation current-bandwidth product of 1200 mA × GHz. This is the best result of a single PD device integrated on silicon up-to-date.

1.3.3.5 Discussion

As discussed above, III-V photodetectors with very high speed, responsivity and performance were developed for telecommunication and sensing applications. However, the examples of wafer-scale integration of these III-V devices (also including lasers, amplifiers, modulators, etc.) on the Si photonics platform is still limited, as compelling heterogeneous integration technologies for realizing this are still in the development phase. In the next section we will focus on the possible heterogeneous III-V-on-Si integration techniques.

1.4 Heterogeneous III-V-on-Si integration

An important problem of Si photonics is that silicon is an indirect bandgap semiconductor, and therefore efficient lasing in silicon is not possible [14]. Conse-

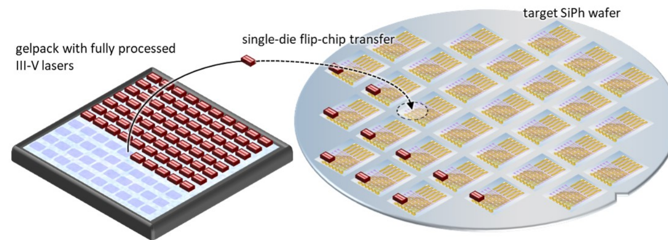


Figure 1.19: Schematics of flip-chip integration technology [67].

quently, there is an extensive attempt to efficiently integrate direct bandgap III-V materials and devices on Si PICs. A number of technological approaches exist to implement III-V-on-Si integration. These range from high-maturity flip-chipping and direct/adhesive bonding techniques to low-maturity epitaxial growth and micro-transfer-printing. We will review these shortly.

1.4.1 Flip-chipping

The best-known technology for integrating semiconductor devices and chips is flip-chipping, a pick-and-place technique. Solder bumps are deposited on the target wafer and/or device to be flip-chipped. Then the prefabricated and pretested chip is flipped, aligned with the solder bumps and brought into contact with the solder. In the final interconnecting step, the solder undergoes reflow to complete the integration [66]. The process is schematically illustrated in Fig. 1.19.

The advantage of this technology is that one can integrate (pre-)fabricated and (pre-)tested devices on the target wafer. The drawback however is that flip-chipping is a sequential operation, therefore the throughput of the technique is limited.

1.4.2 Direct and adhesive bonding

One is particularly interested in a wafer-scale technology allowing the integration of III-V devices on the silicon photonics target substrate. The direct bonding technique can be an interesting technique for this purpose. III-V dies or wafers are flipped upside down and bonded on a fully patterned SOI wafer. The substrate of the III-V wafer is then removed and the bonded III-V wafer is then patterned and etched using III-V processing steps on 200mm or 300mm wafers (Fig 1.20). The integration technique makes use of the Van der Waals forces between the Si and III-V material surfaces to bond two substrates. Therefore utmost

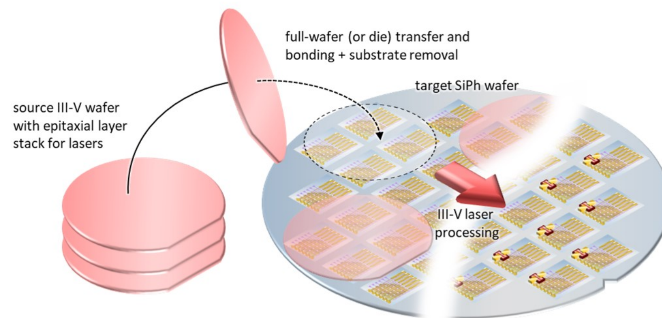


Figure 1.20: Schematics of wafer bonding technology [67].

care has to be taken on the cleanliness and roughness of both surfaces [68] [69] [70]. One can relax the cleanliness and roughness requirements by applying an adhesion enhancing polymer, the most well-known of which is divinylsiloxane-bis-benzocyclobutene (DVS-BCB or simply BCB). Direct and adhesive die-to-wafer/wafer-to-wafer bonding reached a high level of maturity, and many interesting III-V-on-Si devices were demonstrated for telecommunication and sensing applications using the technique [71].

The advantage of the technique is the high-throughput wafer scale integration. The drawback is that the back-end of line processing in the fab becomes compromised and 200/300 mm scales III-V processing needs to be developed.

1.4.3 Direct growth

Direct epitaxial III-V growth on Si can lead to a high cost reduction and fabrication complexity reduction. However, the large lattice constant mismatch (8% between Si/InP) makes it difficult to make efficient III-V devices on silicon, as threading dislocations reduce III-V device performance. Nonetheless, efforts in this direction are ongoing, with recent demonstrations of InP and GaAs lasers epitaxially grown on Si [72], [73].

Direct III-V epitaxial growth represents the ultimate way to integrate light sources on a-Si photonics platform however many difficulties have to be overcome for it to become a mainstream approach.

1.4.4 Micro-transfer-printing

A novel technique for heterogeneously integrating III-V devices on Si is micro-transfer-printing (transfer printing or TP). Materials and devices fabricated in dense

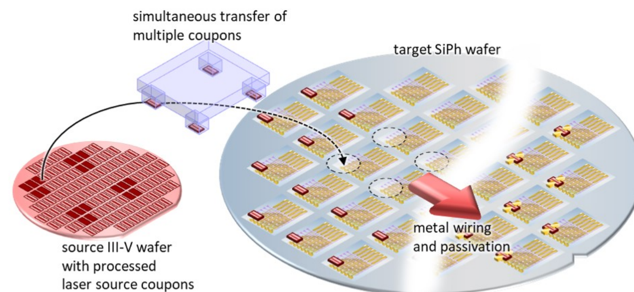


Figure 1.21: Schematic demonstration of transfer printing technology [67].

arrays on the source substrate can be selectively picked using a polydimethylsiloxane (PDMS) stamp and printed on the target substrate with high alignment accuracy (better than 1.5 μm, 3σ [74]; Fig. 1.21 [67]) . The technique has several advantages, for instance, it enables area magnification, whereby devices densely integrated on a source wafer can be sparsely integrated on the target wafer. The technique offers important merits of cost- and time-effectiveness: one printing cycle can take up to 45 seconds [75], thereby integrating 10s to 1000s of devices. Transfer printing is a versatile technique that can be applied to virtually any thin-film device that can be released from its substrate [76].

1.4.5 Discussion

The technology overview hints that micro-transfer-printing is a compelling approach for the heterogeneous integration of opto-electronic devices on an Si photonics platform. The technology combines the advantages of flip-chip integration (pre-fabricating and pre-testing components on a source) and the wafer bonding technique (massively parallel integration). In comparison to flip-chipping, however, the simultaneous integration of arrays of devices is possible, enabling a high throughput process. In comparison to wafer bonding, the silicon photonic process flow is not disturbed by the integration of the III-V devices, and the III-V processing can be done on the III-V source wafer. Furthermore, micro-transfer-printing is not limited to III-V device integration, but can also be used for the integration of e.g. SiGe photodiodes and other Si-based devices.

1.5 Micro-transfer-printing: main principles

Micro-transfer-printing is a technology whereby (arrays of) prefabricated devices can be selectively picked from a source wafer and transferred to a target wafer,

maintaining a constant pitch. The key to this technology is the use of an elastomeric polydimethylsiloxane (PDMS) rubber stamp, selected for its very high resolution molding capabilities, chemical stability, non-toxicity, low mechanical stiffness (about 1-10 MPa) with a reasonably smooth surface and its viscoelastic properties, enabling a kinetically switchable adhesion to the coupons [77] [78].

This section will discuss this physical effect and propose a general scheme of a transfer-printing-enabling process flow. It will briefly describe the PDMS stamp fabrication process and introduce the uTP-100 transfer printing hardware available in the UGent cleanroom.

1.5.1 Basics of kinetically switched adhesion to the stamp

In order to enable the micro-transfer-printing process, the adhesion of the applied stamp to the surface of the film to be transferred, should be stronger than the adhesion of the film to the source substrate. Typically, the PDMS exhibits surface van der Waals forces with a relatively low surface energy but the force can be high enough to pull the films from the source substrate [79] [80].

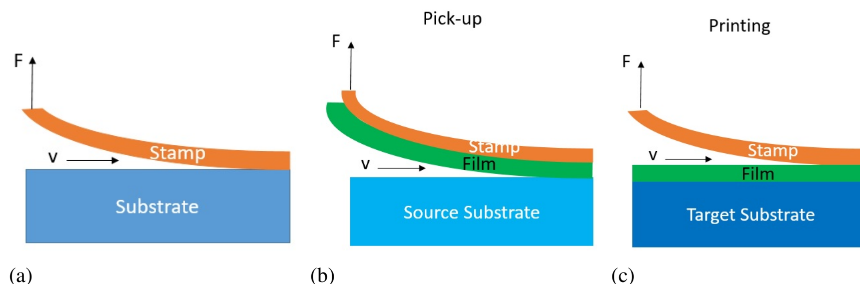


Figure 1.22: Schematics of: (a) PDMS stamp peel; (b) film pick-up; (c) film printing.

Elastomeric PDMS stamp material exhibits a viscoelastic effect - the strength of the adhesion changes significantly with the peeling speed of the PDMS laminated with the film. This is called kinetically switched adhesion: fast separations lead to strong adhesion between the stamp and the device, while slow separations lead to weak adhesion [81].

Figure 1.22 depicts the effects when the PDMS stamp is applied to the substrate [77]. Figure 1.22(a) shows the peel of the stamp, typically quantified by the peeling force F and peeling velocity v. Figure 1.22(b) depicts the peeling of the PDMS stamp together with the film or the so-called pick-up process, while Figure 1.22(c) depicts peeling away the PDMS stamp, leaving only the film attached to the non-native (or target) substrate. This process is called printing.

When the PDMS stamp is peeled vertically it is quantified by a separation energy G, which is dependent on peeling velocity v by

$$G(v) = G_0(1 + (\frac{v}{v_0})^n) \tag{1.7}$$

Here, G_0 is the separation energy in the limit of the slowest delamination speed, v_0 is the reference peeling velocity at which the smallest separation energy becomes $2G_0$ and n is the experimental fitting parameter.

If one considers applying the viscoelastic stamp to the elastic film (Figure 1.22(b) and Figure 1.22(c)), the separation energy is proportional to the peel force F

$$F \sim G \tag{1.8}$$

Separation energy of the film/substrate G_{FS} interface is a fixed number and depends on the material properties. However, for the PDMS/film interface, the parameter depends on the peeling speed ($G_{PDMS}(v)$), therefore an important conclusion can be drawn. The pick-up of the film occurs when the PDMS peeling force exceeds the force of the film/substrate interface.

$$F_{PDMS} > F_{FS} \tag{1.9}$$

Or, from equations 1.7 and 1.8:

$$G_{PDMS}(v) > G_{FS} \tag{1.10}$$

Likewise, the printing will occur when the separation energy of film/substrate interface is larger than the separation energy of the PDMS/film, or when the velocity v is low. In other words, the printing condition is

$$G_{PDMS}(v) < G_{FS} \tag{1.11}$$

The separation energy of the PDMS G_{PDMS} dependency on the peeling velocity v of equation 1.7 is displayed in Figure 1.23. By equating the separation energy of the PDMS to the constant separation energy of the film/substrate interface ($G_{PDMS} = G_{FS}$, or the green line on Figure 1.23) and plugging it into equation 1.7, the critical velocity can be extracted:

$$v_c = v_0(\frac{G_{FC} - G_0}{G_0})^{1/n} \tag{1.12}$$

This implies that in principle for each single material, a critical peeling velocity v_c is present. If it is exceeded by a PDMS peeling speed v, the film attaches to the PDMS stamp and film pick-up occurs. Likewise, printing will occur once the

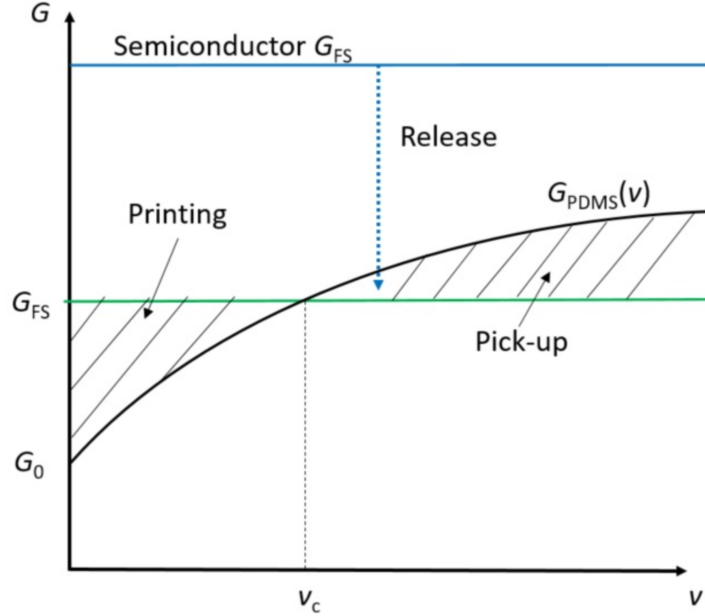


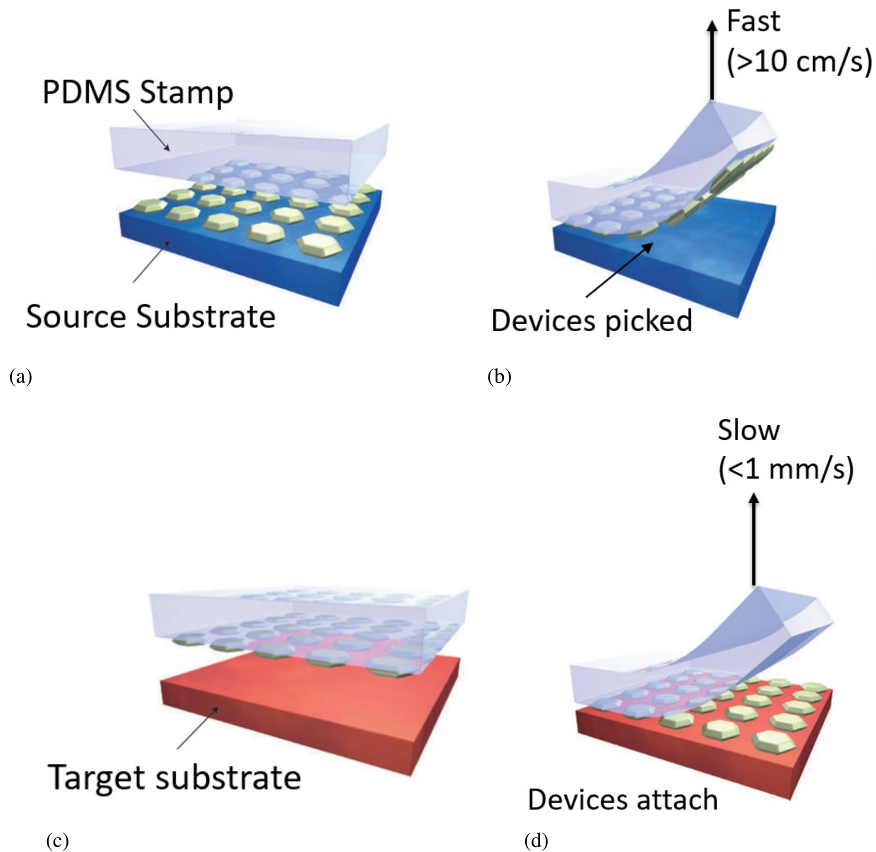
Figure 1.23: Schematics of the separation energy dependencies on the peeling speed. When the peeling speed is lower than the critical speed printing will occur. When it is higher, pick-up will occur. Typically, for inorganic semiconductor devices, the device-substrate separation energies are a lot higher (blue line).

peeling speed v of the PDMS stamp is lower than the critical speed of the specific material interface. This can be rephrased as [81]:

$$v > v_c \text{ - pick-up condition} \tag{1.13}$$

$$v < v_c \text{ - printing condition} \tag{1.14}$$

The micro-transfer-printing process is summarized in Figure 1.24. When the PDMS stamp is applied to a patterned device (or device array - Figure 1.24(a)) and one quickly peels the stamp in the vertical direction, the forces are strong and the device is able to attach to the bottom of the PDMS stamp (Figure 1.24(b)). If the picked device is laminated against the target substrate with the different G_{FS} (Figure 1.24(c)) and one slowly peels the PDMS stamp vertically, the forces between the stamp and the device are weak. Hence, they attach to the target substrate and printing occurs (Figure 1.24(d)) [77] [82] . Similarly, like in the adhesive bonding process, the adhesive (DVS-BCB) can be used on top of the target substrate to enhance the adhesion of the printed coupons [84].



(a) (b) (c) (d)

Figure 1.24: The main concept of the transfer printing process [82].

1.5.2 General flow of micro-transfer-printing process

The scenario described in Figure 1.23 is not entirely straightforward, considering semiconductor materials (Si, Ge, InP, etc.) as their separation energies are situated much higher on the energy scale (the blue line in Figure 1.23). Because of this, any physical peeling speeds of the PDMS will not be enough to pick the device.

Therefore, an important technological process of releasing the devices has to be performed to enable transfer printing of semiconductor devices (weakly) anchoring them to the substrate [84].

The general release process schematic is demonstrated in Figure 1.25. It is critical to choose the correct layer stack with the release layer sandwiched between the device layer and the substrate (Figure 1.25(a)). Afterwards, one patterns the device layer and the release layer (Figure 1.25(b)), and one forms a layer that can anchor the device to the source substrate through tethers (Figure 1.25(c)). The re-

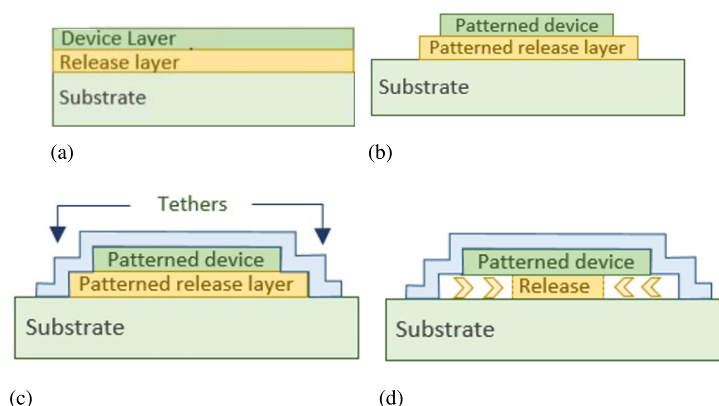


Figure 1.25: Release process schematic [83].

lease layer gets under-etched, making devices free-hanging membranes (coupons) anchored to the substrate by the tethers (Figure 1.25(d)). Once the PDMS stamp comes in contact with the released coupons and quickly moves upwards, the tethers break in the weakest points, enabling it to pick the released coupon.

The key to successful transfer printing is the development of the release process and proper tethering of the coupons. Transfer printing enabling process development is the main focus of this thesis.

1.5.3 The uTP-100 lab scale printer

The uTP-100 is a lab-scale printer system that was used throughout this PhD thesis, manufactured by X-Celeprint Ltd [86]. The system consists of three building blocks, as shown in Figure 1.26: an electrical cabinet, a user interface and a transfer printing machine [85].

The electrical cabinet is the main processing unit and contains the main alternating current (AC) power supply of the printer, a CPU, temperature controller and the vacuum.

The schematics of the transfer printing machine are displayed in Figure 1.27. The source and target substrates are mounted on the sample vacuum chucks next to each other. The third mount at the rear (not visible in Figure 1.27) is the cleaning pad for the PDMS stamp (double-sided scotch tape).

The top part of the transfer printing machine is the head, which has a camera + objective on top (with available 5× and 10× magnification lenses) and the PDMS on-glass mount, which is placed upside down and fixed by the vacuum chuck. In this work we used bulk PDMS with the bottom 3 mm post(s). The camera and the complete head can independently move in Z-direction.

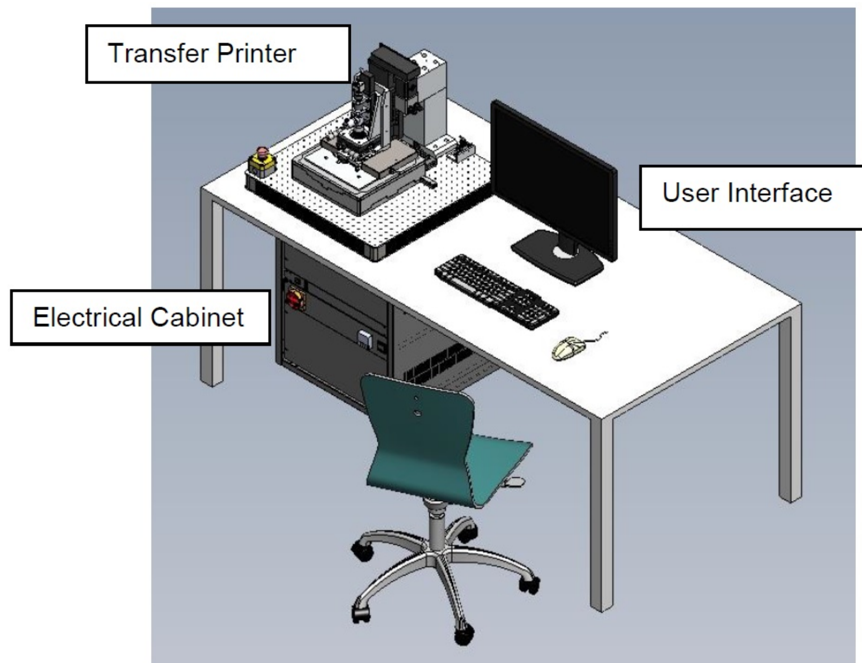


Figure 1.26: The uTP-100 system [85].

The transfer printing proceeds as follows: the user fixes the prepared source and target substrates onto the sample chucks, then mounts the PDMS stamp onto the glass plate, flips the plate and fixes it onto the vacuum chuck on the bottom of the head. The user can independently control the camera movement, the focus and the head movement in Z-direction, as well as the movement of the sample stage in X and Y. The user can manually navigate the stamp to the desired positions of the source wafer, target wafer and the cleaning pad and perform picking, printing and cleaning operations by laminating the stamp against the surface of the source, target and cleaning pad respectively. Automated transfer printing mode is available as well [87].

The uTP-100 lab-scale printer can work with 3-inch wafer-scale substrates and other wafer-scale tools are commercially available. However, all experiments described in this PhD thesis were carried out on small centimeter-sized samples.

1.6 Scope of the thesis

This PhD thesis focuses on the development of micro-transfer-printing technology. We applied it to the printing of passive optical structures and high-speed SiGe and

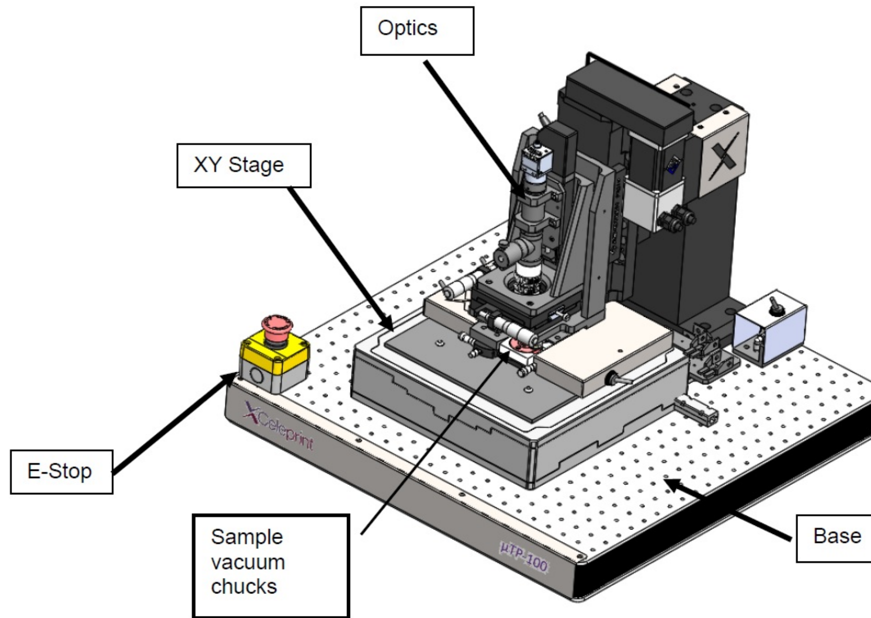


Figure 1.27: Schematics of the transfer printing machine [85].

III-V photodiodes. This thesis comprises four chapters.

Chapter 2 describes the work on micro-transfer-printing silicon passive waveguide structures and silicon-germanium devices. The chapter deals with alignment-tolerant coupling structure simulations, design, key aspects of the tether development and the development of the release processes, as well as device fabrication and characterization.

Chapter 3 describes the work on micro-transfer-printing III-V grating-assisted photodetectors. We start by focusing on the fabrication of a large array of InP/InGaAs photodetectors. The second part of the chapter deals with micro-transfer-printing of grating-assisted III-V photodetectors on a silicon photonic IC for a wavelength division multiplexed receiver. We describe the design, fabrication and characterization of single polarization and polarization diversity 4-channel receivers. We finish the chapter discussing important findings of process development of III-V waveguide-coupled photodetectors.

In chapter 4, we present the conclusions and the main findings of this PhD work. We conclude the thesis with a short discussion on the future work.

1.7 List of publications

This PhD thesis led to a number of publications in peer-reviewed international journals as well as international conferences. An overview of the publications is provided below.

1.7.1 International peer reviewed journal papers

1. N. Ye, **G. Muliuk**, J. Zhang, S. Uvin, D. Van Thourhout, G. Roelkens, A. J. Trindade, C. Bower, *High-Alignment-Accuracy Transfer Printing of Passive Silicon Waveguide Structures* , Optics Express, 26(2), p.2023-2032 (2018).
2. N. Ye, **G. Muliuk**, J. Zhang, A. Abbasi, D. Van Thourhout, G. Roelkens, A. J. Trindade, C. Bower, *Transfer Print Integration of Waveguide-Coupled Germanium Photodiodes onto Silicon Photonics ICs*, IEEE Journal of Lightwave Technology **(invited)**, 36(5), p.1249-1254 (2018).
3. **G. Muliuk**, K. Van Gasse, J. Van Kerrebrouck, A. J. Trindade, B. Corbett, D. Van Thourhout, G. Roelkens, *4× 25 Gbit/s polarisation diversity silicon photonics receiver with transfer printed III-V photodiodes*, IEEE Photonics Technology Letters, 31(4), p.287-290 (2019).
4. J. Zhang, **G. Muliuk**, J. Juvert, S. Kumari, B. Haq, C. Op de Beeck, B. Kuyken, G. Morthier, D. Van Thourhout, R. Baets, G. Lepage, P. Verheyen, J. Van Campenhout, A. Gocalinska, J. O'Callaghan, E. Pelucchi, B. Corbett, A. J. Trindade, G. Roelkens *III-V-on-Si Photonic integrated circuits realized using micro-transfer-printing*, publication in APL Photonics, **(invited)**, (to be published).

1.7.2 International conference proceedings

1. **G. Muliuk**, N. Ye, S. Uvin, G. Roelkens, D. Van Thourhout, *Transfer Printing of Silicon-on-Insulator Devices on Silicon Nitride Waveguide Circuits: Design of Coupling Structures and Process Development*, Proceedings Symposium IEEE Photonics Society Benelux, Belgium, p.4 (2016).
2. **G. Muliuk**, N. Ye, J. Zhang, A. Abbasi, D. Van Thourhout, G. Roelkens, *Transfer Print Integration of 40 Gbps Germanium Photodiodes onto Silicon Photonic ICs*, European Conference on Optical Communication, Sweden, p.PDP.C.4 (2017).
3. **G. Muliuk**, N. Ye, D. Van Thourhout, G. Roelkens, *High Alignment Accuracy Transfer Printing of Silicon Coupons for Heterogeneously Integrated PICs*, Proceedings Symposium IEEE Photonics Society Benelux, Netherlands, p.48-51 (2017).

4. **G. Muliuk**, K. Van Gasse, M. Shahin, J. Verbist, A. J. Trindade, B. Corbett, D. Van Thourhout, G. Roelkens, *4 × 25 Gbit/s Silicon Photonics Tunable Receiver using Transfer Printed III-V Photodiodes*, IEEE Photonics Conference, TuA1.2, United States, p.169 - 170 (2018).

5. G. Roelkens, J. Zhang, A. De Groote, J. Juvert, N. Ye, S. Kumari, J. Goyvaerts, **G. Muliuk**, S. Uvin, G. Chen, B. Haq, B. Snyder, J. Van Campenhout, D. Van Thourhout, A. Trindade, *Transfer printing for silicon photonics transceivers and interposers*, IEEE Optical Interconnects Conference (OI) 2018 (invited), United States, p.13-14 (2018).

6. G. Roelkens, J. Zhang, **G. Muliuk**, J. Goyvaerts, B. Haq, C. Op de Beeck, A. Liles, Z. Wang, S. Dhoore, S. Kumari, J. Juvert, J. Van Campenhout, B. Kuyken, D. Van Thourhout, B. Corbett, *III-V/Si PICs based on micro-transfer printing*, (**invited**) *Optical Fiber Communication Conference*, United States, W4E.6 (2019) .

7. G. Roelkens, J. Zhang, S. Kumari, J. Juvert, A. Liles, **G. Muliuk**, J. Goyvaerts, B. Haq, N. Mahmoud, D. Van Thourhout, *Transfer printing for heterogeneous silicon PICs, Smart Systems Integrations*, Spain, p.48-49 (2019).

8. **G. Muliuk**, J. Zhang, J. Goyvaerts, S. Kumari, B. Corbett, D. Van Thourhout, G. Roelkens, *High-yield parallel transfer print integration of III-V substrate-illuminated C-band photodiodes on silicon photonic integrated circuits*, SPIE Photonics West 2019, Volume 10923, Silicon Photonics XIV; 1092305 United States (2019).

9. F. Pavanello, **G. Muliuk**, G. Roelkens, *Highly efficient grating couplers in transfer-printing technology, European Conference on Integrated Optics*, p.T.Po.2.13, Belgium (2019).

10. J. Zhang, S. Kumari, S. Dhoore, **G. Muliuk**, M. Galarza, G. Agnieszka, P. Emanuele, C. Brian, G. Roelkens, *Micro-transfer-printed III-V-on-silicon C-band Distributed Bragg Reflector Laser*, IEEE International Conference on Group IV Photonics (To be published).

11. J. Zhang, **G. Muliuk**, J. Goyvaerts, B. Haq, A. Liles, S. Kumari, J. Juvert, C. Op de Beeck, B. Kuyken, J. Van Campenhout, G. Lepage, P. Verheyen, A. Gocalinkska, E. Pelucchi, B. Corbett, *Heterogeneous integration in silicon photonics through micro-transfer-printing*, Micro-Optics Conference **(invited)** (To be published).

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2

Micro-Transfer-Printing Silicon-on-Insulator Devices

2.1 Introduction

After we discussed the important concepts of micro-transfer-printing, this chapter develops the process flow for releasing and transfer printing SOI devices; more specifically the silicon-germanium photodetector (SiGe PD) from the imec iSIPP25G full platform. The number of processing steps for a full silicon photonics platform run typically is huge, resulting in a slow turnaround time for a new device generation (typically $\sim$8 months). This hampers the swift development of new products on this platform. Transfer printing can be an effective solution to this problem.

However, the important problem of finding proper optical interfaces has to be resolved before this can be explored, as transfer printing has an alignment accuracy of about ± 1 μm.

Thus the chapter is therefore subdivided into three parts. The first part discusses the simulation, design, post-processing, and transfer printing of passive alignment-tolerant silicon optical interfaces. This information will be applied in the second part, which deals with the design, fabrication, transfer printing, post-processing and characterization of the iSIPP25G SiGe photodetector. We present static and dynamic measurement results on transfer printed SiGe PDs.

In the last part we discuss simulation results, process development and micro-transfer-printing of highly-efficient grating couplers, released on a Si(111) substrate.

This work has been done in a collaboration with Nan Ye who carried out the process development work of the SOI devices described in this chapter. The author carried out the work of numerical simulations, transfer printing and characterization. The work on highly-efficient grating couplers has been done in collaboration with Fabio Pavanello, who contributed numerical simulation results and grating coupler designs. The author contributed with process development, release, transfer printing, and characterization.

2.2 Alignment-tolerant coupling structures

The goal of this work is depicted in Figure 2.1. We aim to release and transfer print a SiGe PD device (or coupon; see Figures 2.1(a) and (b)), with access waveguide structure on top of a target silicon photonic waveguide. This means that when the optical mode is launched in the bottom silicon waveguide, it has to couple to the waveguide of the transfer printed coupon (see Figure 2.1(c)).

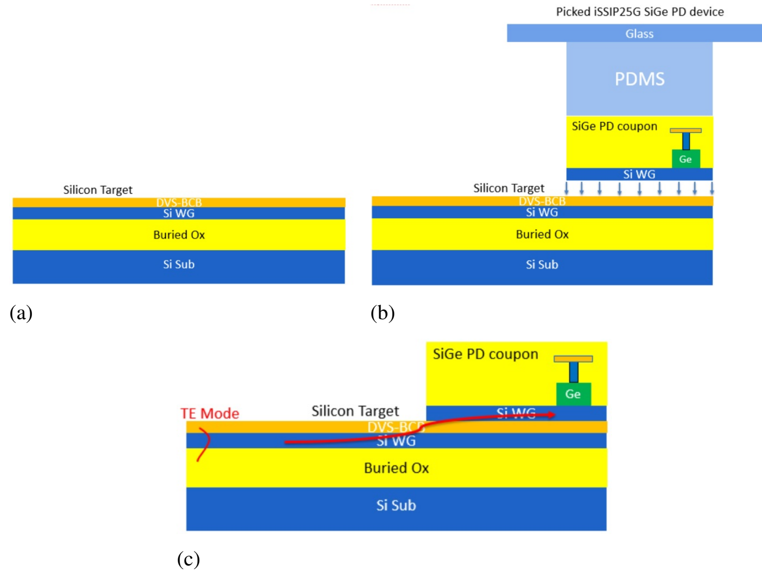


Figure 2.1: Envisioned integration scheme. On top of the silicon photonic target substrate, with the spin-coated DVS-BCB (a), we aim to transfer print an iSIPP25G SiGe PD device (b), with an alignment-tolerant coupling structure, so that the light can efficiently couple to the transfer-printed coupon (c).

2.2.1 The main requirements

The main goal is to design a Si-to-Si coupling interface with the following requirements.

Alignment tolerance. The coupling structure has to demonstrate efficient TE fundamental mode coupling efficiency >80% at a misalignment of ± 1 μm.

Broadband operation. The coupling structure has to show efficient operation over the telecom wavelength bands 1310 nm $\pm$ 50 nm or/and 1550 nm $\pm$ 50 nm.

Compact. The coupling structure has to be as short as possible.

2.2.2 Adiabatic taper design

One approach is to use an adiabatic taper design. When the fundamental mode is tightly confined within the linearly narrowing waveguide on the target wafer, and a waveguide on the printed coupon is placed in close proximity, the power can efficiently couple to the second waveguide, as long as phase-matching is obtained along the taper structure [1] [2].

We propose two waveguide cross-sections, as shown in Figure 2.2. The waveguide on the target wafer is a 220 nm full-etched standard waveguide (Figure 2.2(a)). The waveguides on the source wafer will undergo the HF release etch, therefore we cannot choose the full-etch cladding layers. Therefore, the waveguide on the coupon is a 80 nm etched, 150 nm thick Si waveguide, with top-oxide (Figure 2.2(b)). We sweep the waveguide widths (w_1 and w_2 respectively) to find the optimal width at which the effective indices (n_{eff}) match.

Simulations performed using eigenmode calculations, and their results are displayed in Figure 2.3. We choose λ = 1.3 μm, TE polarization and the result reveals that by choosing w_1 = 0.5 μm and $w_2 > 3$ μm the phase-matching condition holds.

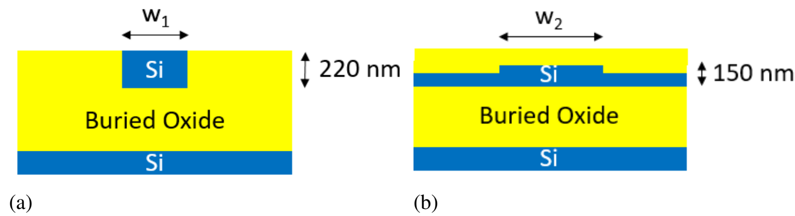


Figure 2.2: Two waveguide cross-sections. (a) the target wafer cross-section, (b) the source wafer cross-section.

A structure with a two-step transition is proposed and displayed in Figure 2.4.

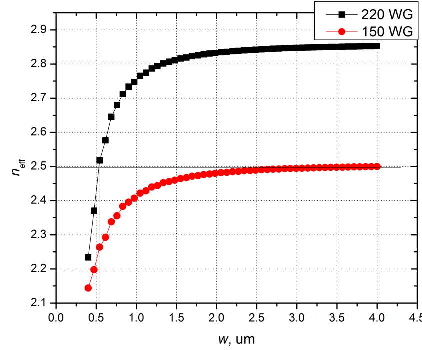


Figure 2.3: Effective index dependencies on the width of waveguides using λ = 1.3 μm, TE polarization.

The first transition consists of coupling the transverse electric (TE) fundamental mode of a 220 nm fully etched input waveguide on the target wafer to a 150 nm thick, 80 nm etched waveguide on the printed device coupon. The silicon waveguide on the target wafer tapers from 800 nm to 150 nm width over a length of x, while the waveguide on the silicon coupon tapers from 150 nm width to a width w_2 over a length of 25 μm. The second transition occurs in the printed coupon from a 150 nm thick and 80 nm etched silicon waveguide to a 220 nm thick and 150 nm etched silicon waveguide. The simulation was performed using finite domain time difference (FDTD) software, where the taper length x and the target waveguide w_2 were swept while misaligning the taper in the the y-direction. For these simulations, we assumed the BCB thickness to be 200 nm and a wavelength of 1.31 μm (TE polarization).

The results are displayed in Figure 2.5. By increasing the taper length x, the coupling efficiency increases at maximum ± 1 μm misalignment: by changing x from 100 to 300 μm, the coupling efficiency increases from 50% to 75%. The coupling efficiency can be increased even further by decreasing the BCB height from 200 nm to 100 nm.

Another important parameter is the waveguide width w_2 of the target wafer. Choosing x = 200 μm and BCB height of 200 nm, the adiabatic taper structure with a waveguide width w_2 of 4 μm, can achieve $>$ 80% coupling efficiency at ± 1 μm misalignment.

Choosing x = 200 μm and w_2 = 4 μm, bandwidth simulations (Figure 2.5(c)) reveal that the adiabatic taper structure is optically broadband and efficiently covers O- and C-bands in aligned and misaligned cases ($>$70% TE fundamental mode coupling).

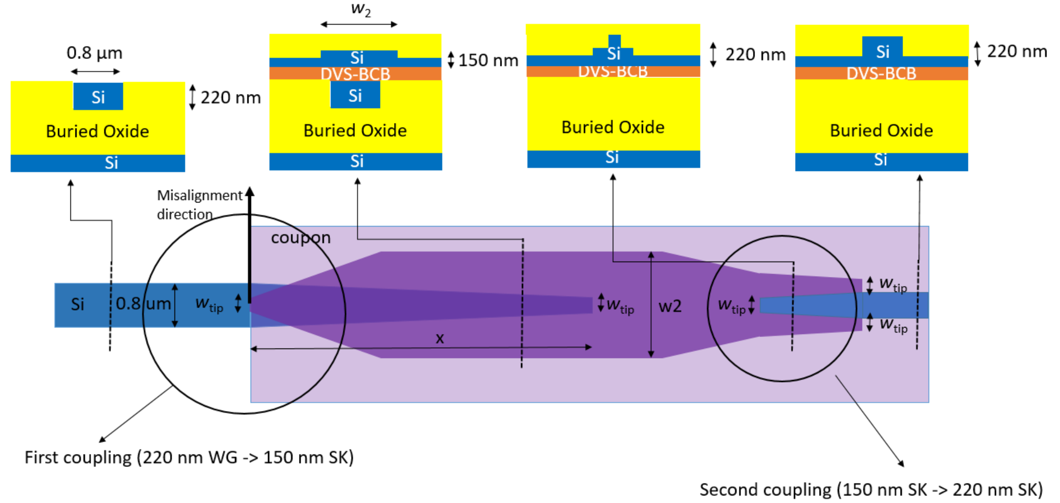


Figure 2.4: Simulated adiabatic taper coupling scheme.

The second transition transforms a 150 nm thick and 80 nm etched silicon waveguide into a 220 nm thick and 150 nm etched silicon waveguide (right-hand side of Figure 2.4). By choosing a taper length of 35 μm and a taper tip of 150 nm, 99% coupling efficiency is simulated.

Care has to be taken when designing the 150 nm waveguide ending tips (denoted as w_{tip} in Figure 2.4) because minimal design size requirements must be satisfied [3]. Therefore, the smallest dimension designed was w_{min} = 150 nm.

2.2.3 Directional coupler design

A vertical directional coupler structure can also be considered for a Si-to-Si coupling scheme. Two identical waveguides, placed vertically and in close proximity, can result in a complete optical power exchange between the two waveguides [4]. This can be implemented by using two identical 220 nm thick and 150 nm etched silicon waveguides, the schematics of which are depicted in Figure 2.6. In this case, the vertical directional coupler is implemented in waveguides with a width w that is substantially wider than a single mode waveguide, in order to improve the misalignment tolerance. A parabolic taper structure with the length L_{PAR} can then be used to transition to a single mode 220 nm thick and 150 nm etched waveguide on both the target and the coupon.

First, we found the optimal length L, at which power exchange is the most efficient. The directional coupler structures were analyzed using eigenmode expansion simulations. The simulation assumes a 150 nm thick DVS-BCB layer.

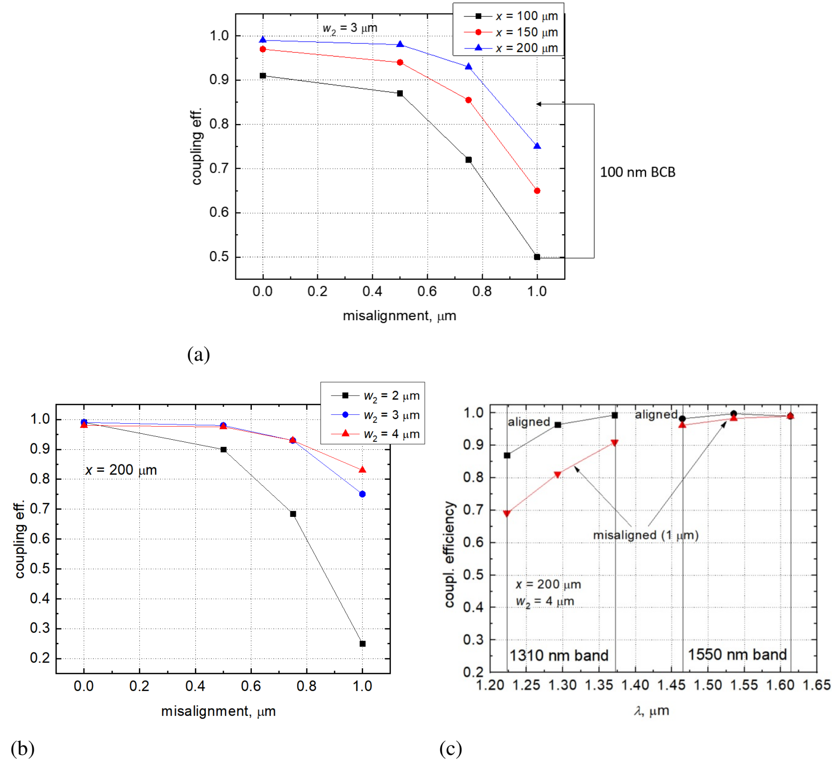


Figure 2.5: Simulation results of the adiabatic taper coupling transition. (a) TE (λ = 1.31 μm) fundamental mode coupling efficiency dependencies on misalignment in lateral direction (y-), (b) TE (λ = 1.31 μm) fundamental mode coupling efficiency dependencies on misalignment, in y-direction and sweeping over the waveguide width (w_2). (c) Bandwidth simulation comparing aligned and misaligned structures, choosing the length x = 200μm and width w_2 = 3μm.

The results are displayed in Figure 2.7, which reveals that the directional coupler operation is wavelength dependent and the optimal coupling at λ = 1310 nm is at L = 12 μm and for λ = 1550 nm it is at L = 20 μm (Figure 2.7(a)).

Next, we simulated the effect of misaligning the directional coupler in lateral (y-) and longitudinal (x-) directions on the coupling efficiency. In the case of a directional coupler structure, using a 5 μm wide waveguide allows around 80% coupling efficiency at $\pm$0.7 μm misalignment (Figure 2.7(b)). $\pm$1 μm longitudinal misalignment has no substantial impact on the coupling efficiency for the directional coupler (Figure 2.7(c)). A parabolic taper length of L_{PAR} = 100 μm can achieve efficient coupling to the wide waveguide sections (Figure 2.6).

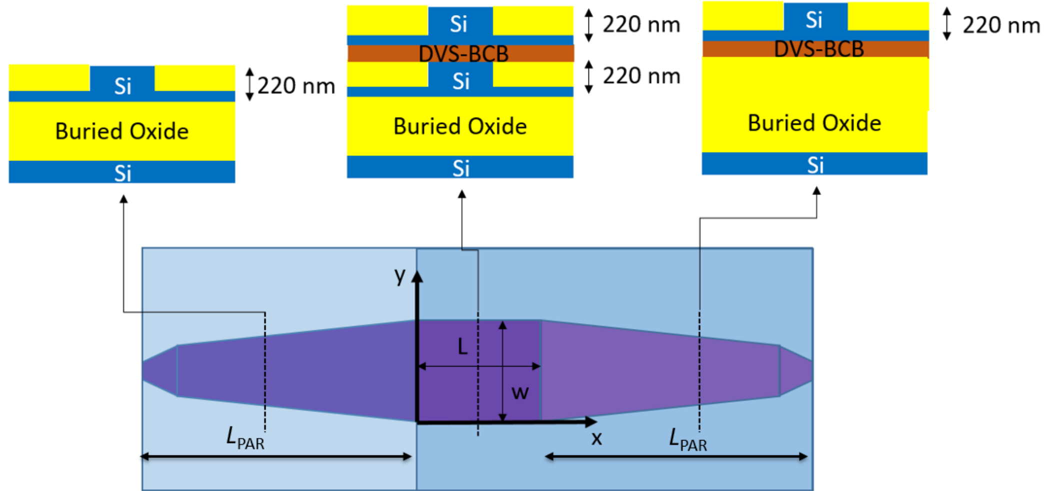


Figure 2.6: Simulated vertical directional coupler coupling scheme.

2.2.4 Trident taper

Good misalignment tolerance could be obtained using a trident taper structure, a schematic example of which is depicted in Figure 2.8(a). The alignment simulation results are depicted in Figure 2.8(b). this demonstrates that the coupling efficiency is steady at ~-0.4 dB (89%), with the misalignment of the coupon from 0 to ±1 μm.

More information on a similar coupling scheme can be found here [5]. More details on the design is described here [6].

2.3 Mask layout

Silicon device coupons and target waveguide structures were designed on imec's passive 220 nm silicon photonics platform, comprising a full (220 nm), shallow (70 nm), and socket etch (150 nm) [3].

The complete mask layout can be found in Figure 2.9. This mask was designed for releasing and printing adiabatic tapers and directional coupler structures. Adiabatic taper coupling structures (marked 4 on Figure 2.9) and directional coupling structures (5) were designed with two couplers per coupon and a loop. They are shown in closer detail in Figures 2.10(c) and (d). We designed adiabatic tapers with sweeps of the coupling lengths (100 μm, 200 μm and 300 μm) and widths (2 μm, 3 μm and 4 μm), as well as directional coupler structures for C-band (L = 20 μm) and O-band (L = 12 μm), which we swept over the waveguide width (2 μm,

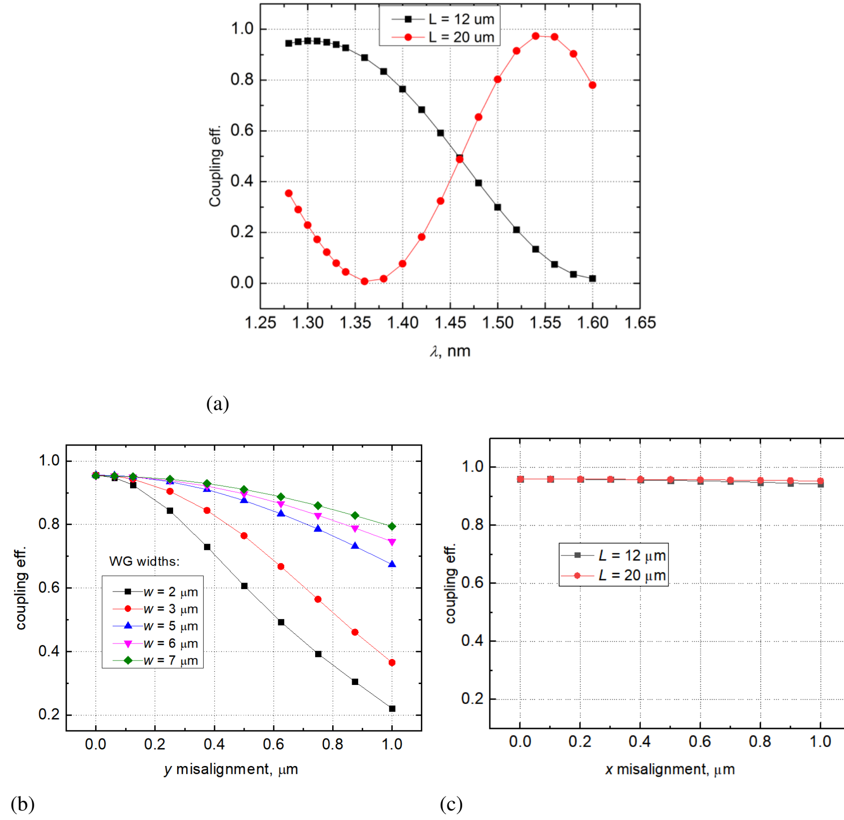
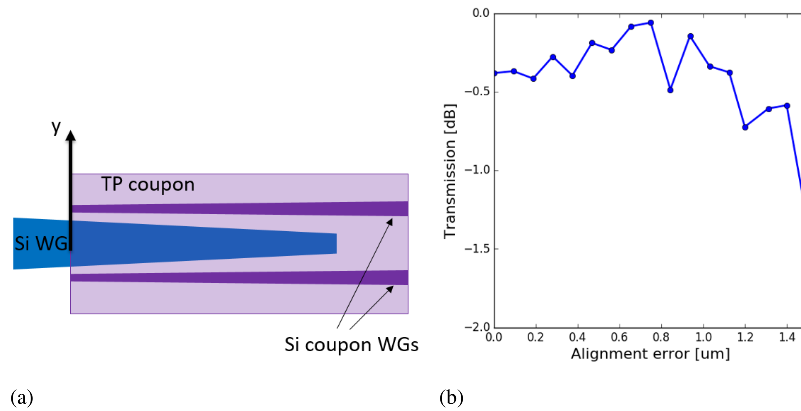


Figure 2.7: Simulation results for the directional coupler structure. (a) bandwidth simulations choosing L = 12 μm and L = 20 μm coupling lengths, (b) coupling efficiency dependencies on misalignment in y-direction sweeping the waveguide widths, (c) coupling dependencies on misalignment in x-direction.

3 μm, and 4 μm). The source wafer was ordered with top-oxide cladding.

Separate dies were ordered, with side oxide cladding to be used as the target chip. Figure 2.9 also includes silicon photonic target waveguide structures. We designed target structures to print the adiabatic taper structures (marked as 1 in Figure 2.9) for printing one (1b), two (1a), and four (1c) devices in one loop. Likewise, the chip can accommodate directional coupler coupons for printing one (2a) and two (2b) loops. A detailed view of the target structures is shown in Figure 2.10(a) and (b) and the design of the target chips also contains waveguide couplers for printing the iSIPP25G SiGe photodetectors (3).

Using two grating couplers on the silicon target chip (Figures 2.10 (a) and (b)), the light can be coupled in and out of the silicon device coupon to extract



(a) (b)

Figure 2.8: Trident taper conceptual schematics and the alignment tolerance simulations.

the coupling losses. To achieve high alignment accuracy during transfer printing, it is crucial to add transfer printing alignment markers to both the silicon device coupon (rectangles) and the target waveguide structure (Tetris brick markers). Device coupons were enclosed in a non-tiling area (red background on the source coupons; Figures 2.10(c) and (d)) so that in the release process steps, the devices can be released without attacking the top oxide. Tethers are defined in a separate contact lithography process.

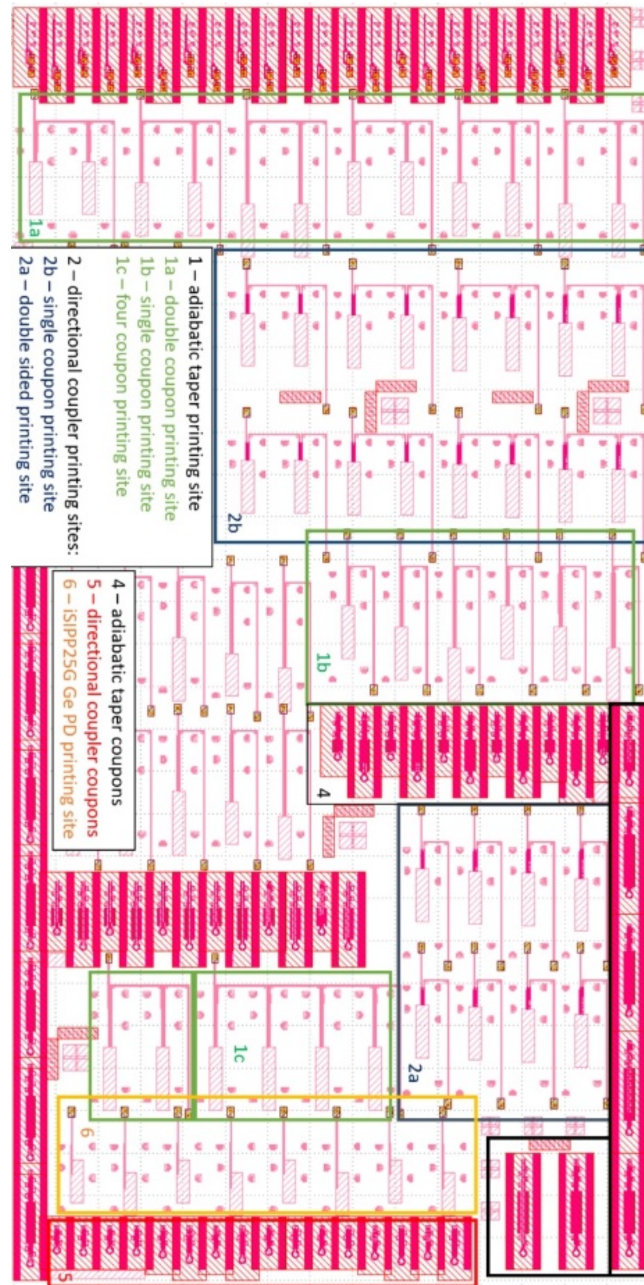


Figure 2.9: Full mask layout accommodating adiabatic tapers and directional coupler coupons, as well as landing sites for the adiabatic tapers, directional couplers, and germanium photodiodes.

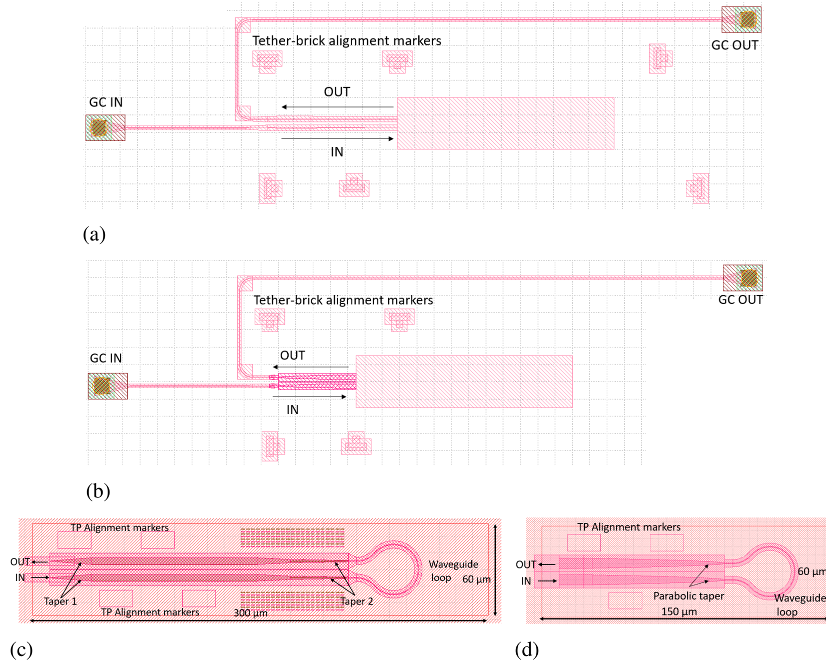


Figure 2.10: Schematics of the coupons and the target sites. (a) Schematic of the adiabatic taper target site. (b) Schematic of the directional coupler landing site. (c) Schematic of the adiabatic taper coupon. (d) Schematic of the directional coupler coupon.

2.4 Process development

The envisioned process flow for device release is depicted in Figure 2.11. Here, we aim to make silicon devices transfer-printing-compatible by accessing and underetching the buried oxide layer, using a hydrofluoric acid (HF) solution. We aim to anchor the silicon suspended membranes sideways using Si tethers. We identify the important points of the process development.

Top layer protection. The top oxide layer needs to be protected from the aggressive HF chemical (Figure 2.11(b)) used to etch the buried SiO_x layer. Removing the top oxide layer is not an option because a) the silicon 220 nm coupon will become a very thin film, what makes it fragile and subject to deformation when releasing, and, b) in the case of an iSIPP25G device, the top oxide is an integral part of the device (back-end stack). Therefore, it is of paramount importance to find a material that is resistant to HF, with a good adhesion to silicon oxide/nitride dielectrics, and which has relatively easy handling abilities (such as deposition and

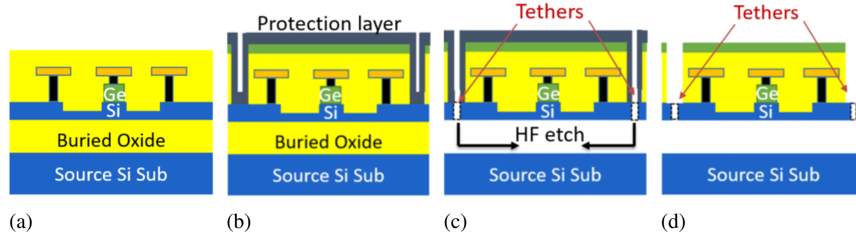


Figure 2.11: Envisioned SOI device release scheme. (a) SiGe PD cross-section. (b) Deposition of a-Si protection layer, (c) patterning tethers and HF release. (d) Removal of top protection material on released suspended devices.

removal) in a cleanroom environment.

Release. The release etch should be a well-controlled process. We plan to use hyrdofluoric acid (HF) solution (Figure 2.11(c)), as it has good selectivity when etching the buried oxide, compared to Si. Therefore, the Si device layer can act as a protective layer during the release in order to prevent HF penetration into the top oxide layers.

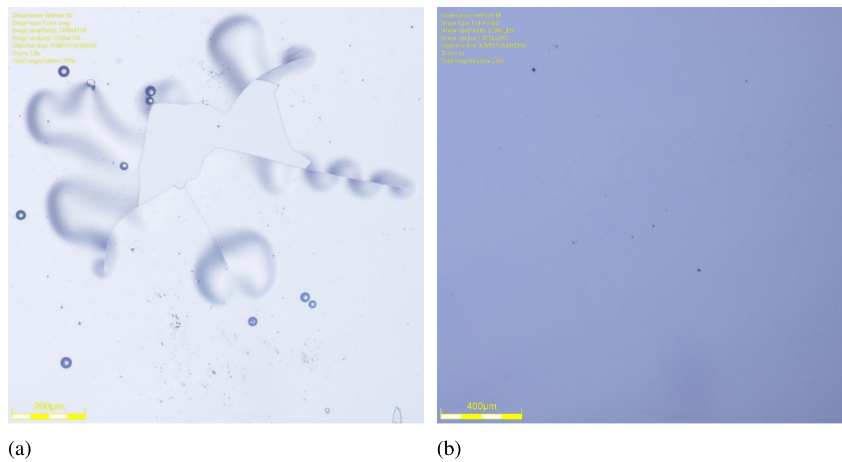
Tethers. Once the device is released, it should remain anchored to the wafer using tether structures (Figure 2.11(d)). This is a crucial development, as tethers should be strong enough to hold the released silicon device in place and cleanly break in the correct place during the device pick-up using the PDMS stamp, without creating any additional debris.

Stress management. When devices are released on the source, the top dielectric layers can induce a lot of stress. This can bend devices, causing them to collapse onto the substrate. Therefore, stress management is an important concern of this work.

2.4.1 Amorphous silicon protection layer

Amorphous silicon (a-Si) is a material that can be deposited using plasma-enhanced chemical vapor deposition (PECVD). It is resistant to HF and yields a good adhesion to the dielectric films. Using reactive ion etching (RIE), it is also fairly easy to remove.

To assess the material quality (in terms of being pinhole-free), we took a blank silicon substrate and deposited 100 nm of silicon oxide (SiO_x) and an additional layer of a-Si. On one substrate $\simeq$1 μm of a-Si was deposited at 200°C and on another $\simeq$1 μm at 180°C. Both substrates were dipped in buffered hydrofluoric acid (7% HF or BHF) for about 1 hour.



(a) (b)

Figure 2.12: Effect of BHF exposure of the SiO_x/a-Si layer stack. (a) a-Si deposited at 200°C clearly indicating a broken top layer, with the presence of pinholes, (b) deposition at 180°C demonstrates a pinhole-free surface.

The surfaces of these substrates are depicted in Figure 2.12. a-Si deposited at 200°C yields a lot of pinholes and cracks (Figure 2.12(a)), which causes the BHF to enter inside and damage the SiO_x layer underneath. The a-Si deposited at 180°C shows a clean surface and no evident damage to the SiO_x layer. This difference between 200°C and 180°C a-Si deposition quality currently is not understood.

To validate the experiment further, we prepared the same Si substrate with the same material stack but this time the SiO_x was patterned (Figure 2.13(a)) and the a-Si was deposited at 180°C (Figure 2.13(b)). After keeping this stack in BHF for 1 hour, inspecting the surface revealed that there were no pinholes, damage, or other evidence of the HF chemical penetrating into the SiO_x area.

The removal of the a-Si layer was done using RIE (SF_6:CF_4:H_2 gas mixture) for $\sim$19 minutes. a-Si has been fully removed from the substrate (Figure 2.13(c)). The color variations indicate the non-planar plasma etching of the substrate. This effect must be considered.

It is clear that, when deposited at 180°C, a-Si can effectively protect the top dielectric layers and it is an easy layer to remove. Over-etching must be handled carefully however because, in order to fully remove the A-Si layer, the top dielectric layer needs to be over-etched.

2.4.2 Releasing SOI devices using HF

Under-etching tests were performed on a standard SOI substrate that comprised of a Si substrate, a 2-micrometer buried oxide layer, and a 220 nm Si device layer.

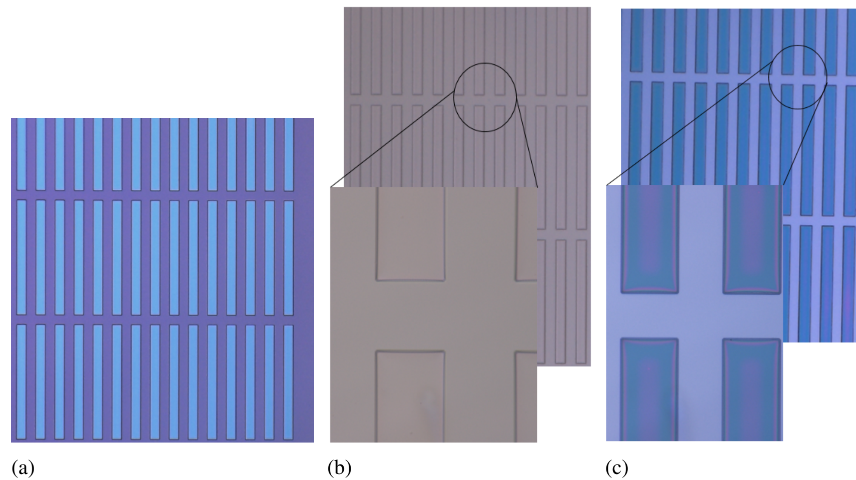


Figure 2.13: (a) Si substrate with the patterned SiO_x coupons, (b) a-Si deposited, (c) a-Si removed after keeping the substrate in BHF for 1 hour.

Top device layer was patterned and etched in order to expose the buried oxide layer, as depicted in Figure 2.14(a). The blank silicon devices were attached to the substrate using c-Si tethers as shown in Figure 2.14

The initial plan was to under-etch the devices using a BHF solution, however, to fully release the 60 μm wide coupons it takes more than an hour. Therefore, to accelerate the process a 40% HF solution was used.

After 2 minutes of etching in the HF and drying with isopropyl alcohol (IPA) revealed that the HF etches the buried oxide isotropically. Monitoring the HF penetration into the side region (barrier) one can control the under-etch of the coupon. Since etching for 2 minutes was not enough, another wafer was kept in the HF for an additional 1 minute (Figure 2.14(c)). Keeping the same wafer in the HF long enough (10 minutes) will fully etch the barrier and the top silicon device layer will collapse onto the substrate (Figure 2.14(d)).

Switching from blank SOI test devices to imec's passives/iSIPP25G devices, we noticed that one needs about 13 minutes in order to fully release the 60μm wide devices in the 40% HF solution. The origin of this difference is not fully understood.

2.4.3 SOI tether system

Devices released on the source become thin membranes that are suspended on the substrate and that are kept in place by structures called tethers. These have to be strong enough to keep the fragile released devices attached to the substrate but also

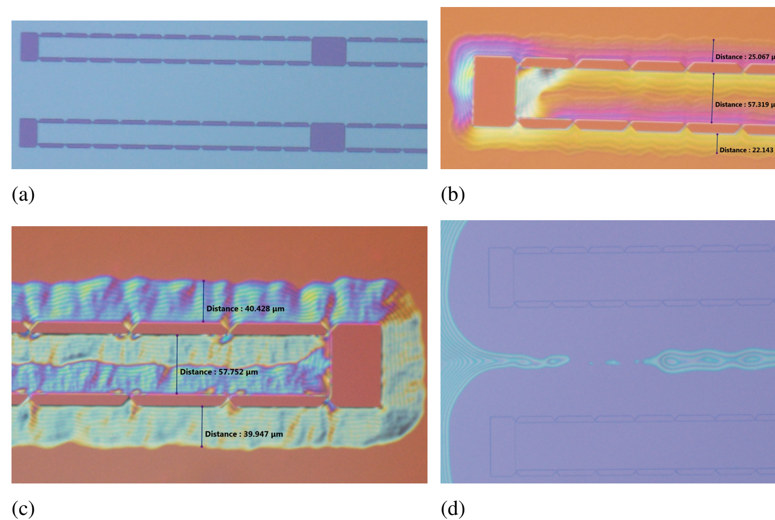


Figure 2.14: HF etching of the buried oxide. (a) the initial patterned Si device layer with the tethers and exposed buried oxide, (b) 2 min of 40% HF etching (dark mode image), (c) 3 min of 40% HF etching (dark mode image), (d) 10 minutes of 40% HF etching.

they should cleanly and properly break in the weakest point, when the devices are picked up.

A mask with different tether structures was designed, where we also swept over the tether width and tether spacing. SOI devices were released using HF. Many of the tethers were not strong enough to support the devices on the source, after release (right-hand side of Figure 2.15(a)). Furthermore, many didn't break cleanly during pick-up as part of the barrier was picked and printed together with the coupon (Figure 2.15(b)).

Triangular Si tethers were found to work the most efficiently; Figure 2.15(c) shows that triangular tethers break cleanly in the narrowest point. The printed device contains no debris or residues from the barrier.

However, the width of the narrowest points must be carefully controlled: the optimal width is about 1.2 - 1.5 micrometers and the tether spacing is around 75 - 100 μm (Figure 2.16). When the tether width is below 1 μm, the tethers are too weak to hold the coupons suspended and thus collapse on the silicon substrate. Conversely, when the tether width exceeds 2 μm, the coupon attachment to its surroundings is too strong and it becomes difficult to pick the coupons using the PDMS stamp without taking up part of the barrier.

Fracturing at the narrowest points of the triangular tethers is attributed to being the point where the highest value of stress of the suspended film is located during device pick-up [7] [8].

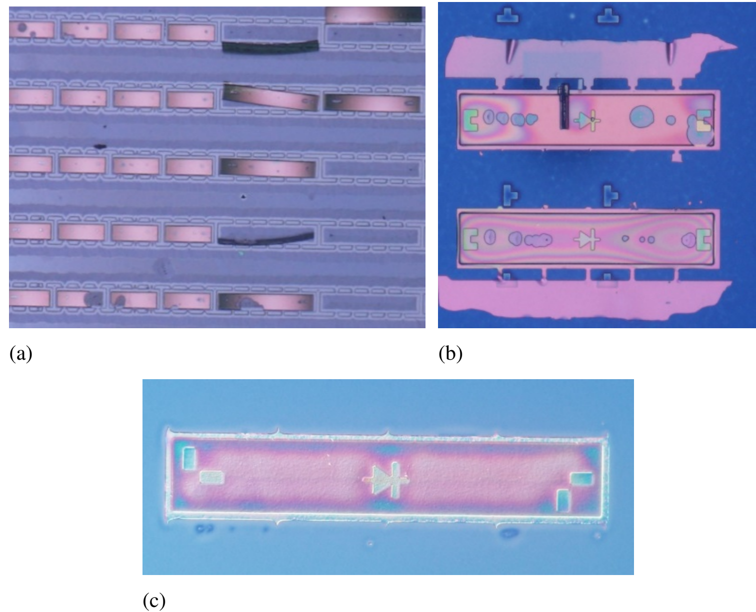


Figure 2.15: (a) Example of strong vs. weak tethers, (b) coupons printed on the Si substrate with improperly broken tethers, c) the coupon printed on the Si substrate with correctly broken tethers.

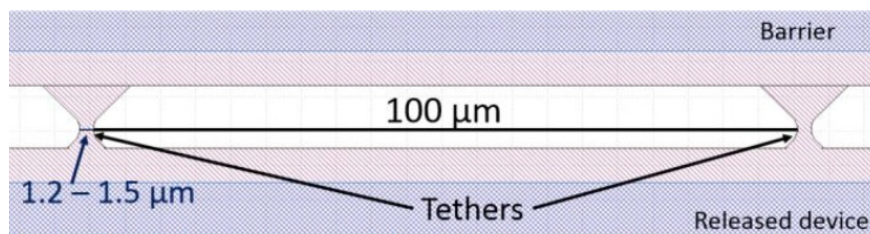
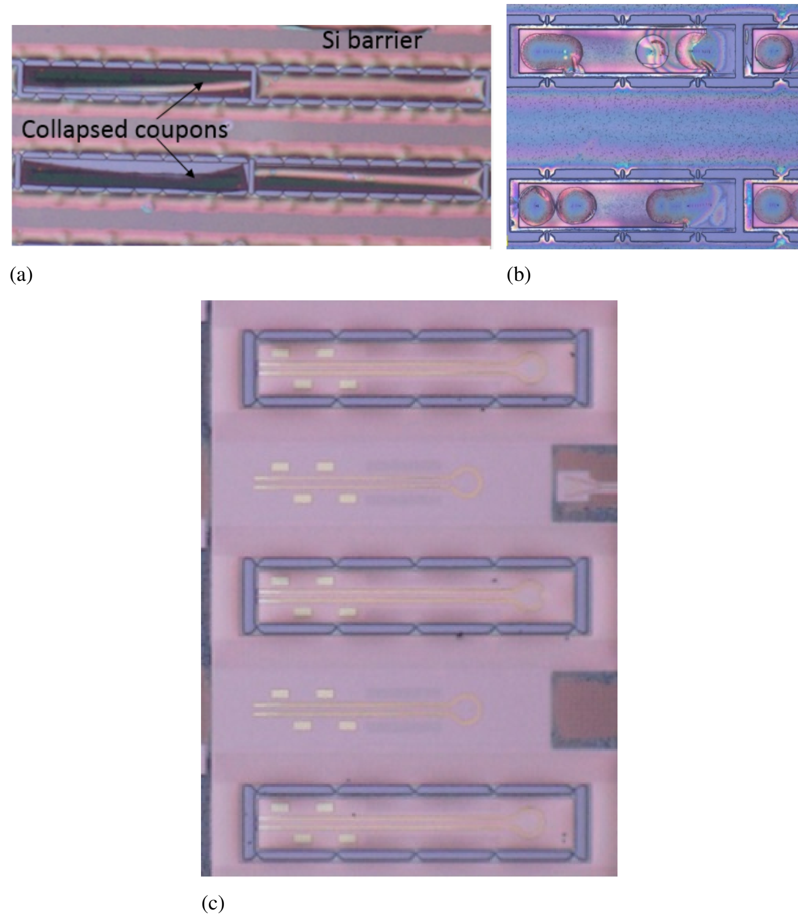


Figure 2.16: Schematic image of the SOI device tether structures.

2.4.4 Stress management

When under-etching the Si devices stress management is of utmost importance. If released devices contain layers with stress, this can cause bending of the coupons, which can, in effect, cause devices to collapse onto the substrate (Figure 2.17(a)) or cause the thin silicon device layers to crack, causing the penetration of HF into the top oxide layer (Figure 2.17(b)).

The stress was measured using the DEKTAK stylus profiler [9]. We first scan the surface curvature of a blank silicon substrate and use it as a reference. Then on the same silicon wafer we deposit a layer of the desired film with a known



(a) (b) (c)

Figure 2.17: Impact of stress on released devices. (a) bending of devices and collapsing onto the substrate, (b) bending causes the bottom Si layer to crack, which allows HF to penetrate the top layers, (c) released devices with the stress compensating layers.

thickness and measure the curvature of the wafer on the same coordinates. The software of the DEKTAK can extract the value of the stress in the film.

This way the stress in the top oxide cladding layer was measured as 153 MPa compressive, while the stress in the a-Si encapsulation was measured as 20 MPa compressive. The films total stress can be calculated as [10]:

$$\sigma_{total} d_{total} = \sigma_1 d_1 + \sigma_2 d_2 \tag{2.1}$$

In order to compensate for the compressive stress, a material with tensile stress can be deposited on top of the film. We found that PECVD mixed-frequency

silicon nitride (MF-SiN$_x$) yields tensile stress (170 MPa). Therefore, the total stress in the stack is:

$$\sigma_{total} = \frac{\sigma_{SiO_x} d_{SiO_x} + \sigma_{SiN_x} d_{SiN_x} + \sigma_{a-Si} d_{a-Si}}{d_{SiO_x} + d_{SiN_x} + d_{a-Si}} \quad (2.2)$$

Before the a-Si removal and

$$\sigma = \frac{\sigma_{SiO_x} d_{SiO_x} + \sigma_{SiN_x} d_{SiN_x}}{d_{SiO_x} + d_{SiN_x}} \quad (2.3)$$

After the a-Si removal.

Thinning the top silicon oxide layer to 100 nm and depositing 90 nm tensile MF-SiN$_x$ allows for proper release of the device.

The comparison of released coupons without and with proper stress management (by optimizing the deposition conditions of the back-end layers) is shown in Figure 2.17, after the removal of the amorphous silicon encapsulation. Figure 2.17(c) demonstrates that using top stress compensation layers greatly reduces device bending.

2.4.5 Final process flow

With all major problems resolved, we now present the final process flow in Figure 2.18. Devices were fabricated on a standard silicon-on-insulator (SOI) substrate, with 1.1 μm top oxide cladding (Figure 2.18(a)). We started by thinning the top oxide to 100 nm using BHF (Figure 2.18(b)). 170 nm thick MF-SiN$_x$ is deposited (slightly thicker than necessary, to offer over-etching tolerance in the following wet and dry etching steps) (Figure 2.18(c)). Rectangular coupons are defined by dry RIE etching (SF_6:CF_4:H_2) the dielectric back-end, and slightly etching the 220 nm silicon device layer (Figure 2.18(d)). Then, 1 μm of the a-Si protection layer is deposited at 180°C (Figure 2.18(e)), which is then patterned. Tethers are defined using dry etching, thereby also exposing the buried oxide (Figure 2.18(f)). By dipping structures in 40% HF for around 13 minutes, the buried oxide is removed underneath the membrane, rendering the passive silicon devices free-hanging and attached to the surrounding silicon by the tethers (Figure 2.18(g)). Finally, the encapsulating a-Si is removed using dry etching, slightly over-etching the top MF-SiN$_x$ layer (Figure 2.18(h)).

2.5 Micro-transfer-printing passive optical devices

The released passive silicon devices now become thin, suspended membranes that are attached to the substrate by tethers. However, before we proceed to the transfer printing, the alignment accuracy of micro-transfer-printing technology has to be

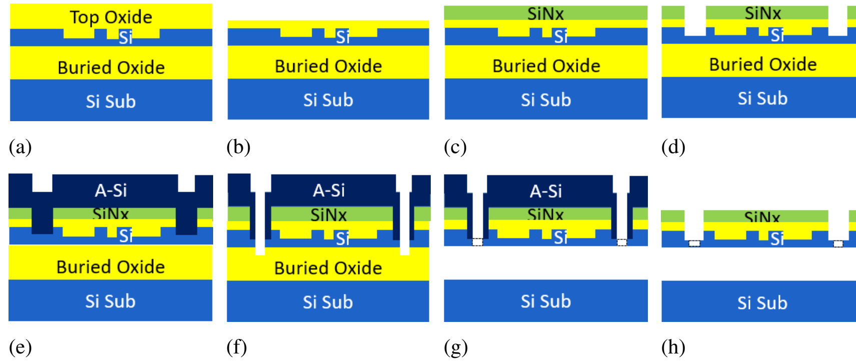


Figure 2.18: Schematics of passive SOI devices release process flow.

thoroughly investigated, as the passive optical interfaces were designed to operate at misalignment that is better than ± 1 μm.

2.5.1 COGNEX^{TM} pattern recognition pattern

The alignment is performed using COGNEX^{TM} pattern recognition software [11], which works by bringing the picked device in close proximity of the target wafer printing position. The software can be trained to scan for the alignment features on the picked device, as well as on the target substrate. It can also be taught auto-alignment by locating the geometric centers of both features and aligning them with each other (a so-called center-to-center alignment) or by seting a certain distance between them (called off-center printing).

We will investigate this further by fabricating, releasing, and transfer printing some of the test structures using the COGNEX^{TM} pattern recognition software.

2.5.1.1 Experiment

We fabricated dummy devices on a silicon-on-insulator (SOI) substrate (220 nm silicon device layer, 2 μm buried oxide layer thickness), following the process flow schematic that is depicted in Figure 2.19. The first step is to deposit 500 nm a-Si: we use this material as it induces no stress and easily withstands the HF etch (PECVD at 180°C, Figure 2.19(b)). The a-Si is patterned to define the size of the silicon coupon that will be transfer printed (300 $\times$ 60 μm, Figure 2.19(c)). In the second step, the buried oxide is locally exposed, and the transfer-printing alignment markers are defined on top of the coupon (Figure 2.19(d)). Immersing these structures in BHF for about an hour releases the coupons, rendering the thin silicon membranes free-hanging and supported by Si tether structures (Figure 2.19(e)).

As described in section 1.5, using the X-Celeprint uTP100 lab-scale printer resulted in the released coupons being transfer printed. Laminating a structured viscoelastic PDMS stamp to the suspended coupon and quickly moving it in a vertical direction enables the triangular silicon tethers to break and hence pick up the released coupon (Figure 2.19(f)). Printing is performed by laminating the picked coupon against a 50 nm DVS-BCB-coated (soft cured at 180°C) SOI target substrate (Figure 2.19(g)). By slowly moving the stamp away the Si coupon remains attached to the SOI target wafer (Figure 2.19(h)).

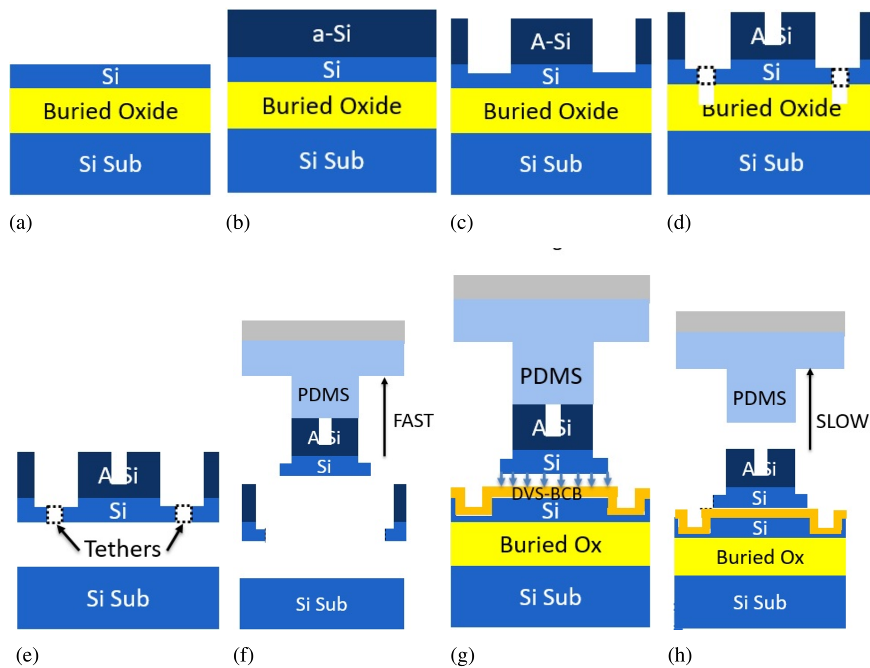


Figure 2.19: Schematics of the process flow to assess the printing alignment accuracy. (a) standard SOI substrate, (b) 500 nm a-Si deposition, (c) coupon patterning, (d) buried oxide exposure and alignment marker formation, (e) release process by under-etching the buried oxide in 40% HF, (f) device pick by pulling back the stamp quickly, (g) transferring a picked device to a target substrate, (h) printing by retracting the stamp slowly.

A schematic of a coupon overlaid on the target wafer is displayed in Figure 2.20. We defined circular transfer printing alignment markers on the coupons. Similarly, Tetris-brick shaped alignment markers were defined on the target substrate. Figure 2.20 demonstrates two alignment methods used by the COGNEX^{TM} image processing software. The left-hand side of Figure 2.20 uses the off-center alignment method, which calculates the center of the pattern of the target markers (the dashed blue line) and the coupon circle marker (purple circle) by defining the

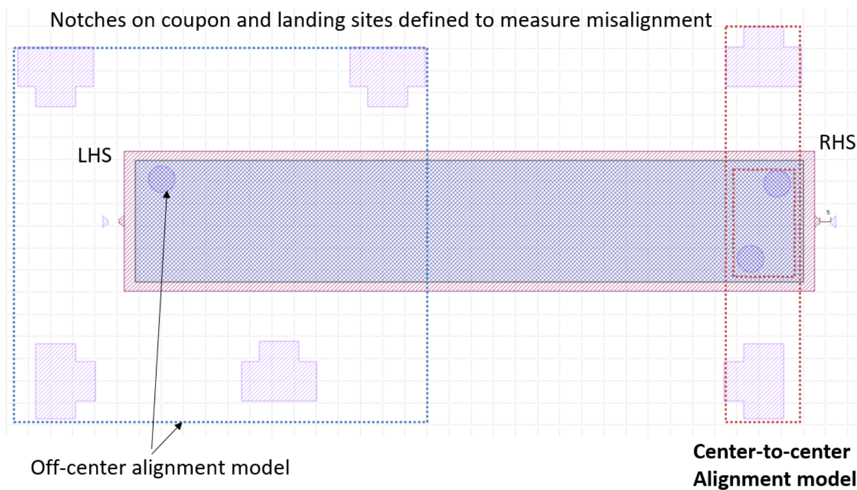


Figure 2.20: Schematics of the coupon overlaid on the target wafer, using the marked off-center alignment approach (left) and center-to-center alignment approach (right).

coordinate difference in the software. On the right-hand side, both of the selected markers have a common geometrical center (center-to-center alignment method). The software can be trained to recognize patterns on the coupon and on the target, allowing an automatic alignment.

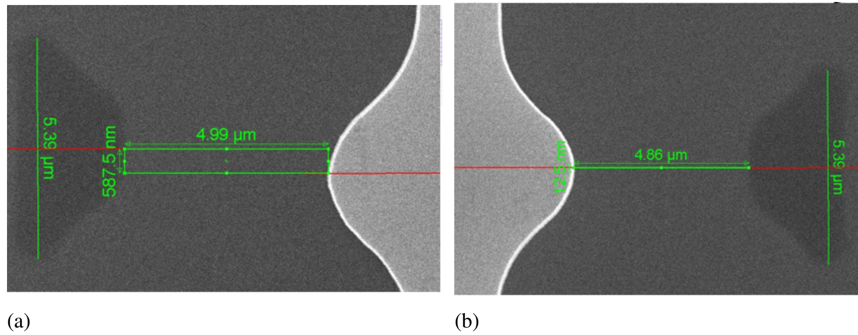
In this experiment we focused only on center-to-center alignment. We designed notches on the silicon coupons and on the target in order to accurately measure the misalignment in x- and y-directions, using scanning electron microscopy. The notches on the landing sites were designed to be 5 μm away from the same notches on the printed devices, in the x-direction, both on the left- and right-hand side (see 2.20).

2.5.1.2 Quantitative assessment of alignment accuracy

We printed 15 devices using only the center-to-center alignment method (the right hand side marker system in Figure 2.20) and then assessed the misalignment on the left- and right-hand side using the scanning electron microscope (SEM), an example of which is shown in Figure 2.21.

The final result is displayed in Figure 2.22, after collecting all misalignment values. The red points on the graph depict misalignment measured on the right-hand side of all coupons. Most of the measured points are within a $\pm$ 500 nm misalignment window in x and y.

However, the left-hand side measurement results show significantly higher misalignment values, particularly in y. This is an indication of a rotational mis-



(a) (b)

Figure 2.21: Example of the transfer-printing alignment measurement on the left-hand-side and the right-hand-side, using scanning electron microscopy.

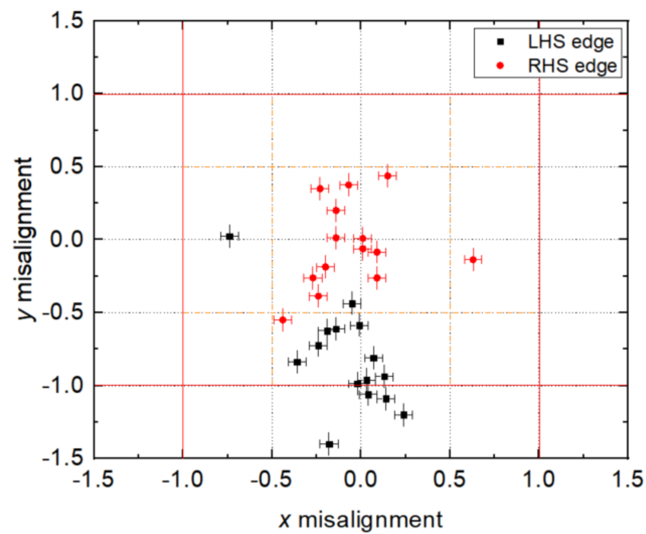


Figure 2.22: Misalignment measurement results for left- and right-hand side.

alignment, which should be tackled by better aligning the orientation of the source and target wafer on the tool.

For our purposes, however, the light only couples from one side and the results are sufficient to continue with transfer printing the released passive devices.

2.5.2 Micro-transfer-printing and post-processing of alignment-tolerant optical structures

The process sequence of transfer printing passive devices is shown in Figure 2.23. By laminating a structured viscoelastic PDMS stamp, with the same dimensions as the device coupons to the suspended silicon coupon (300 μm $\times$ 50 μm for the adiabatic taper coupons and 150 μm $\times$ 50 μm for directional coupler coupons) and quickly moving it in a vertical direction, the silicon tethers are able to break at their narrowest points, allowing to pick up the released coupon (Figure 2.23(a)). Printing is performed by laminating the picked coupon against a DVS-BCB-coated SOI target substrate (soft cured at 180°C) (Figure 2.23(b)). By slowly moving the stamp up, the coupon remains attached to the SOI target wafer (Figure 2.23(c)). In the only post-processing step, the DVS-BCB is cured at 280°C.

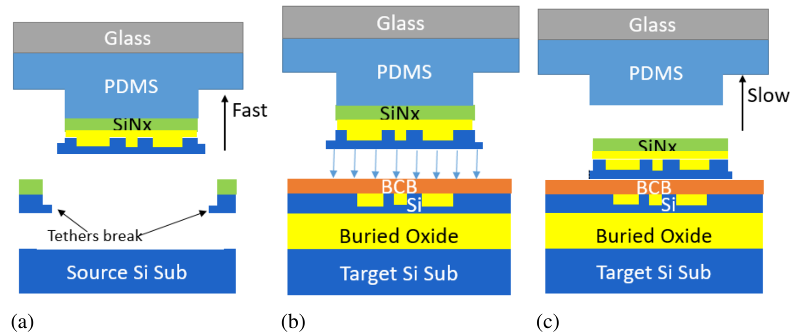
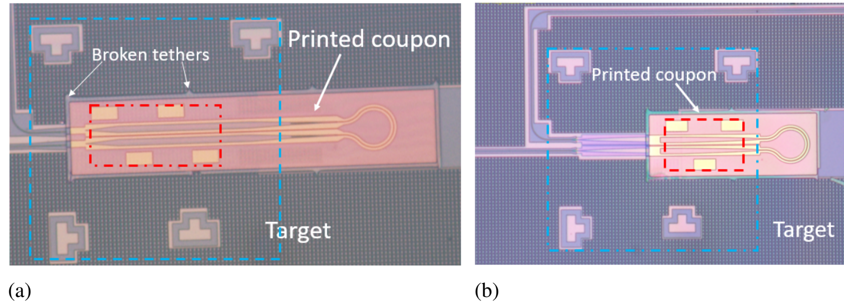


Figure 2.23: Schematic representation of the transfer printing of optical passive devices.

Even though many different devices were defined on the mask (demonstrated in Figure 2.9), we managed to transfer print only two silicon coupons with passive optical coupling structures: the adiabatic taper structure (4 μm taper width and 100 μm taper length) for 1310 nm operation (Figure 2.24((a)) and the directional coupler structure (6 μm directional coupler width) that operates at 1600 nm (Figure 2.24((b)). The tethers that broke during the pick process can be identified here. Clean prints, with no contamination on the target substrate, are obtained. We used markers on the target wafer (the blue dashed rectangle in Figure 2.24) and markers on the coupon (the red dashed rectangle in Figure 2.24) for off-center alignment.

2.5.3 Measurement results

Transmission measurements were carried out by using a pair of single-mode optical fibers connected to the grating couplers on the target waveguide circuit. The measurement schematics are displayed in Figure 2.25. A HP8153A power meter and a Santec TSL-510 O-band or C-Band tunable laser enabled measurement



(a) (b)

Figure 2.24: Transfer-printed coupons on the target waveguide circuit: (a) adiabatic taper coupon, (b) directional coupler coupon. The blue dashed rectangle indicates transfer-printing alignment markers on the target wafer, while the red dashed rectangle indicates transfer-printing alignment markers on the source.

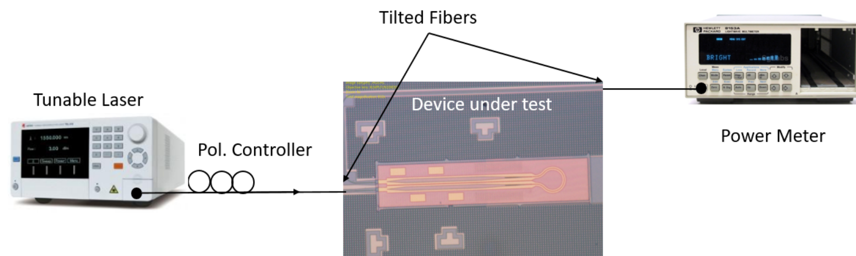


Figure 2.25: Transmission measurement schematics.

of the transmission of both types of coupons. Reference structures on the target waveguide circuit were used to calibrate grating coupler losses. The extracted coupling efficiency for a single adiabatic taper interface is displayed in Figure 2.26(a). Coupling losses below 3 dB are obtained in the complete 1300 nm wavelength range, with a - 1.5 $\pm$ - 0.5 dB coupling loss at 1310 nm.

The coupling loss for the directional coupler structure is depicted in Figure 2.26(b), which reveals that a peak transmission at 1600 nm was obtained, with a coupling loss of 0.5 $\pm$ 0.5 dB per coupler. Using a focused ion beam (FIB), we evaluated the cross-section of the directional coupler interface, which is displayed in Figure 2.27. From this figure, we measured a DVS-BCB thickness of 140 nm and a lateral printing misalignment of 700 nm. We corrected the simulation results by inputting the measured FIB results, which is represented by the red curve in Figure 2.26(b). The coupling efficiency spectrum aligns with the simulation result.

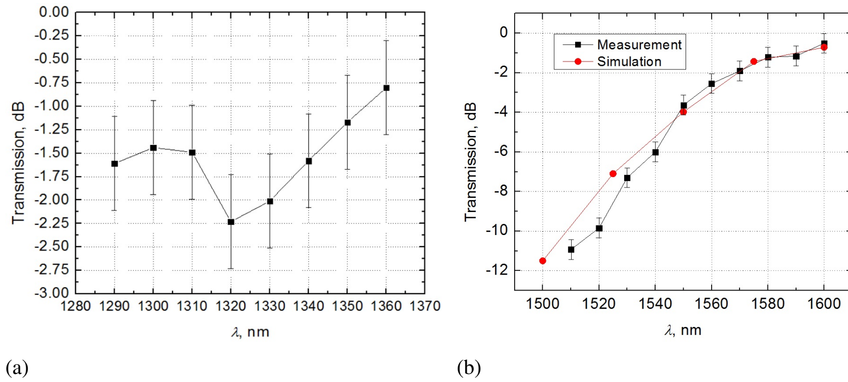


Figure 2.26: Measurement results. (a) Adiabatic taper transmission per one coupler measured in the 1290 - 1360 nm wavelength range. (b) Directional coupler transmission per coupler measured in the 1500 - 1600 nm wavelength range and compared with simulation results.

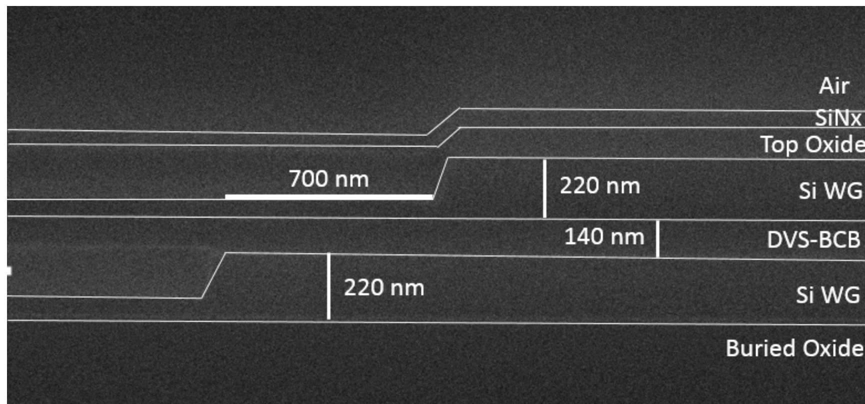


Figure 2.27: Focused ion beam cross-section of transfer printed directional coupler interface.

2.5.4 Conclusions

This is the first time that the transfer printing of passive silicon photonic devices on a silicon photonic target waveguide substrate has been demonstrated. We designed compact alignment tolerant coupling schemes (an adiabatic taper and a directional coupler structure) that can efficiently operate at $\pm$ 1 μm misalignment in the 1310 nm and 1600 nm wavelength range, respectively. A coupon release scheme was developed by under-etching the buried oxide layer, while the top device layers were protected through the use of amorphous silicon. By using an optimized tether design, clean device picking and printing are both demonstrated. The coupling loss

of a single interface was - 1.5 $\pm$ 0.5 dB for the adiabatic taper coupler at 1310 nm and - 0.5 $\pm$ 0.5 dB for the directional coupler at 1600 nm.

2.6 Micro-transfer-printing iSSIP25G SiGe photodetectors

Previous sections of this chapter have addressed important process development issues to release and transfer print SOI passive devices, with high-alignment accuracy. This subsection subsequently utilizes this information, in order to release and transfer print active SOI devices, SiGe photodetectors, on a passive Si photonic circuit. It will discuss the iSIPP25G mask design, release, transfer print, and post-processing steps. This subsection will present static and dynamic measurement results, before it is ended with a conclusion.

2.6.1 iSIPP25G mask layout

Imec offers full-platform Si photonic technology, which includes p- and n-type doping levels, a poly-Si layer, and two layers of metal interconnects. One of the core strengths of the technology is the availability of Ge, which allows users to design and fabricate SiGe electro-absorption modulators and photodetectors. The cross-section of the iSIPP25G stack is displayed in Figure 1.7. The current state-of-the-art imec platform offers modulators that can operate up to 50 Gbit/s (iSIPP50G). The work in this study was conducted using older iSIPP25G technology. More details about this can be found in [12]. The wafers go through a standard CMOS process flow that is described in [13].

The iSIPP25G mask layout is depicted in Figure 2.28. The mask design looks more complex, compared to the passive SOI mask design (which is depicted in Figure 2.9). In this design we added an array of waveguide-coupled SiGe photodiodes, which are depicted with a blue dashed line in Figure 2.28.

Figure 2.29 displays a zoomed microscope image of this photodiode device on the source chip. The coupon size is 310 μm $\times$ 50 μm. No large contact pads are defined in this coupon design, which allows a denser packing of the coupons on the source wafer, as well as an easier release of the coupons. In order to enable high alignment accuracy transfer printing, alignment marker circles were integrated, which aid automatic alignment. High marker contrast is of paramount importance for a good alignment accuracy; hence, two different types of markers were used to evaluate their performance: markers etched 150 nm in the silicon device layer and M1 markers.

The light coupling structure of the SiGe PD is a trident taper, similar to the structure described Figure 2.8 [5]. Not combining the two waveguides of the trident on the silicon coupon, and instead feeding these waveguides to opposite sides

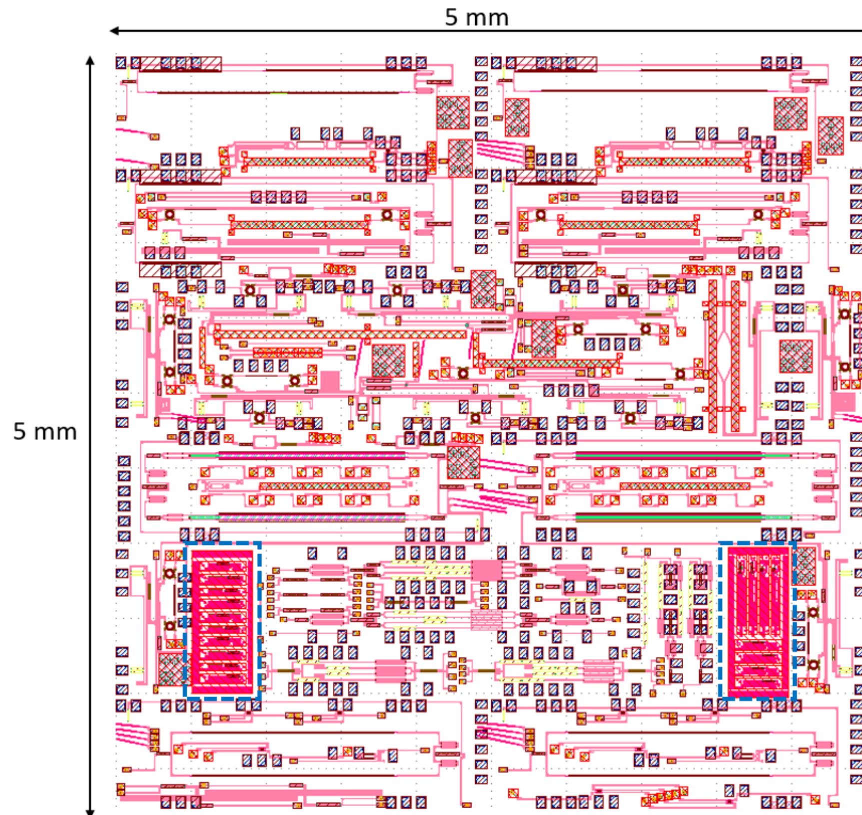


Figure 2.28: Layout of the iSIPP25G design. Blue dashed rectangles indicate the TP-compatible photodiode array.

of the SiGe PD, results in good lateral misalignment tolerance, which is illustrated in Figure 2.8(b).

2.6.2 Releasing iSIPP25G photodetectors

Compared to Figure 2.18, several differences must be considered when releasing iSIPP25G devices. The main difference relates to the back-end layer stack, as it consists of $\sim 2\ \mu$m planarized layers of silicon oxide, silicon nitride, and silicon oxynitride. Therefore, longer etching times are needed to reach the bottom Si layer and to eventually expose the bottom oxide.

The other difference is that using a combination of these layers compensates for the stress in the back-end stack. Therefore, stress compensation is not necessary releasing iSIPP25G devices

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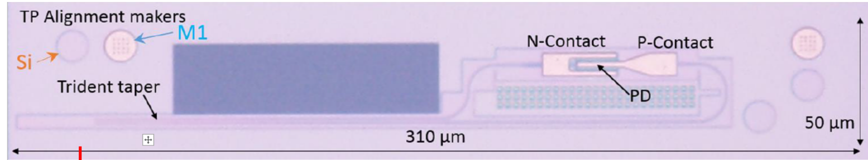


Figure 2.29: Microscope image of germanium photodiode.

2.6.2.1 Final process flow

Figure 2.30 depicts the process flow for the SiGe photodiode release. Onto a standard iSIPP25G chip (Figure 2.30(a)), we deposit a 75 nm thick silicon nitride layer to protect the back-end stack during further processing steps (Figure 2.30(b)). During the initial lithography step, we form 310 μm $\times$ 50 μm coupon mesas by dry-etching the back-end stack down to the silicon device layer, using CF_4:SF_6:H_2. Due to the thick back-end stack and dry-etching non-uniformity, the next step of the process immerses the structures in BHF for 30 seconds, to remove all residual SiO_x in the trenches (Figure 2.30(c)). Next, a 1 micrometer PECVD a-Si protection layer is deposited at 180°C (Figure 2.30(d)), which protects the coupon back-end stack during the buried oxide under-etch. As the bottom side of the coupon consists of a uniform silicon device layer, the device will also be protected from this side during the release etch. A second lithography and dry etch (CF_4:SF_6:H_2) locally exposes the buried oxide and forms the tether structures (Figure 2.30(e)). Immersing the structures in a 40% HF solution for around 13 minutes facilitates under-etching of the buried oxide layer (Figure 2.30(f)), while the coupons are kept in place using the tethers. Finally, dry etching using CF_4:SF_6:H_2 allows for uniform removal of the a-Si layer in the final process step (Figure 2.30(g)), resulting in coupons that are ready for transfer printing.

Figure 2.31 presents the top view image of a released germanium photodiode coupon. Here, the silicon-germanium coupon is now a thin membrane, attached to the surrounding area by triangular tether structures. We picked this device using an X-Celeprint micro-TP100 lab-scale printer (Figure 2.30(h)). Printing is performed by first bringing the SiGe PD coupon within close proximity of the SOI target coupon and using the COGNEX^{TM} image recognition software to align the picked coupon with the target. We used the circular metal markers on the source substrate because, in comparison, to etched Si layer, these markers yield higher contrast for the image recognition. The coupon is printed by laminating the picked coupon on the stamp against a $\sim$50 nm DVS-BCB-coated SOI target substrate (soft cured at 180 ^{o}C) (Figure 2.30(i)), and slowly delaminating the stamp in the vertical direction. The SiGe PD coupon remains attached to the SOI target wafer (Figure 2.30(j)).

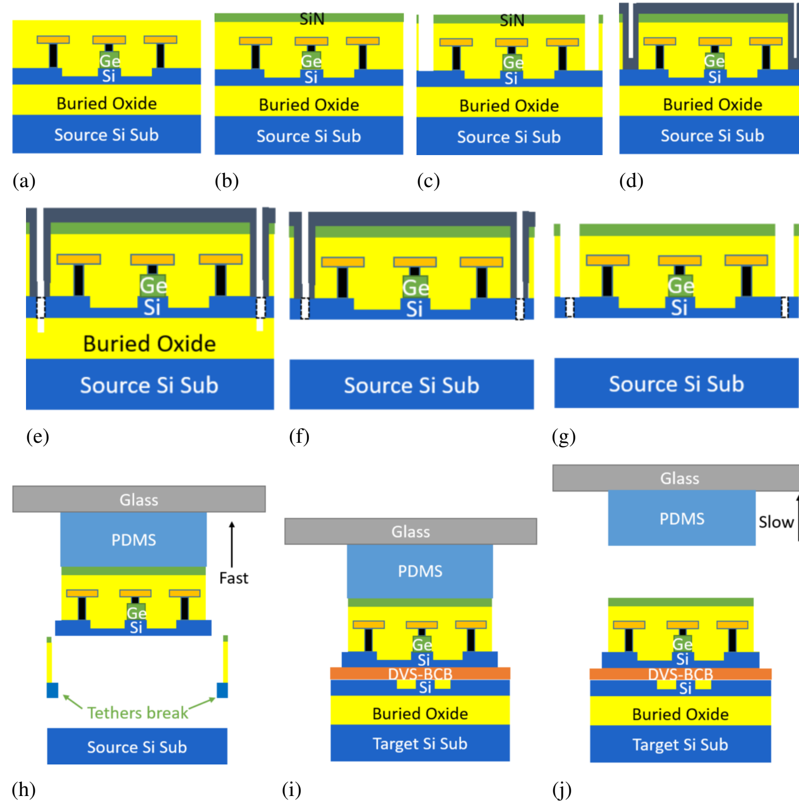


Figure 2.30: Schematics of SiGe photodiode release and transfer printing process.

2.6.3 Post-processing

Post-processing of the transfer-printed active device is depicted in Figure 2.32. We start by spin-coating a thick ($\sim$ 3 micron) DVS-BCB layer on the target substrate and fully curing it at 280°C (Figure 2.32(a)). The purpose of this is to planarize the device, to allow for the metallization of the coupon. The DVS-BCB is then etched back using RIE (SF_6:O_2 plasma; Figure 2.32(b)). Initial lithography and then dry etching (CF_4:SF_6:H_2) open the Cu contacts (Figure 2.32(c)). In a second lithography step, we define 1.2 μm thick Au metal tracks using lift-off. It is important to note that after the window opening, Cu contacts tend to oxidize very quickly. Therefore, before depositing the Au metal pads, the devices were immersed in an acetic acid: H_2O (1:9) solution for about 10 minutes to remove the thin oxide layer on top of the Cu metal contacts [14].

Figure 2.33 depicts the final germanium photodiode coupon transfer printed on the silicon target circuit, consisting of a single mode waveguide connected to

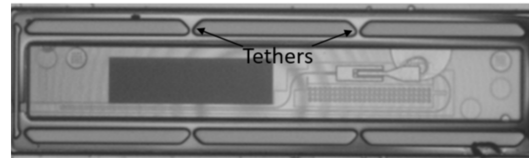


Figure 2.31: Microscope image of a released germanium photodiode coupon.

a grating coupler. High alignment accuracy printing was achieved using the high contrast metal markers on the source coupon. GSG Au contact pads were formed to enable the electric probing.

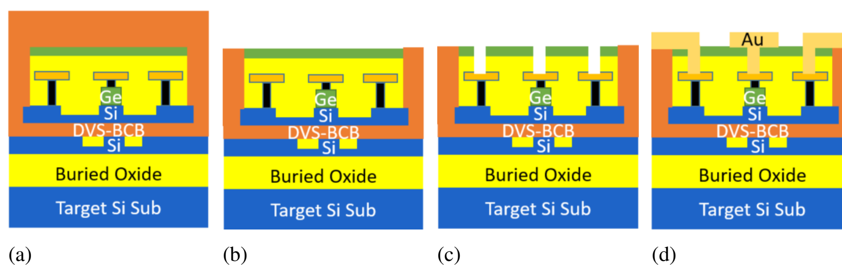


Figure 2.32: Schematics of the post-processing of the printed coupons.

2.6.4 Characterization of micro-transfer-printed SiGe photodiodes

Characterization of a transfer-printed photodiode consisted of both static and dynamic measurements. In the static characterization, the IV curve of the transfer printed germanium PD was measured and compared with a similar device on the source. Wavelength dependent responsivity was measured for the transfer printed device and then compared with the responsivity of the same device in the imec process design kit (PDK). Dynamic characterization consisted of small signal (3dB bandwidth measurements) and large signal (eye diagram and bit-error rate) measurements.

2.6.4.1 Static characterization results

The IV curves of the devices were measured using a Keithley 2400 current-voltage source, and they are depicted in Figure 2.34. The black points in this diagram represent the IV of the transfer printed device, which is compared to a similar device on the source, where the same post-processing schematics were applied as displayed in Figure 2.32. The result in Figure 2.34 reveals a decent match of these

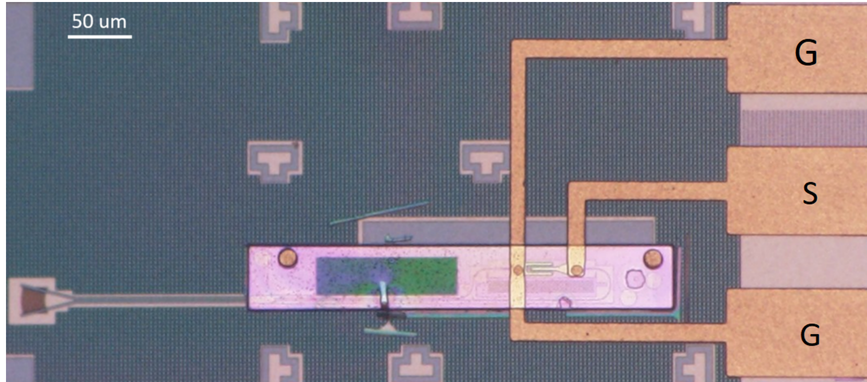


Figure 2.33: Microscope image of a germanium photodiode coupon printed on the target wafer, with the Au contact pads deposited. The printing was not perfect in this case, as it can be observed that part of the barrier was picked and printed.

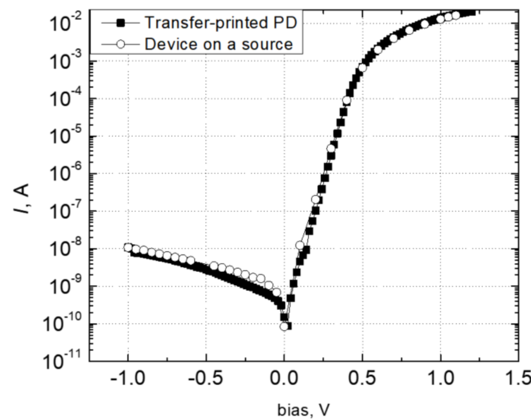


Figure 2.34: Measured IV characteristics of the transfer-printed germanium photodiode, compared with the IV of a similar device on the source wafer.

two curves, with the dark current measured to be 12 nA at -1 V bias and a series resistance of 29.6 Ω.

Figure 2.35 depicts responsivity measurement schematics. The TSL-510 tunable C-band laser light is coupled to the chip through a fiber-to-chip grating coupler. The transfer-printed photodiode is biased using DC probes that are connected to a Keithley 2400 current-voltage source. The photocurrent is subsequently measured.

Figure 2.36 presents the waveguide-referred device responsivity curve versus the wavelength. A responsivity of 0.66 A/W at 1550 nm is demonstrated. De-

Figure 2.35: Responsivity measurement schematics.

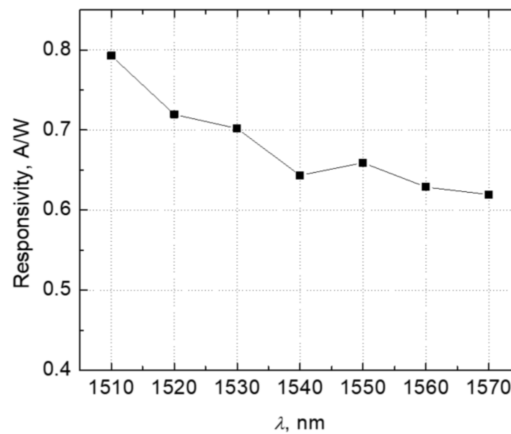


Figure 2.36: Waveguide-referred responsivity of the transfer-printed germanium photodiode as a function of wavelength.

creasing trend of the responsivity can be attributed to the decrease of absorption coefficient of germanium over the wavelength. These p-i-n iSIPP25G photodetectors were specified in the PDK with a device responsivity of 0.8 A/W at 1550 nm, which is higher than the value for the transfer printed device coupon. This is attributed to the finite coupling loss when coupling the light from the Si target wafer to the SiGe photodetector coupon.

2.6.4.2 Small-signal characterization

Schematics of the small-signal characterization of the SiGe PD are displayed in Figure 2.37. The key component is an Agilent 67 GHz Vector Network Analyzer (VNA), which, using channel 1, drives the 40 GHz Mach-Zehnder modulator (MZM). The modulator sends the modulated TSL510 C-band laser light to the photodiode chip, using a tilted optical fiber. The small signal response of the

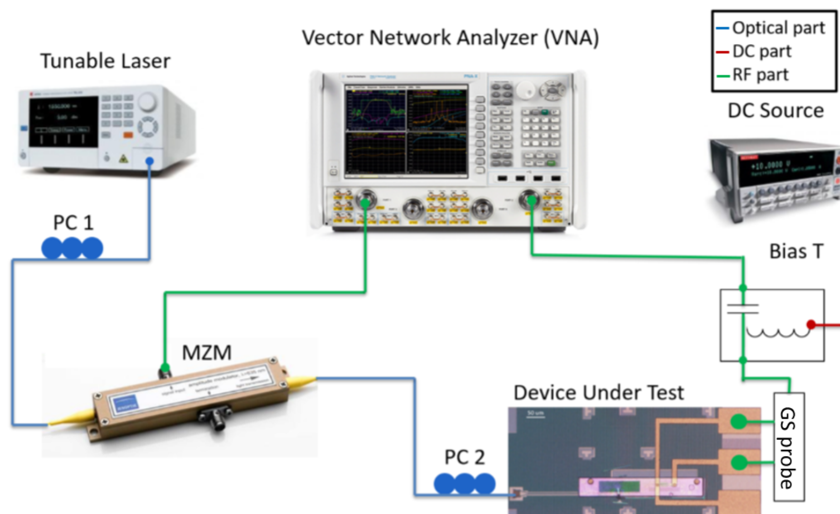


Figure 2.37: Small-signal measurement schematics.

photodiode is read out using the high-speed radio frequency (RF) probe that is connected to the DC Keithley 2400 current-voltage source by a bias-T. The RF part is simultaneously connected to channel 2 of the VNA. Biasing the photodiode at -0.5 V results in a slowly rolling-off frequency response, with a 3-dB bandwidth at 14 GHz (Figure 2.38). This behavior is attributed to the electrode structure (as the device spec in the iSIPP25G PDK showed a 3dB bandwidth of >35 GHz), which is presented in Figure 2.33, not being adequately optimized for high-speed performance.

2.6.4.3 Large-signal characterization

Figure 2.39 presents large-signal measurement schematics. Large signal measurements were performed using a Keysight M8195A arbitrary waveform generator (AWG), which was driving a 40 GHz $LiNbO_3$ MZM. A pseudo-random bit sequence (PRBS), with 2^7-1 and 2^{15} pattern lengths, and using a Root-Raised Cosine (RRC) filter, at 40 Gbit/s and 50 Gbit/s Non-Return-Zero On Off Keying (NRZ-OOK), was generated and the eye diagrams were measured using a Keysight DSA-Z 634A real time oscilloscope.

Figure 2.40 depicts the open eyes at 40 Gbit/s, using pattern lengths of 2^7-1 and 2^{15}, as well as open eyes at 50 Gbit/s. Bit-error rate (BER) curves were calculated using the real-time scope traces. Figure 2.41 depicts operation of the PD, below the 7% HD-FEC limit, with a 1.5 dB power penalty for going from 40 Gbit/s to 50 Gbit/s.

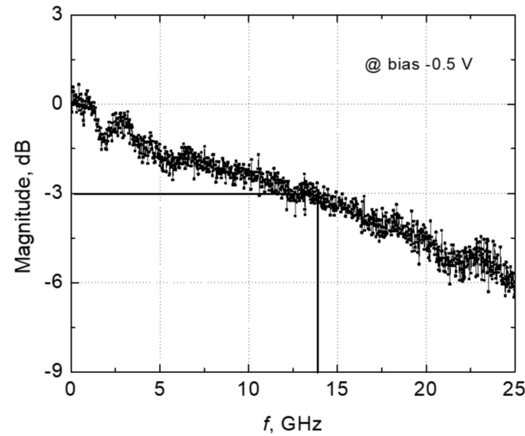


Figure 2.38: Small signal measurement result.

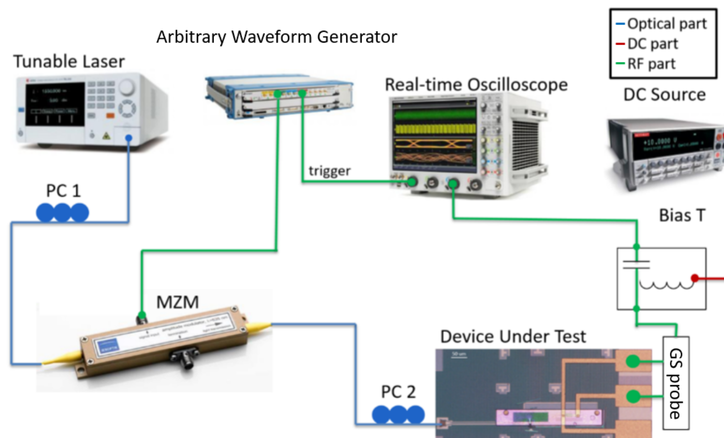


Figure 2.39: Large-signal measurement schematics.

2.6.5 Conclusions

We demonstrated the micro-transfer-printing of high-speed silicon-germanium photodiodes on a silicon-on-insulator passive waveguide circuit. We managed to successfully release the devices, while leaving the back-end stack intact. After picking and printing, we demonstrated high-efficiency coupling between the target waveguide and the device coupon, combining an alignment tolerant coupling structure with high-accuracy transfer printing. We obtained 0.66 A/W responsivity, open eye diagrams, and sub HD-FEC transmission at 50 Gbit/s. This demonstration paves the way for applying transfer printing to the realization of complex photonic

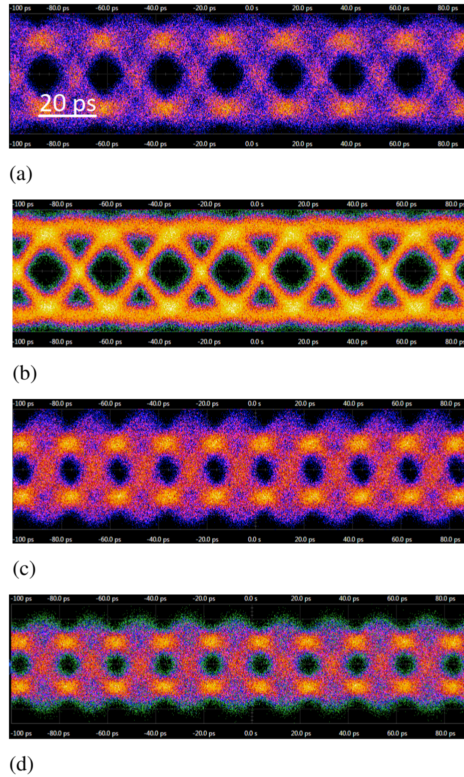


Figure 2.40: Eye diagrams measured for transfer printed SiGe PDs, using the real-time scope. (a) 40 Gbit/s using 2^7-1 pattern length, (b) 40 Gbit/s using 2^{15} pattern length, (c) 50 Gbit/s using 2^7-1 pattern length, (d) 50 Gbit/s using 2^{15} pattern length.

integrated circuits on a wafer scale. This potentially comprises both Si/Ge photonic and electronic devices, as well as III-V optoelectronic components, in ways which are both cost effective and time efficient.

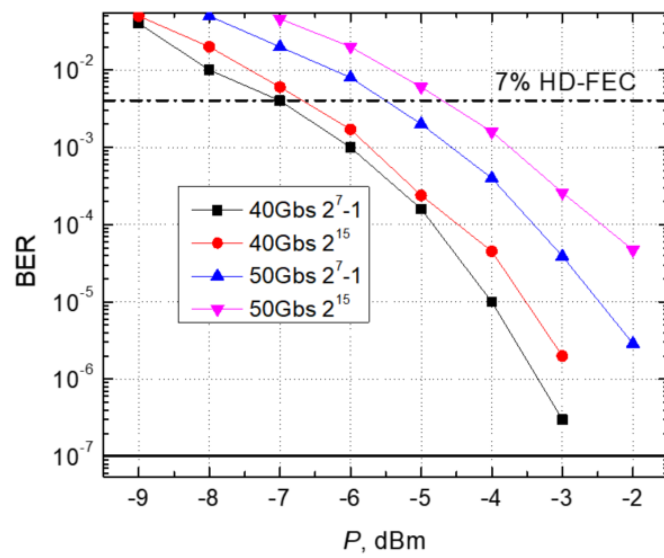


Figure 2.41: Bit-error rate curve measured for transfer printed SiGe PD.

2.7 Micro-transfer-printing of highly-efficient grating couplers.

In subsection 2.4 we concluded that releasing the 220 nm thin Si film is difficult as the 220 nm layer is too thin for the triangular Si tethers to support it. Moreover, the isotropic underetch using HF makes that the devices can not be arranged in dense arrays on the source wafer due to the undercut of the barrier.

In this subsection, we demonstrate a different solution for transfer printing passive silicon devices by fabricating, releasing, and transfer-printing grating coupler (GCs) structures for highly efficient fiber-to-chip coupling. We discuss an apodized, partially etched, grating couplers connected to a directional coupler implemented in an amorphous Si (a-Si) layer on a Si(111) substrate. Standard 220 nm silicon-on-insulator (SOI) wafers with top crystalline silicon (c-Si) were used for the target PIC. We discuss the simulation results and the grating and mask design together with the process development. Part of this section focuses on Si(111) substrate etching properties and afterwards, we discuss the process development results, process flow, transfer printing process, and characterization.

2.7.1 Design and performance

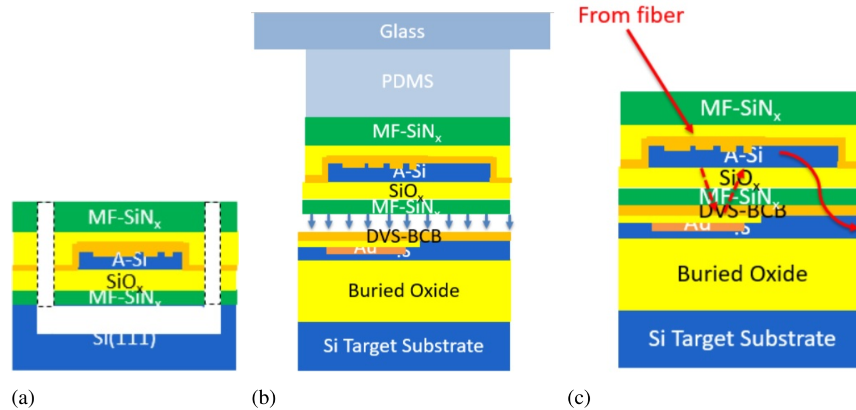


Figure 2.42: Envisioned integration scheme. The fabricated apodized grating in an a-Si layer released on the Si(111) substrate (a) was picked and transfer printed on top of the SOI wafer with the integrated metal mirror (b). The device operate such that when the light couples from the optical fiber, part of the light reflects from the bottom of the mirror, enhancing the coupling efficiency of the grating. In the second transition, a directional coupler structure is implemented so that the light couples into the SOI waveguide.

The aim of the experiment is to release and micro-transfer-print highly-efficient, apodized GCs defined in the a-Si layer on top of the SOI target that comprises a

metal mirror to enhance coupling efficiency (see Figure 2.42).

We propose the processing schematics displayed in Figure 2.43. Here, we use a Si(111) substrate (Figure 2.43(a)) and deposit ∼150 nm thick PECVD silicon oxide (SiO_x). Then we deposit the a-Si waveguide layer, which is 265 nm thick (Figure 2.43(b)) with a 105 nm grating etch depth (Figure 2.43(c)), which was then covered with a similarly thick (∼150 nm) silicon oxide top layer (Figure 2.43(d)) to protect the a-Si layer. The SiO_x layer is patterned and Si(111) substrate is accessed (Figure 2.43(e)). We underetch the Si(111) using a potassium hydroxide (KOH) solution (Figure 2.43(f))

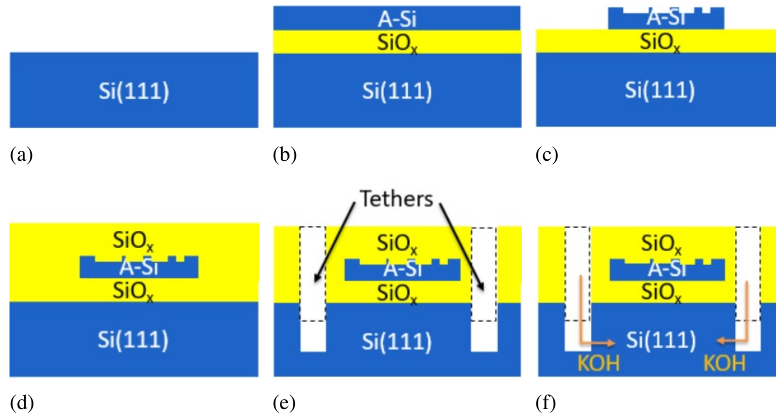


Figure 2.43: Schematics of the initially envisioned highly-efficient grating coupler release scheme. We deposit SiO_x and a-Si layers (b) on the Si(111) substrate (a). We pattern these layers using contact lithography and define the gratings using e-beam lithography (c). We then deposit the top oxide layer (d). In the next lithography step, we define the tethers and access the Si(111) substrate (e), which we then use to release the devices using a KOH solution (f).

The target PIC is displayed in Figure 2.44(a) and it is based on a 220 nm SOI platform with a 70 nm partial etching step (so-called rib waveguides) on which a 100/50-nm-thick SiO_x/DVS-BCB bi-layer was deposited to promote the adhesion with the printed GC structure. The DVS-BCB layer is used to reduce the thickness variations associated with the DVS-BCB layer during processing. A 70-nm-thick Au mirror was deposited after partially etching a recess in the target PIC. The metal mirror was added to enhance the directionality and thereby to increase the coupling efficiency. Simulations were performed considering the initially envisioned process flow in Figure 2.43.

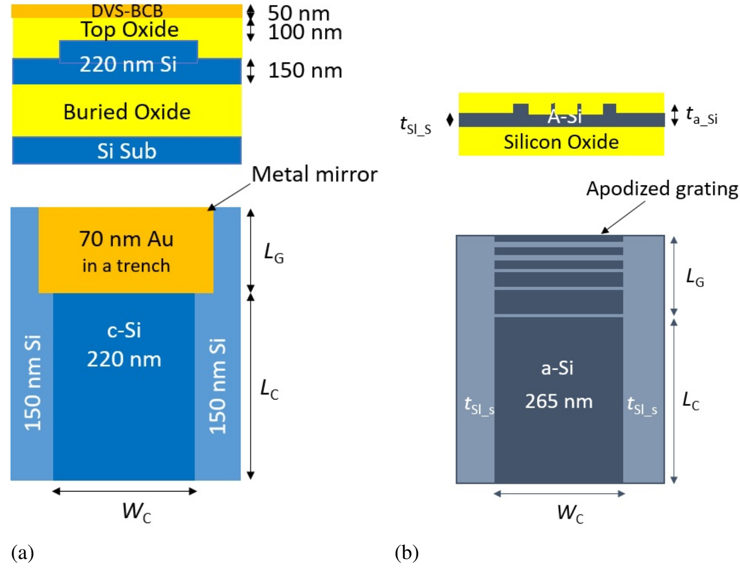


Figure 2.44: Target (a) and source (b) waveguide cross-sections (top) and top views (bottom).

2.7.1.1 Simulation results of apodized grating couplers and directional coupler

We focused on choosing the correct design for the source, as displayed in Figure 2.44(b). The simulated parameters are denoted as a-Si layer thickness (t_{a_Si}), slab layer thickness (t_{Si_S}), grating area length (L_G), and directional coupler waveguide length (L_C) and width (W_G). The thickness t_{a_Si} of the a-Si layer (refractive index of n = 3.35 at λ = 1550 nm) was determined by simulating the supermodes' effective index as a function of the layer thickness. The thickness t_{a_Si} = 265 nm was chosen as this results in phase-matching between the printed a-Si and the rib c-Si waveguide defined on the target. The separation between waveguides was 400 nm.

Afterwards, the vertical separation of the two waveguides was determined by aiming at an approximately 20 μm coupling length L_C for compactness. We chose 150 nm buried oxide (BOX) thickness on the source and 100 nm top oxide with a 50 nm DVS-BCB adhesion promotor on the target. The coupler width W_C = 13.5 μm was kept equal to the grating width to achieve optimal mode matching with the 10.4 μm mode field diameter of the Gaussian beam of the fiber without introducing any tapering on the source structure.

The 2D grating simulation was performed in finite difference time domain (FDTD) software. The mode was launched into the waveguide 10 μm away from

the first slit and the scattered field at the top surface of the grating coupler (1 μm above the top a-Si waveguide) was recorded as in [15], assuming angled cleaved fibres and a SiO_x index-matched environment. The simulated gratings were apodized where the fill factor (FF) had linear variation (similar to that shown in Figure 2.44(b)) and the simulation methodology was similar to that described in [16]. The grating structure was tailored along the propagation direction, taking into account local corrections of the grating period according to the grating formula:

$$n_{ox}k_0 \sin\theta = k_0 n_{eff}^G - K \tag{2.4}$$

Here, n_{ox} is the refractive index of silicon oxide, k_0 is the wavevector in vacuum ($2\pi/\lambda$), θ is the fiber angle with respect to normal direction, and K is the reciprocal lattice vector. n_{eff}^G is an effective grating index that can be described as:

$$n_{eff}^G = FF n_{eff}^{thick} + (1 - FF) n_{eff}^{thin} \tag{2.5}$$

Where n_{eff}^{thick} is the effective thickness in the full a-Si slab area (t_{a_Si}) and n_{eff}^{thin} is the effective index in the partially etched area.

The simulated grating results are displayed in Figure 2.45. We defined a grating coupler of 26 periods and simulated the optimal linear fill factor coefficient (FF_{lin}) and the etch depth of the grating (see Figure 2.45(a)). The optimum linear fill factor (FF_{lin} = 0.045 μm^{-1}) and the optimal etch depth of 105 nm. By sweeping the bottom oxide thickness on the source and the fibre angle, the optimal values of 140 nm and 20 deg were obtained respectively (Figure 2.45(b)). This led to a total simulated coupling efficiency of 96.2% (-0.17 dB) at 1550 nm. The reflection reached -27 dB around 1550 nm all thanks to the apodization and the small etch step. The total length of the grating section (L_G) was estimated as 18.4 μm.

Finally, we used all the simulated parameters of the grating coupler to estimate the directional coupler dimension for efficient power transfer. The simulations were performed using eigenmode expansion software assuming the source coupons were printed on top of the target substrate. A nearly lossless power transfer was achieved with a length of L_C = 19.3 μm, where the reflection was negligible because of the large separation between the waveguides (Figure 2.46(a)). A transfer printing misalignment of ± 1 μm was considered and Figure 2.46(b) shows the response of the directional coupler to tolerances such as lateral misalignment and variations of the bottom oxide thickness on the source wafer.

Wide waveguides led to smaller insertion loss once the lateral misalignment increased, therefore, one can achieve -1dB coupling for 2 μm lateral misalignment by choosing a waveguide width of W_C = 13.5 μm. Figure 2.46(d) shows the top

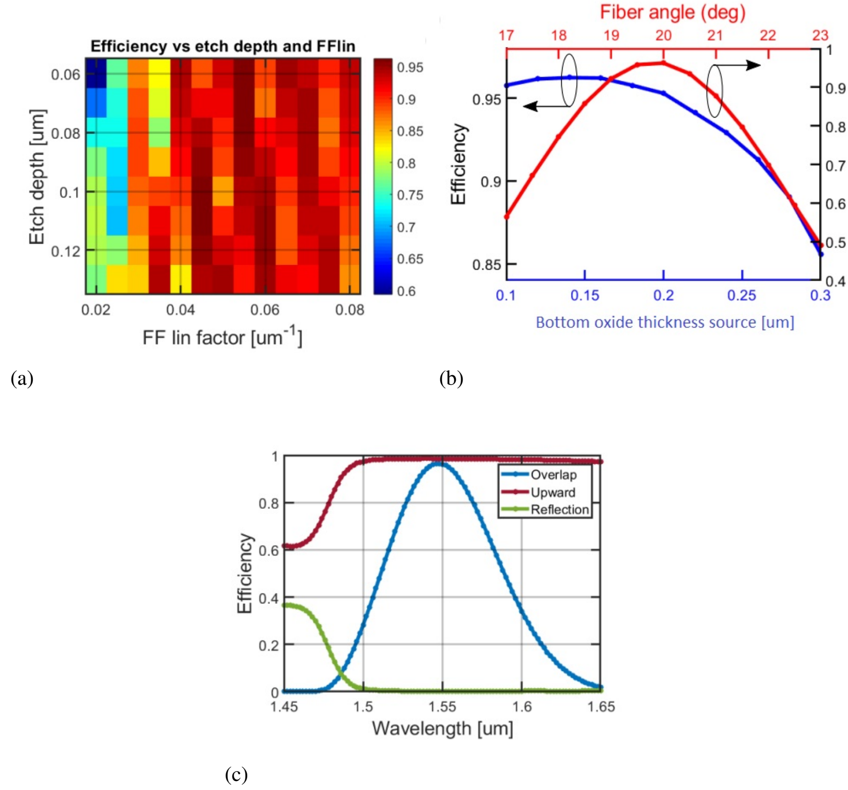


Figure 2.45: Numerical results of performance of the grating coupler. (a) Sweep of the linear fill factor FF_{lin} and the etch depth; (b) Sweep of the bottom oxide thickness on the grating coupler source wafer using the optimal values found in (a). The angle was swept to find the optimum by using the optimal value of the bottom oxide thickness; (c) The grating response versus wavelength.

view and the cross-section of a simulation with a misalignment of 2 μm, where it was possible to observe the effect of the presence of a misalignment on the optical mode distortion. In Figure 2.46(c), a directional coupler 1dB bandwidth of 144 nm is shown, where the overall 1dB bandwidth of the grating coupler + directional coupler is 45 nm and it is dominated by the GC response.

2.7.1.2 Apodized grating coupler dimensions

The simulated apodized GC dimensions are shown in Table 2.1. The grating makes use of 26 periods and the linear fill factor of FF_{lin} = 0.045 μm^{-1} will be implemented in the design. The grating will be defined using an e-beam process.

Period N.	Slit, nm	Period, nm
1	63.4	634.4
2	81.8	637
3	100.5	639.7
4	119.4	642.3
5	138.6	645
6	158	647.8
7	177.6	650.6
8	197.5	653.4
9	217.7	656.2
10	238.1	659.2
11	258.8	662.1
12	279.8	665
13	301.1	668.1
14	322.6	671.1
15	344.5	674.2
16	366.7	677.4
17	389.1	680.6
18	411.9	683.3
19	435	687.1
20	458.5	690.4
21	482.3	693.8
22	506.5	697.4
23	530.9	700.7
24	555.8	704.2
25	581.1	707.8
26	606.7	711.5

Table 2.1: Simulated apodized grating coupler dimensions.

2.7.2 Process development

Figure 2.43 shows the schematics of initial process attempt of releasing the apodized gratings written in the a-Si layer using the Si(111) substrate as a release layer. Top dielectric layers were used as a-Si protection and tethers. Before we start the process development, however, it is necessary to understand the properties of the etching of the Si(111) wafer layer using the potassium hydroxide (KOH) solution as underetching of the coupon is dependent on the mask orientation. We plan to use SiO_x as tether material, therefore it is necessary to develop the new tether system to efficiently anchor the suspended devices. Moreover these should cleanly break at the correct points when the devices are picked.

2.7.2.1 Underetching the Si(111) substrate

Si(111) shows particular anisotropic etching properties [17]. To better understand the anisotropy in the (111) direction, consider a cubic octahedron oriented in the (111) direction on the wafer (as depicted in Figure 2.47(a)).

The etch behavior in the Si(111) is determined by $\{111\}$ planes and can be found by intersecting the in-plane points (A, B, C) and projected out-of-plane points (A', B', and C'; Figure 2.47(a) and (b)) on the octahedron. By plotting all the lines of intersection on the 2D plane, a hexagonal shape is obtained (Figure 2.47(b)).

These features help to explain the Si(111) undercut features versus the mask orientation and this is displayed in Figure 2.48. Anisotropic etching in XY-directions takes place at a local scale by etch-steps travelling along the $\{111\}$ planes. This means that once the mask is aligned with one of the hexagonal $\{111\}$ etching orientations, the underetching occurrs along the other two $\{111\}$ planes (see Figure 2.48(a)). Once the mask is misaligned, the etching happens along all three $\{111\}$ hexagonal planes in the crystal (see Figure 7(a), right-hand side).

Figure 2.48(b) summarises the discussion. Si(111) undercut profile can be chosen by orienting the mask along the hexagonal $\{111\}$ planes.

2.7.2.2 Amorphous silicon protection

The first release attempt was performed according to schematics displayed in Figure 2.43 skipping the grating patterning step. We dipped the substrate in the KOH (28%) solution heated at 75°C [18]. Figure 2.49(a) shows that the top surface was damaged after 10 minutes of KOH etch with plenty of pinholes present. The a-Si layer was clearly attacked.

To better understand if the top SiO_x layer provides enough protection from the aggressive KOH agent, we deposited a 150 nm SiO_x layer on top of the Si(111) substrate, a 265 nm a-Si layer, and variable thicknesses of the top SiO_x layer (150 nm to 1 μm) without any further patterning. We immersed these structures into the KOH solution for a second time for $\sim$10 minutes. Figure 2.49(b) shows that the top SiO_x layer quality deposited on a-Si is poor and this is visible to the naked eye.

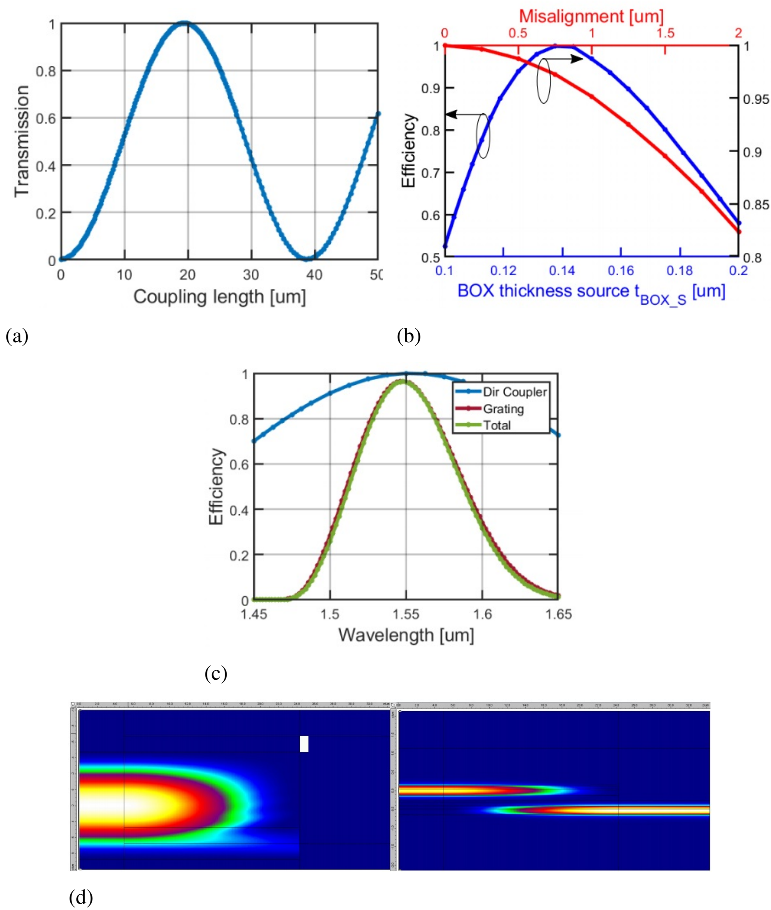
The experiment shows the poor deposition of PECVD-SiO_x on the a-Si layer as it yields pinholes. To solve this problem, we added $\sim$40 nm of atomic layer deposition (ALD)-SiO_x on top of the patterned a-Si layer (see Figure 2.50). The system used bis(diethylamino)silane (BDEAS) precursos gas combined with the O_2 reactant for 550 cycles at 250°C. ALD is known for its conformal deposition properties [19] [20], therefore, we changed the process flow by depositing 40 nm of ALD-SiO_x (Figure 2.50(a)) and we added $\sim$60 nm of the PECVD silicon oxide layer on top of the ALD-SiO_x (Figure 2.50(b)). The Si(111) substrate was then

accessed (Figure 2.50(c)) and the patterned structure was immersed in the KOH solution.

The results can be seen in Figure 2.51. After the first 5 minutes of etching, the surface was better compared with the surface displayed in Figure 2.49(a): the quality improved with no obvious pinholes present. After continuing etching for 15 minutes (Figure 2.51(b)), however, the a-Si and SiO_x layers began to disappear. After 25 minutes of KOH etching only, the a-Si and SiO_x layers appeared to have gone (Figure Figure 2.51(c)). This can be explained by the fact that KOH has poor selectivity towards SiO_x. Thermal oxide selectivity versus Si is 320:1 [21]. The selectivity in this case was even poorer considering the top 270°C PECVD silicon oxide top layer.

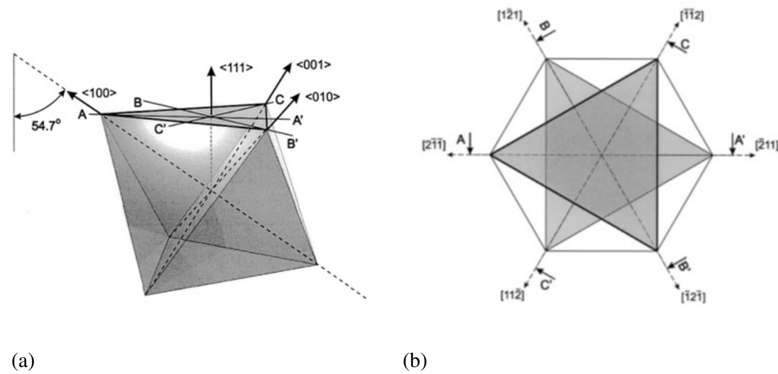
Therefore, an additional 50 nm mixed frequency top and bottom silicon nitride (MF-SiN_x) layers should be added to protect the Si and SiO_x layers from the KOH. The new schematics are presented in Figure 2.52.

Figure 2.53(a) depicts the surface of the chip after 7 minutes of etching, where a clean etching profile was obtained. After 25 minutes of etching (Figure 2.53(b)), it can be seen that the colour of the surface of the chip remained largely unchanged, what indicates that the top silicon nitride layer is not attacked by the KOH. Some penetration of KOH into the a-Si coupons is visible, however, causing many of the coupons to be destroyed. Tethers, on the other hand, seem also not strong enough to support all the released devices. This is visible on the left in Figure 2.53(b).



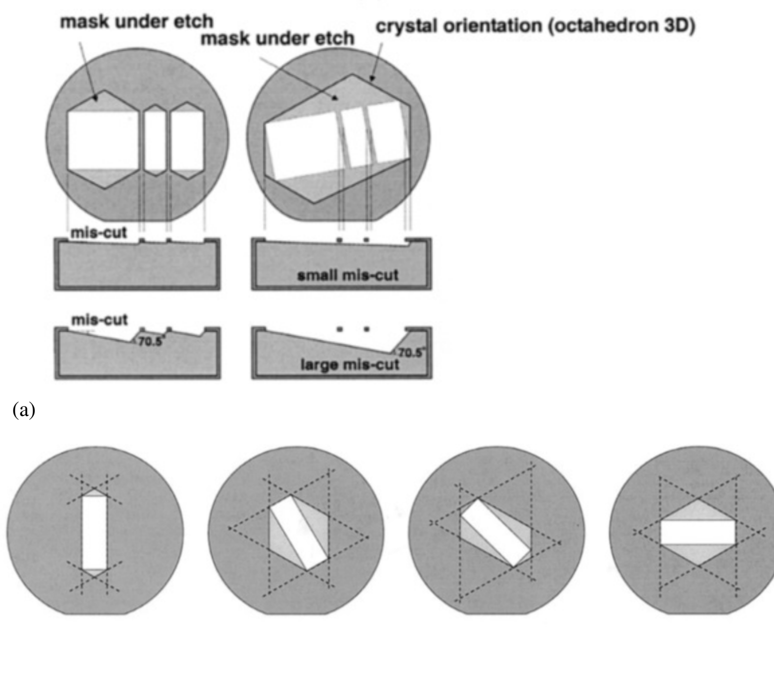
(a) (b) (c) (d)

Figure 2.46: Performance of the directional coupler. (a) Transmission versus coupling length; (b) Efficiency as a function of the misalignment and variation of buried oxide thickness; (c) The directional coupler response versus wavelength. The grating coupler response has been added to compute the total bandwidth of the device, which is dominated by the grating coupler; (d) A top-view of the simulation with 2 μm of misalignment indicated by the white bar. A cross-section of the same simulation is displayed on the right.



(a) (b)

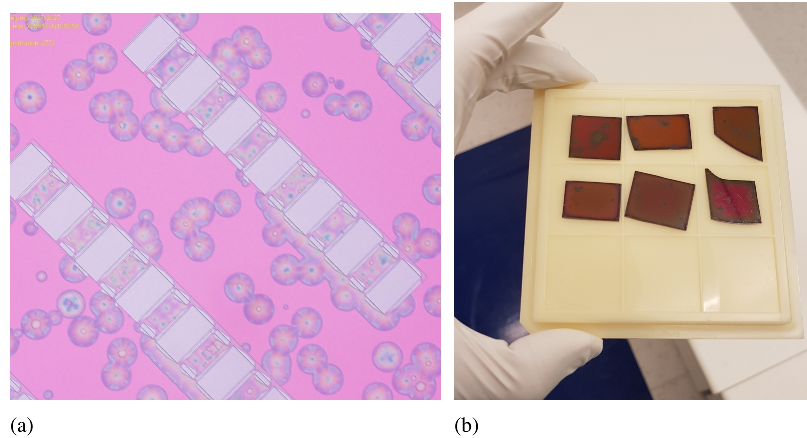
Figure 2.47: Spatial positioning of the crystal octahedron built with {111} planes oriented in a (111) direction on the silicon wafer (a); Hexagonal contour formed by the projection of the atomic octahedron structure on the (111)-plane (b) [17].



(a)

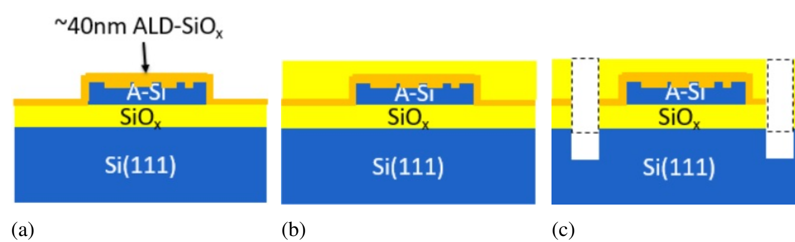
(b)

Figure 2.48: Etch geometries in the XY directions obtained for the wafers and the underetching effects in the Z-direction dependent on the mask orientation (a). Effect on the underetching versus the mask orientation. Light grey colour indicates the underetching direction (b) [17].



(a) (b)

Figure 2.49: Microscope image of the surface of the patterned sample using a PECVD-SiO$_x$ protection layer on a-Si after keeping the sample for 10 minutes in the KOH solution. (b) Surfaces of the samples using different thicknesses of PECVD-SiO$_x$ protection layers deposited directly on a-Si after keeping these samples for ∼10 minutes in the KOH solution.



(a) (b) (c)

Figure 2.50: Schematics of re-attempted release of Si(111) substrate using the deposition of ∼40 nm of ALD-SiO$_x$ on top of a-Si (a). Depositing additional ∼60 nm of PECVD-SiO$_x$ (b). The substrate was immersed into KOH after accessing the Si(111) substrate.

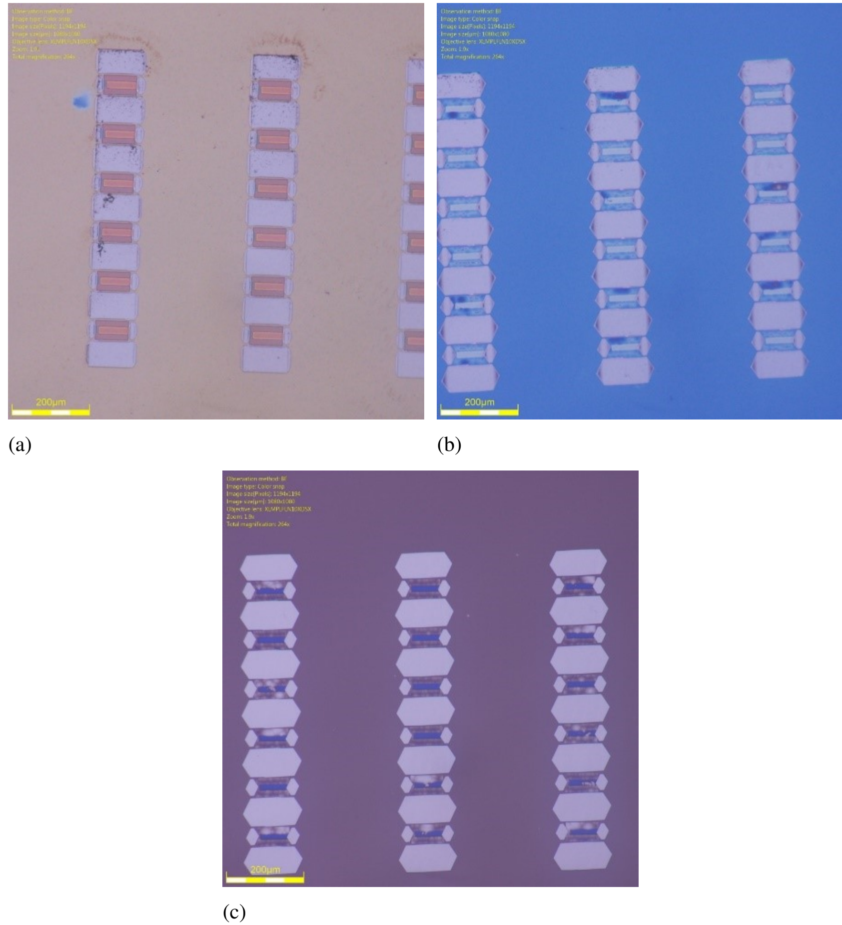


Figure 2.51: Attempted release in KOH solution of structures using a combination of top atomic layer deposition and PECVD silicon oxide protection layer after 5 minutes (a), 15 minutes (b), and 25 minutes (c) of KOH etching time.

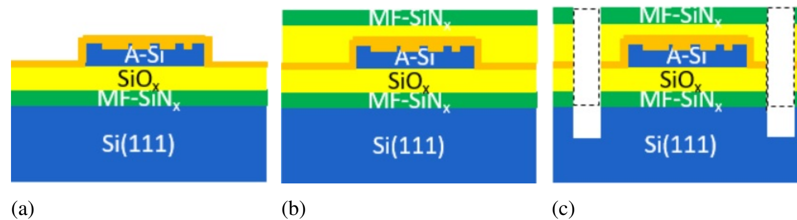
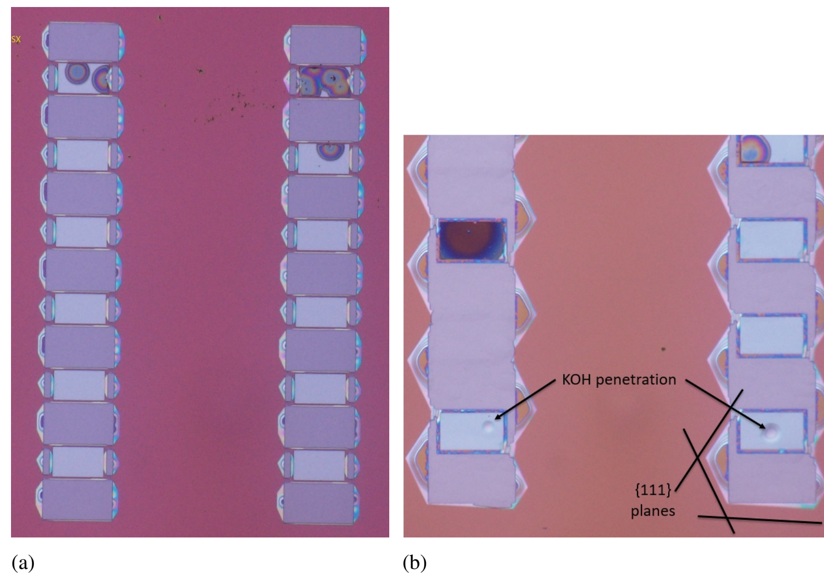


Figure 2.52: Schematics of updated process flow using the PECVD mixed frequency silicon nitride protection layer to protect silicon oxide and amorphous silicon layers.



(a) (b)

Figure 2.53: Microscope images of attempted release in KOH solution using silicon nitride top and bottom protection layers, after 7 minutes (a) and 25 minutes (b) of etching time.

Importantly, it was shown that a combination of PECVD & ALD silicon oxide and silicon nitride can protect the a-Si layer from KOH penetration. The discussion of the tether design is continued later. Next, we attempted to incorporate the GCs into an a-Si layer and checked how effectively we could release these.

2.7.2.3 Grating coupler definition and release

The sizes of the slits and the periods of the apodized GCs are described in Table 2.1. We defined the GCs in the a-Si layer using e-beam lithography. We used the A-RP-6200-09 resist [22], which yields a thickness of ∼250 nm. The etch depth of 105 nm was realized using a CF_4:SF_6:H_2 recipe in the RIE for ∼1.5 minute.

An e-beam exposure dose of 175 μC/cm^2 was used and the effect of overexposure of the slit region had to be considered. Therefore, it was necessary to design the GC slits to be 30 nm smaller on the mask than the values defined in Table 2.1. The scanning electron microscopy (SEM) image of the defined grating is shown in Figure 2.54. It can be seen that the first two narrowest grating slits (63.4 nm and 84.1 nm) were difficult to fabricate because of the too narrow dimensions.

After we deposited ∼45 nm of ALD-SiO_x, ∼55 nm of PECVD-SiO_x, and ∼50 nm of MF-SiN_x, we patterned the tethers, accessed the Si(111) (see Figure 2.52), and immersed the structures into the KOH solution. The results are displayed in Figure 2.55. After keeping the fabricated source substrate with the patterned

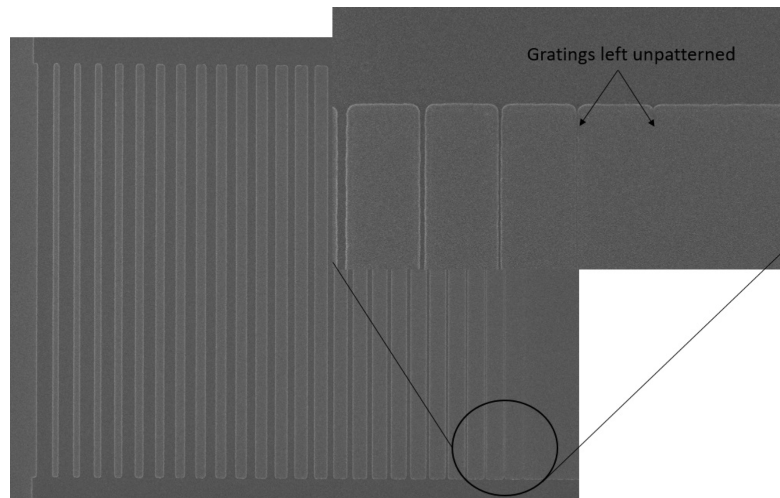


Figure 2.54: Scanning electron microscopy image of initial attempt to fabricate grating couplers on the a-Si layer. The picture shows the clearly unpatterned first periods of the grating coupler.

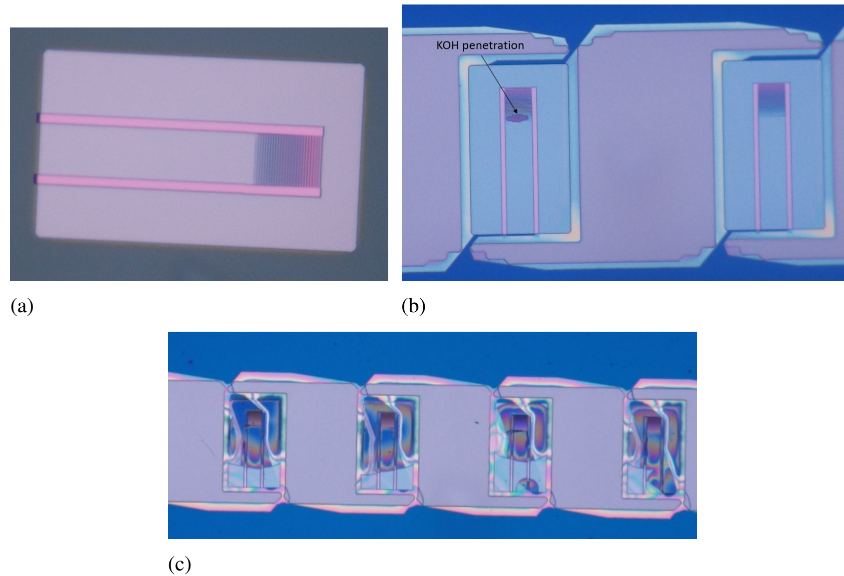
GCs and the directional coupler waveguides (Figure 2.55(a)) in the KOH solution for 7 minutes, the chemical penetrated the a-Si layer in the narrow grating slit region (Figure 2.55(b)). After keeping these structures in the KOH for 25 minutes, virtually all a-Si in the coupon area was etched (Figure 2.55(c)).

Figure 2.56 displays the focused ion beam (FIB) cross-section result. It can be seen that the PECVD deposited top layers cannot conformally cover the narrow grating slits. We expected, however, that thicker top layers could prevent the KOH penetration into the a-Si layer and increase the release yield. Therefore, we introduced two modifications: we repeated the process as depicted in Figure 2.52, adding a thicker top silicon nitride ($\sim$170 nm instead of 50 nm) top protection layer, and we increased the two narrowest grating slit dimensions on the mask of the GC.

The results of repeating the same process as displayed in Figure 2.52 with the thicker PECVD MF-SiN$_x$ top layer, immersing the substrate in the KOH solution for $\sim$27 minutes are shown in Figure 2.57 by orienting the coupons 45° with respect to the major flat. The devices were cleanly released with no evident damage to the a-Si layer. After solving the main release problems, we focused on choosing a suitable tether design.

2.7.2.4 Tether design

As we have already discussed in the previous sections of this work, tethers have to be strong enough to hold the fragile released devices in place after underetching



(a) (b) (c)

Figure 2.55: Microscope images of the patterned grating coupler in the amorphous silicon layer (a); Attempted release of grating couplers using a ∼50 nm MF-SiN$_x$ top layer after 7 minutes (b) and 25 minutes of KOH etching (c).

the release layer. They also need to break in the correct place when the devices are picked with the PDMS stamp. We fabricated a number of different devices with variations in tether design and width.

The most important conclusions are presented in Figure 2.58. One can see that the staicase-shaped tethers with the narrowest point (2 - 6 μm wide) cannot stop the KOH penetration into the barrier region and the KOH propagated further into the barrier layer under the tether (Figure 2.58(a)). It was not possible to pick these devices using the PDMS stamp, probably because they collapse onto the substrate.

Same tethers with the wider narrowest point (8 - 12 μm) limited the KOH penetration into the barrier (Figure 2.58(b)). Thus, the thicker tethers received additional support from the barrier and could firmly hold the suspended devices in place. As a result the tethers broke cleanly at the narrowest points when we attempted to pick these released devices using the PDMS stamp (see Figure 2.59(a)) and print them onto a glass substrate. The devices printed on the glass looked clean from the top view (Figure 2.59(b)), but the backside view on the bottom of the glass substrate indicated some printing imperfections (Figure 2.59(c)). This could be attributed to the dirty glass substrate surface or the fact that a longer release etching time was necessary. The important conclusion, however, is that staircase-shaped tethers with 12μm wide narrowest points are good for further use.

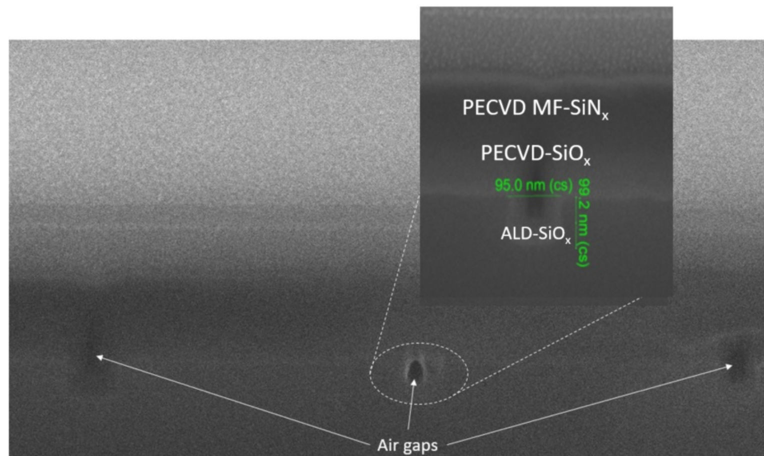


Figure 2.56: Focused ion beam cross-section image of the patterned grating coupler in the narrow-slit region with the top layers applied. A clear air gap is visible between the ALD and PECVD deposited layers.

2.7.2.5 Fabrication of the target substrate

The target substrate fabrication is depicted in Figure 2.60. We used a standard SOI substrate, which consists of a 220 nm Si top layer and 2 micron buried oxide (Figure 2.60(a)). In the first optical lithography step, we opened a $\sim$100 nm deep recess using RIE (CF_4:SF_6:H_2) - (Figure 2.60(b)), in which we deposited $\sim$100 nm gold to act as a mirror (Figure 2.60(c)). Next, we used the e-beam process to define 70 nm etched waveguide trenches (Figure 2.60(d)). After this, we deposited 110 nm PECVD-SiO_x (Figure 2.60(e)) and a thin $\sim$40 nm DVS-BCB bonding layer was spin-coated and partially cured at 180°C (Figure 2.60(f)) to provide a planar surface for the transfer printed coupons.

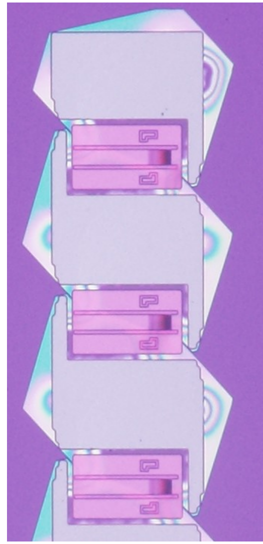


Figure 2.57: Microscope image of the grating coupler structures with the thicker (∼170 nm) silicon nitride top layer protection released on the source after immersing the substrate in the KOH solution for 27 minutes.

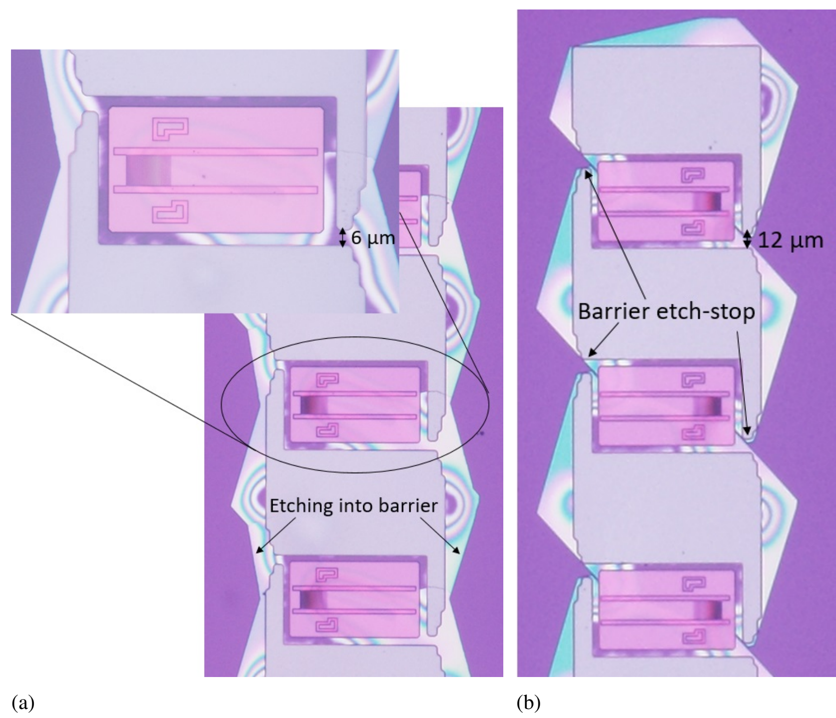


Figure 2.58: Microscope image of the surface of the chip after releasing grating couplers with different tether designs for 30 minutes. After release using 6μm wide tethers (a) and 12μm wide tethers(b).

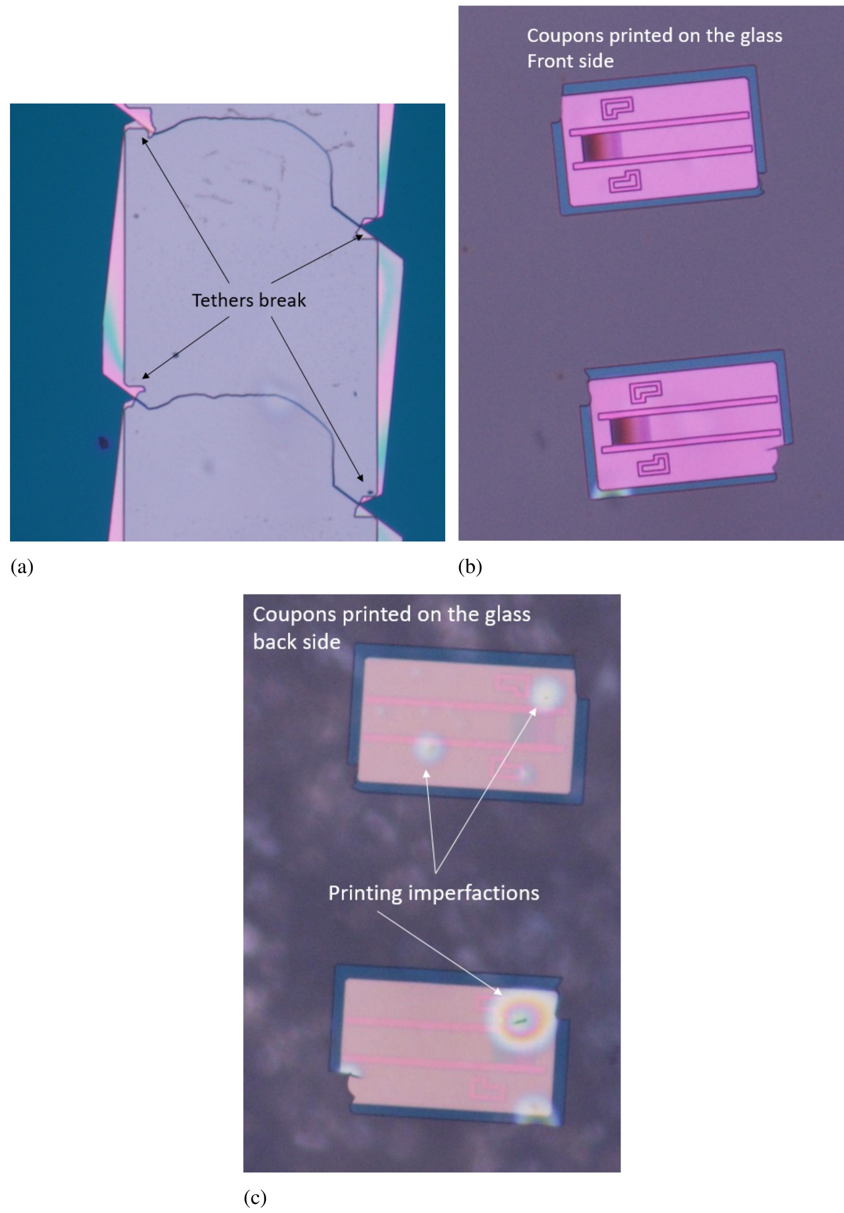


Figure 2.59: Microscope image of the surface of the chip with the thicker tethers when the released coupons were picked (a). Front-side (b) and back-side (c) image of these coupons printed onto a glass substrate.

The SEM images of the initial target substrate fabrication attempt are displayed in Figure 2.61. Initially, a grainy metal surface was obtained (Figure 2.61(a)). The FIB image depicted unclean metal with many defects present on the etched bottom of the silicon surface (Figure 2.61(b)). Because the same lithography step was used for plasma etching as well as for Au mirror deposition, this could be the result of photoresist re-deposition while etching the Si recess. We tackled this problem by using a deeper recess etch ($\sim$100 nm) and by keeping the substrate for an additional 30 seconds of O_2 plasma treatment after the Si recess etch to clean the bottom of the etched Si.

The result of this is displayed in Figure 2.61(c) and (d). A cleaner metal was deposited in the recess. The FIB image shows the 130 nm thick metal, which was about 30 nm thicker than the etched silicon level (Figure 2.61(d)).

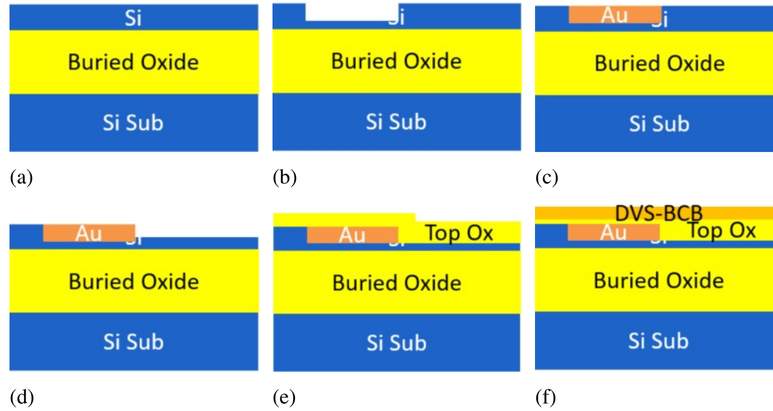


Figure 2.60: Schematics of the fabrication of the target substrate.

2.7.3 Experiment

The designed source and target substrates are depicted in Figure 2.62. The individual coupon size on the source was 95 μm $\times$60 μm and comprised an apodized GC, a 60 μm long directional coupler waveguide, and the Tetris-brick transfer printing alignment markers, which were defined in the same e-beam process step. The coupon was anchored to the barrier by staircase-shaped tethers with a width of 12 μm at the narrowest point. We placed six of these coupons with a 127 μm pitch in a total release area of 800$\times$100 μm on the source substrate (Figure 2.62(a)), which matched the PDMS stamp dimensions available.

The goal of the experiment was to pick six of these coupons in one picking cycle and transfer print these onto the target substrate. The pitch of the adjacent waveguides and the metal mirrors were defined on the same 127 μm pitch. Dur-

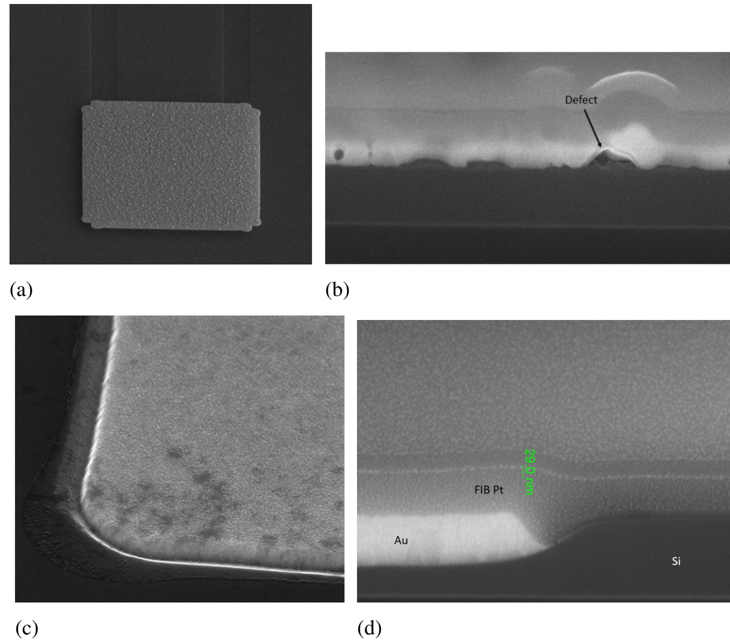
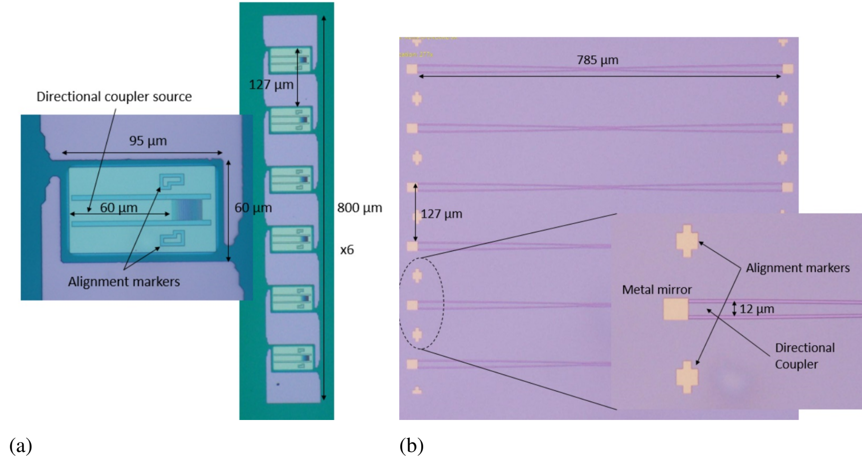


Figure 2.61: Fabrication of the metal mirror in the Si recess. Scanning electron microscope image of the Au deposited in the recess indicating a grainy metal (a). The FIB image indicates a dirty Si surface with a lot of air bubbles present (b). Scanning electron microscope image of the Au deposited in the Si recess using an additional 30 seconds of O_2 plasma treatment and thicker recess etch with the thicker deposited metal (c). The FIB cross-section depicts a clean metal deposited in the Si recess with a 30 nm height difference (d).

ing the initial metal deposition step, we defined the metal mirrors together with the transfer printing alignment markers on the target substrate, which enabled a center-to-center alignment scheme using in-built COGNEX^{TM} pattern recognition sofware. Also, on the target wafer, we defined waveguides that tapered from 12 μm wide (compatible with the directional coupler on the source) to a single mode 650 nm wide waveguide and back to 12 μm again over the length of 785 μm (Figure 2.62(b)). In this experiment, we aimed to transfer print highly efficient GCs on the left and right sides of the waveguides checking the fiber-to-fiber optical transmission.

2.7.4 Final process flow

Figure 2.63 depicts the final process flow of the source substrate. On the carefully cleaned Si(111) substrate (Figure 2.63(a)), we deposited 50 nm of PECVD mixed frequency silicon nitride (Figure 2.63(b)) and 100 nm of the standard PECVD sil-



(a) (b)

Figure 2.62: Microscope images of the unreleased source and target substrates with the insets indicating the chosen dimensions.

icon oxide (Figure 2.63(c)). Then, we deposited 265 nm of PECVD a-Si (Figure 2.63(d)), which we patterned using optical lithography (Figure 2.63(e)). On top of the a-Si layer, we patterned the apodized gratings together with the directional coupler waveguide using e-beam lithography with a 175 μC/cm^2 exposure dose (Figure 2.63(f)). We then deposited $\sim$40 nm of ALD-SiO$_x$ (Figure 2.63(g)) and added an additional $\sim$60 nm of PECVD SiO$_x$ on top (Figure 2.63(h)), together with $\sim$200 nm of PECVD MF-SiN$_x$ (Figure 22(i)). Then, using the RIE CF$_4$-SF$_6$-H$_2$ recipe for $\sim$15 minutes, we patterned the tethers and etched $\sim$1 micron into Si(111) substrate layer (Figure 2.63(j)). These structures were then immersed into a gently steered 28% KOH solution heated to 75^{o}C. After about 35 minutes, the coupons underetched (Figure 2.63(k)) and the highly-efficient GC coupons became free hanging, suspended membranes anchored to the side barrier by tethers. By applying the 800$\times$100 μm PDMS stamp on top of the coupons and quickly moving the stamp to the vertical direction, the tethers broke in the correct places and the coupon was picked (Figure 2.63(l)). By moving the stamp within close proximity of the target substrate, we aligned the coupon with respect to the target substrate using the defined alignment markers by the in-built COGNEX^{TM} pattern recognition software. By laminating the coupon with respect to the target wafer (Figure 2.63(m)) and slowly moving the stamp in the vertical direction, the stamp delaminated from the coupon, therefore, the coupon stayed attached to the target substrate (Figure 2.63(n)). The top view of the released coupons is depicted in Figure 2.64. In this experiment coupons were oriented 90 deg with respect to major flat. The fabrication of the target substrate was according to the processing

demonstrated in Figures 2.60 and 2.61.

The surfaces of the source and target substrates after completing the transfer printing process are depicted in Figure 2.65. It can be seen that the tethers on the source substrate broke cleanly at the narrowest points, leaving no Si residue on the bottom (Figure 2.48(a)). The lines connecting the two tethers left on the source substrate may be attributed to the angled etch in the Z-direction on the source. This made no impact on the pick-up of the devices nor on the tether break.

Figure 2.65(b) depicts the coupons printed on the target substrate. Six devices were printed on the left-hand side and on the right-hand side of the target wafer. The zoomed-in image shows clean print and a good alignment where the grating coupler transfer printed on top of the metal mirror and the directional coupler on the source interfaces with the directional coupler on the target substrate.

2.7.5 Characterization

Transmission measurements were carried out using a pair of single-mode optical fibers connected to the GCs on the target waveguide circuit. The measurement schematics are displayed in Figure 2.66. An HP8153A power meter and a Santec TSL-510 C-Band tunable laser were used to measure the fiber-to-fiber transmission.

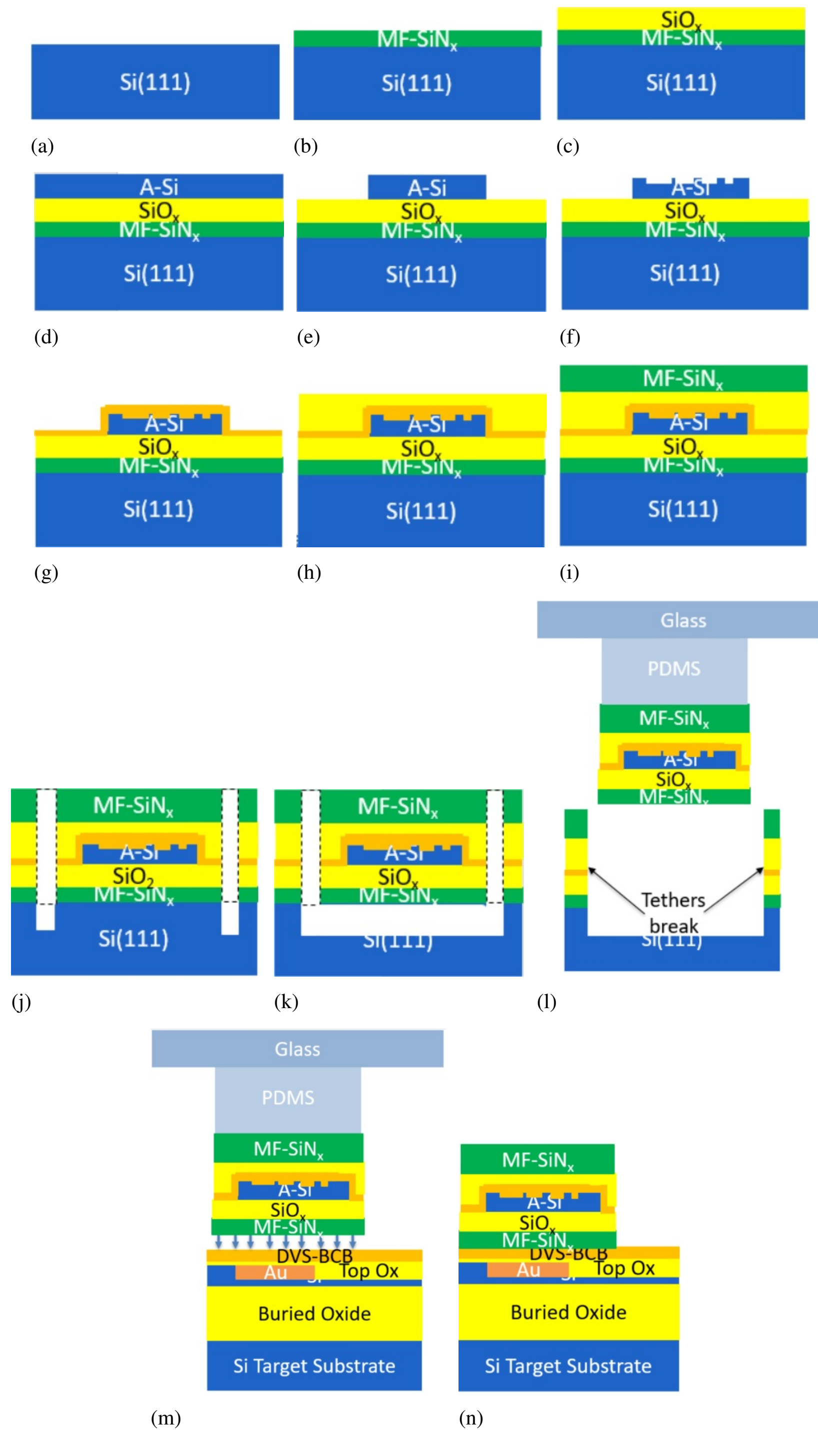


Figure 2.63: Schematics of the final process flow of the fabrication of the source.

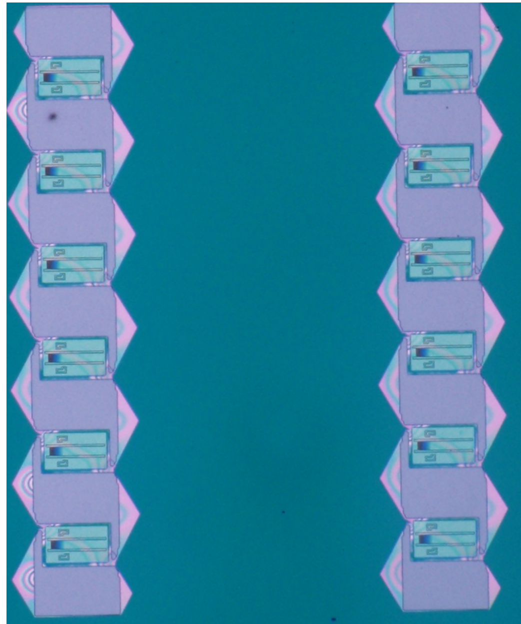
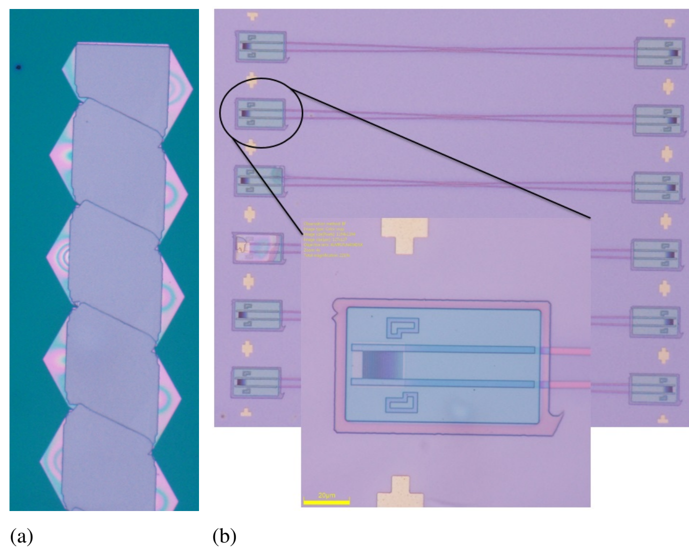


Figure 2.64: Highly efficient grating couplers released on source wafer.



(a) (b)

Figure 2.65: Microscope images of the source substrate with the clean tether break (a) and the target substrate (b) after completing the transfer printing experiment.

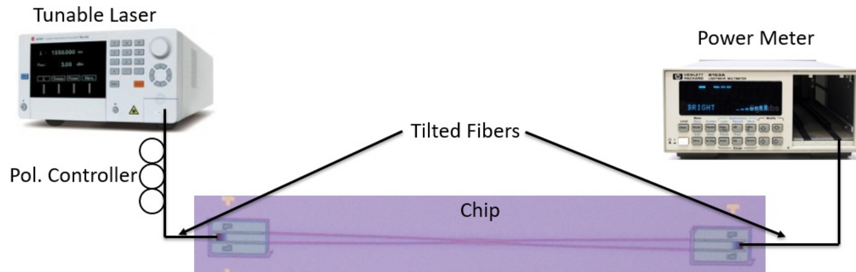


Figure 2.66: Transmission measurement schematics.

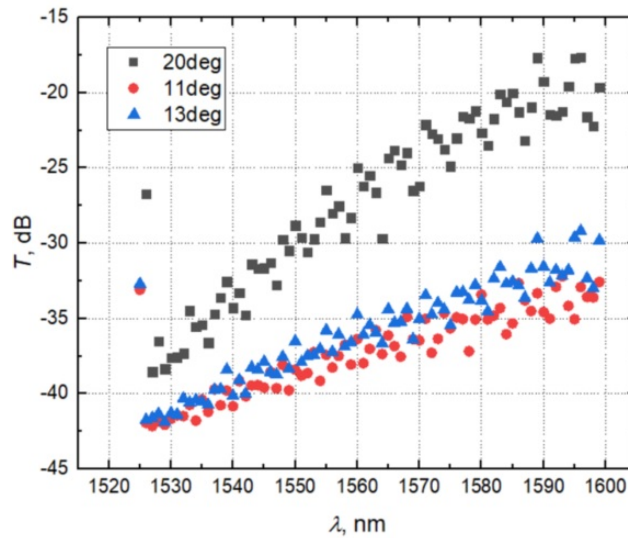
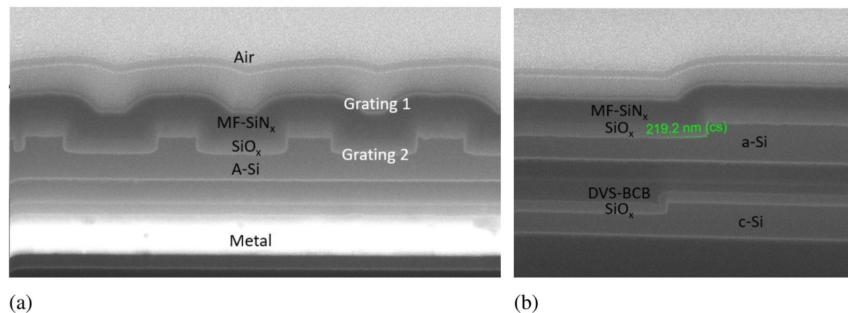


Figure 2.67: Transmission measurement results using different fiber angles.

The measurement results are depicted in Figure 2.67, with poor transmission at all the measured fiber angles. To better understand this result, we performed FIB cross-sections on the transfer printed coupons to explore if the printing interface was good enough or if the printing imperfections seen in Figure 2.59(c) would impact the quality of the light coupling to the coupon.

These cross-sections were made in the grating region and in the directional coupler region and are displayed in Figure 2.68. As one can see the grating couplers are printed well above the metal mirror and a clean printing interface is observed (Figure 2.68(a)). The same is observed for a directional coupler and the cross-section indicates the lateral printing misalignment of $\sim$220 nm (Figure 2.68(b)).



(a) (b)

Figure 2.68: Focused ion beam cross-sections of the transfer printed highly-efficient grating coupler on the SOI target substrate. Grating region with the indicated layers (a) and waveguide layers with the indicated layers and the misalignment in the lateral direction (b).

One of the possible reasons could be in the Figure 2.68(a) displayed the top MF-SiN$_x$, which was not planar (as shown in Figure 2.63(i)), but rather mimicked the topography of the grating, especially in the larger grating slit area. This created an additional apodized grating with the air-silicon nitride interface where the refractive index contrast was big. This grating modifies the phase front of the incoupled light. A simple solution to this problem was to spin-coat a $\sim$1.5 μm-thick DVS-BCB layer and cure it at 280^{o}C to planarize the top surface of the substrate thereby reducing the effect of the SiN$_x$ grating. After applying this solution, however, the transmission measurement results remained similar.

2.7.6 Conclusions and possible reasons for the poor transmission

In this section, we discussed the design, simulations, process development, release, and transfer printing results for the highly efficient grating couplers transfer printed onto a silicon-on-insulator target wafer. We patterned apodized gratings and directional coupler waveguides using e-beam lithography in the a-Si layer and exploited the Si(111) substrate for releasing the devices. We developed a sophisticated a-Si layer protection scheme using a combination of silicon oxide and nitride layers and released patterned grating devices using 28% KOH solution, which was gently steered and heated to 75°C. The released devices were suspended on the 12 μm narrowest point, staircase-shaped tethers, which broke at the correct points when the released devices were picked. We transfer printed these GCs on top of the SOI with the integrated metal mirror in a Si recess.

The transmission measurements, however, indicated a poor result of about -20 dB fiber-to-fiber, while the simulation results showed that transmission should

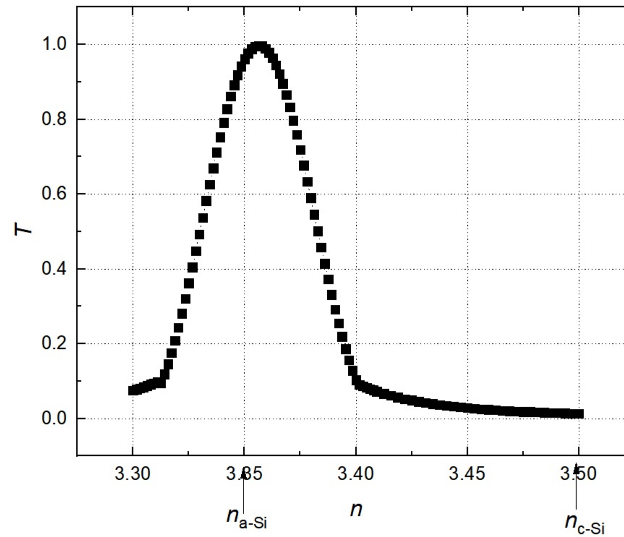


Figure 2.69: Simulation results of the directional coupler transmission dependencies on the amorphous silicon material refractive index.

yield no less than -1 dB per transition. A possible reason for this could be a poor design of the directional coupler as one can see about 5 dB ripples in the transmission spectrum. This can hint to poor index matching between top a-Si and bottom c-Si waveguides. The re-simulations of the directional coupler interface indicated high sensitivity of the directional coupler transmission to the refractive index value of the amorphous silicon material (see Figure 2.69). The refractive index of the a-Si material was chosen $n = 3.35$. It is the value of the low frequency a-Si deposited material, measured using elipsometry. The material we used in the experiment, however, was the optimized PECVD high frequency a-Si. It yields a uniform, good quality, pinhole-free layer at 180°C.

Before we continue to re-optimize the experiment, it is necessary to check the ellipsometry results for a better estimation of the refractive indices of high frequency a-Si at 1550 nm wavelength.

2.8 Conclusions

In this chapter we developed the process flow for releasing and transfer printing silicon germanium devices. An SOI release scheme was developed by under-etching the buried oxide layer, while the top device layers were protected through the use of amorphous silicon. By using an optimized triangular tether design, clean device picking and printing were demonstrated. We showed transfer printing alignment

accuracy better than ± 1 μm. We used this knowledge to transfer print passive silicon photonic devices on a silicon photonic target waveguide substrate. The coupling loss of a single interface was - 1.5 ± 0.5 dB for the adiabatic taper coupler at 1310 nm and - 0.5 ± 0.5 dB for the directional coupler at 1600 nm. Also, we demonstrated the micro-transfer-printing of high-speed silicon-germanium photodiodes on a silicon-on-insulator passive waveguide circuit. We obtained 0.66 A/W responsivity, open eye diagrams, and sub HD-FEC transmission at 50 Gbit/s. Finally, we discussed the design, simulations, process development, release, and transfer printing results for the high-efficiency grating couplers. We patterned apodized gratings and directional coupler waveguides using e-beam lithography in the a-Si layer and exploited the Si(111) substrate to release these. We transfer printed these structures onto silicon-on-insulator target wafers.

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3

Micro-Transfer-Printing InP/InGaAs Photodetectors

3.1 Introduction

Over the last few years, a tremendous amount of research effort has been devoted to developing efficient III-V-on-Si integration techniques to solve one of the major problems of silicon photonics: cost-efficient integration of a laser source on Si PICs. However, the range of III-V optoelectronic devices is much broader, and for some applications, III-V photodiode (PD) devices are indispensable. One of the biggest advantages of III-V PDs in comparison to monolithic Ge photodiodes is that III-V PDs allow for custom device dimensions and geometries, and engineered layer stacks for applications where, for example, wavelength duplexing, polarization-independent optical detection [1], or operation outside the classical telecommunication wavelength window [2] is required.

This chapter focuses on micro-transfer-printing of substrate-illuminated InP/InGaAs PDs on Si PICs. We begin the chapter by simulating the operation of substrate illuminated devices using grating couplers (GC). Next, we describe the process development of the fabrication, the release, and transfer-printing of arrays of substrate-illuminated III-V PDs. In the second part of the chapter, we focus on transfer-printing similar PDs for a telecom receiver application, namely a 4×25 Gbit/s tunable receiver, for both a single polarization and operating in a polarization-diversity mode. Static and dynamic characterization results for both receivers are presented.

Finally, we present important process development results of waveguide-coupled III-V photodetectors, after which the chapter is concluded.

3.2 Simulations of light absorption in a grating-coupled InP/InGaAs photodiode

Simulation of the light absorption in the III-V photodiodes is similar to the work described in [3]. The schematics of the simulated structure is depicted in Figure 3.1. The structure consists of the standard SOI with Si substrate, 2 μm buried silicon oxide, standard 220 nm Si waveguide, and a top 1.05 μm silicon oxide cladding. This layer incorporates both the top oxide layer (1 μm thick, typical in the imec silicon photonics passive platform) and spin-coated BCB (few 10s of nm) as both refractive indices at 1550 nm are closely matched.

The III-V photodetector layer stack is integrated on top of the SOI stack and consists of the bottom 300 nm n-InP layer, top 300 nm p-InP, and one micrometre intrinsic InGaAs absorption layer that is sandwiched in-between. The top 300 nm Au layer is deposited on top of the III-V layer stack, which acts as a p-metal electrode.

Using finite difference time domain (FDTD) software, we launched the fundamental transverse electric (TE) mode (in the 1500 - 1600 nm wavelength range) in the silicon waveguide, which encounters a diffraction grating coupler with a period of 628 nm, 50% fill factor and 70 nm etch-depth. We place the absorbed power monitor (P_{abs}) in the InGaAs absorbing layer to monitor the amount of absorbed light in the layer.

The intrinsic InGaAs layer is not a standard material in the simulation software, therefore using values in the literature [4] we estimated the absorption coefficient ($\alpha_{InGaAs}(\lambda)$) and refractive index (n) which are wavelength dependent. We hence calculated the imaginary refractive index ($k_{InGaAs}(\lambda)$) by

$$k_{InGaAs} = \frac{\lambda \alpha_{InGaAs}}{4\pi} \tag{3.1}$$

And the values of the InGaAs are depicted in Table 3.1.

The grating scatters the TE mode upwards and downwards (Figure 3.1). The upward scattered light passes through the top silicon oxide layer and n-InP layer and gets absorbed in the intrinsic InGaAs. The top metal layer reflects the unabsorbed light back to the InGaAs layer and the total absorption of the PD increases.

We studied this effect and Figure 3.2 compares the absorbed optical power versus the wavelength with the top metal electrode and without it. One can see that when no top electrode is present the absorbed optical power decreases with respect to the wavelength as the absorption coefficient estimated in Table 3.1 decreases with increasing wavelengths.

λ, nm	n	α, m^{-1}	k
1500	3.372	10^6	0.119
1510	3.373	9.5×10^5	0.114
1520	3.374	9×10^5	0.109
1530	3.375	8.5×10^5	0.103
1540	3.376	8×10^5	0.098
1550	3.377	7×10^5	0.086
1560	3.378	6.5×10^5	0.081
1570	3.379	6×10^5	0.075
1580	3.38	5.5×10^5	0.069
1590	3.381	5×10^5	0.063
1600	3.382	4.5×10^5	0.057

Table 3.1: Estimated InGaAs imaginary refractive index.

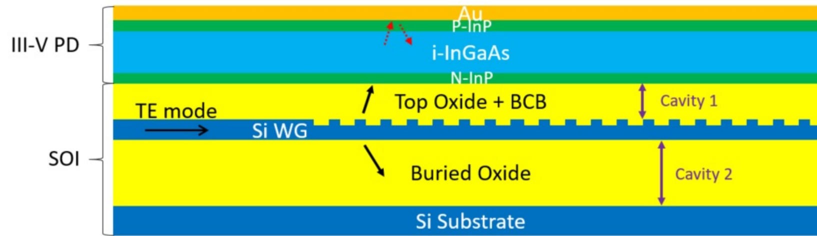


Figure 3.1: Simulated structure: III-V PD integrated on top of the silicon-on-insulator waveguide.

When we add the top Au layer into the simulation, higher absorption value in the InGaAs layer is estimated (4 - 5 %) comparing to the simulation without top Au layer at 1500 - 1575 nm wavelength window. However, starting from λ = 1575 nm this effect has much higher impact as smaller absorption coefficient at longer wavelengths causes less light to be absorbed by InGaAs, thus, higher fraction of light reflects back from the top of the metal electrode back to i-InGaAs.

Care has to be also taken when choosing the oxide thicknesses. Because of the index contrasts between silicon/InP and oxide layers, cavities are created on the top and on the bottom (Figure 3.1) what impacts the absorbed optical power fraction in the i-InGaAs.

It is clear that top & bottom silicon oxide thicknesses have to be chosen correctly to maximize the absorption and we simulated this effect. Figure 3.5(a) depicts the absorbed power versus the top oxide thickness (t_{top_oxide} = 0.25 - 2 μm) choosing different bottom oxide thickness (t_{bot_ox} = 1.5 - 2 μm) at λ = 1550 nm. One can see that the highest absorbed power fraction we obtain for 0.25 μm top

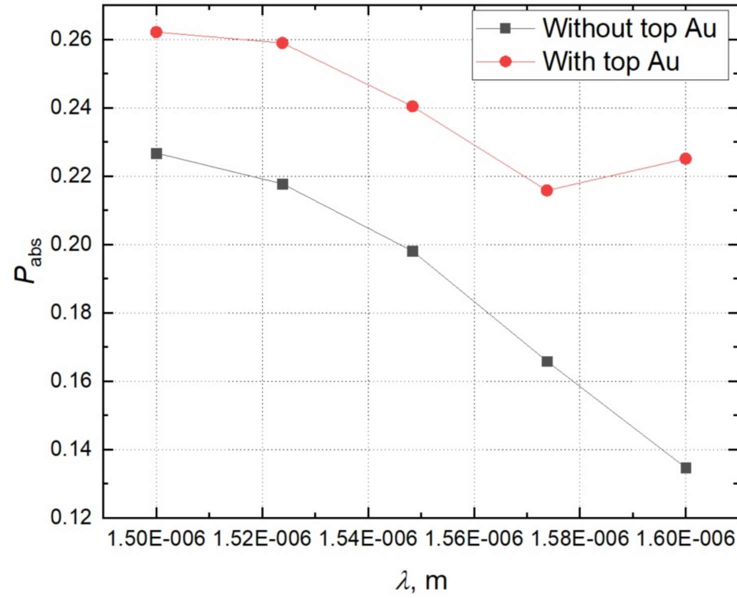


Figure 3.2: Absorbed optical power in the InGaAs intrinsic absorption layer, dependencies on the wavelength with the top Au electrode and removing the top Au electrode.

oxide. We choose the top oxide thickness of 0.25 μm and in Figure 3.5(b) we plot the absorbed power values over different bottom oxide thicknesses.The simulation shows that the bottom oxide thickness can impact $\sim$4% of absorbed optical power in the i-InGaAs. One can see a periodic behavior with a period of $\lambda/2n$ and a higher absorbed power value at t_{bot_ox} = 2 μm what is compatible with the SOI substrates used in this experiment.

3.3 Transfer-printing of in-house fabricated InP/InGaAs photodiodes

After becoming familiar with the operation principle of the grating-assisted photodetector, now we can focus on the fabrication, release, and transfer-printing of InP/InGaAs photodiodes. Using a III-V epitaxial material stack, one can fabricate a large array of compact photodiode devices in a dense array and then transfer print these devices to a silicon target chip in a sparse fashion. In this experiment, we will showcase this advantage of the micro-transfer-printing technique.

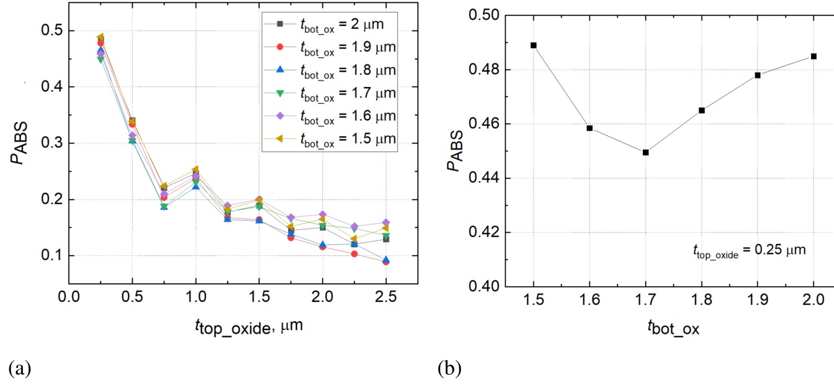


Figure 3.3: Absorbed optical power in the InGaAs intrinsic absoprtion layer dependencies on the top oxide layer thickness (a). Absorbed optical power in the InGaAs intrinsic absoprtion layer choosing the top oxide layer thickness of 0.25 µm and sweeping the thickness of the bottom oxide layer.

3.3.1 III-V layer stack

The layer stack is displayed in Table 3.2 and consists of material similar to the structure used in simulations. The biggest difference is that we included a 300 nm highly doped, low-absorbing InGaAs top layer for an improved metal contact. The p-i-n layer stack consists of an intrinsic 1 μm InGaAs absorbing layer sandwiched between InP p-type and n-type cladding layers. The key to successful transfer-printing is an additional bottom InGaAs release layer, which is sandwiched between the InP undercladding and the buffer.

Layer N.	Material	Thickness, nm	Doping	Function
1	InP	100	n.i.d	Cap
2	InGaAs	100	$> 1 \times 10^{19}$	p-contact
3	InGaAs	200	10^{19}	p-contact
4	InP	300	5×10^{17}	p-contact
5	InGaAs	1000	n.i.d	absorption
6	InP	240	10^{18}	n-contact
7	InP	60	n.i.d	n-contact
8	InGaAs	1000	n.i.d	release
9	InP	150	n.i.d	buffer
10	InP	–	n-type	substrate

Table 3.2: The InP/InGaAs photodiode material layer stack.

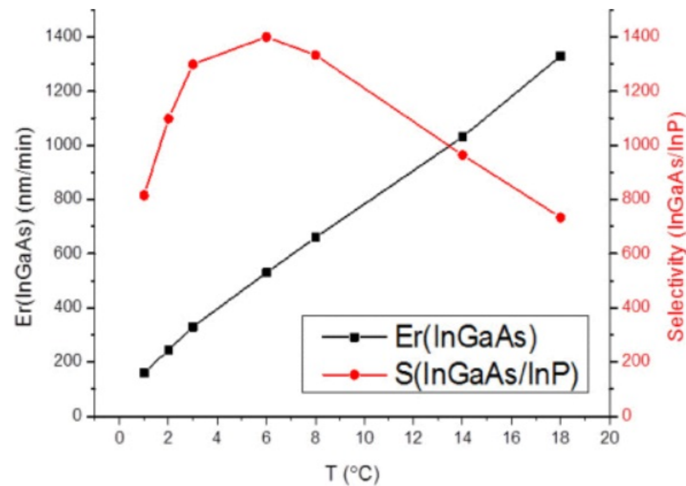


Figure 3.4: Etch rate (left hand side) and the selectivity of InGaAs etch versus InP (right hand side) dependencies on temperature for etching using an aqueous $FeCl_3$:H_2O solution [5].

3.3.2 $FeCl_3$ release etch

The goal of this work is to etch the InGaAs release layer using an aqueous $FeCl_3$:H_2O (1 mg : 2 ml) solution. The selectivity of InGaAs versus intrinsic InP is reported in the literature, and is depicted in Figure 3.4. The etch rate for the InGaAs increases linearly with the temperature; however, an important factor is the etching selectivity of InGaAs versus InP. It yields the highest value (over 1500) at 6^oC [5] [6].

It is important to mention, however, that InGaAs etching using $FeCl_3$ is anisotropic and several examples of underetching 60×60 μm InGaAs patches are depicted in Figure 3.5 whereby InGaAs is etched directionally, under an angle of 45° with respect to the major flat. A recent study showed superior underetching quality using an InAlAs release layer [7] with the same $FeCl_3$:H_2O solution. The isotropic etching and further improved etching selectivity (up to four times higher) decreases the etching time and the flatness of the bottom of the underetched coupon is improved.

$FeCl_3$ is a metallic black powder and, when mixed in water, it leaves a residue on the bottom of the beaker. Moreover, etching at lower temperatures leads to an increased amount of precipitation of the $FeCl_3$ which tends to create more debris on the surface of the III-V chip. As this is undesirable, the $FeCl_3$ is filtered before use.

A comparison of the surface of the InP/InGaAs chip when released in the unfiltered and filtered $FeCl_3$:H_2O solution is depicted in Figure 3.6(a) and (b). One can see the difference between the quality of the surfaces. Filtering the $FeCl_3$:H_2O using a funnel and paper filters is a crucial step leading to cleaner release etch and

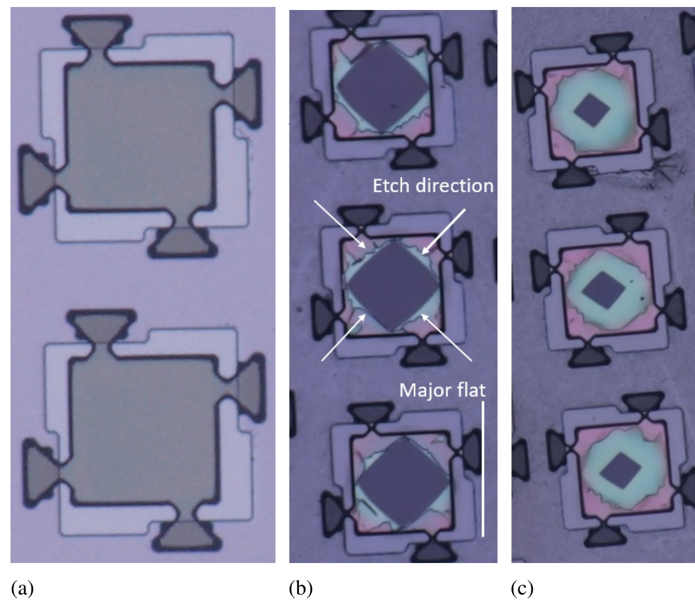


Figure 3.5: Example of etching the InGaAs release layer using a $FeCl_3$:H_2O solution. (a) Before the etching, (b) after 20 minutes of etching, (c) after 35 minutes of etching.

increasing the release yield.

3.3.3 Tethers for InP/InGaAs photodiodes

One of the most important developments to enable the transfer-printing of III-V PDs is the tether system. These have to be strong enough to keep the released devices in place after the release etch, provide encapsulation to protect the device layers from aggressive etchant penetration, and, moreover, break in a well defined point, creating no debris, when the PDMS stamp picks the device.

The schematics we will be pursuing in this work are similar to the one depicted in Figure 1.25. The tether material will be deposited on top of the device and release layers and patterned accordingly to anchor the III-V devices to the substrate. The simplest material to choose for this matter is photoresist (PR). It is a straightforward, directly lithographically patternable soft material that can protect the top InGaAs device layers from $FeCl_3$:H_2O penetration. Besides, soft photoresist material properties enable a clean tether break in the narrowest points, and, when printed, the photoresist is easy to remove using an RIE oxygen plasma for about 40 minutes.

This is demonstrated in Figure 3.7. A $\sim$3 μm thick Ti35E photoresist was used (Figure 3.7(a)) [8]. After releasing the devices using $FeCl_3$:H_2O, the PDs become

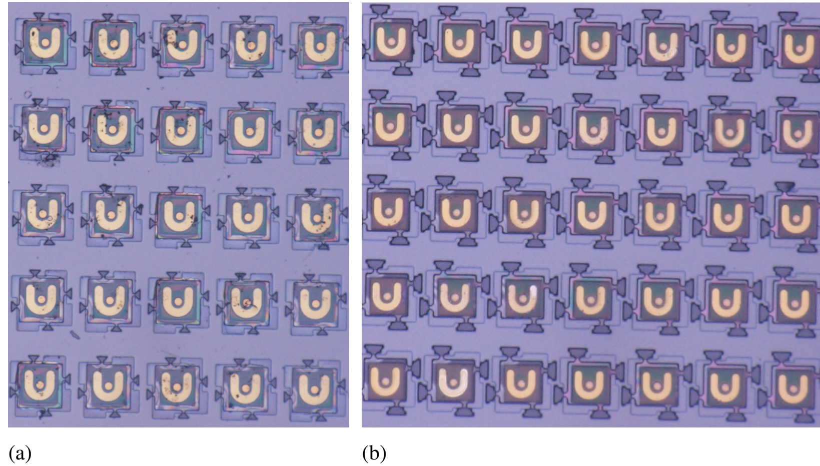

(a) (b)

Figure 3.6: (a) Surface of the chip after releasing using an unfiltered $FeCl_3$ solution. (b) The surface of the chip after releasing using the filtered $FeCl_3$ solution.

free suspended membranes as can be seen from the colourful coupons in Figure 3.7(a). After picking the devices with the printer, the tethers break at the narrowest points, leaving a clean bottom InP buffer layer depicted in Figure 3.7(b). After being transfer-printed on the silicon photonics target wafer, cleanly broken tethers are visible in Figure 3.7(c), and a coupon with the photoresist tethers removed can be seen in Figure 3.7(d) after 40 minutes of oxygen plasma treatment.

There are several important considerations when designing and fabricating tethers. The narrowest tether point has to be strong enough to keep the coupon in place when released. We noticed that using 6 - 10 μm wide and 6.5 μm long tether points (Figure 3.8(a)) work well. It is also very important to put the weakest point of the tether well inside the release layer pattern. The underetching of such tether design is demonstrated in Figure 3.8(b). By placing the narrowest point too close to the edge of the release layer pattern the tethers become too weak to hold the coupon in place, and the majority of coupons collapse on the source; this is demonstrated in Figure 3.8(c). By extending the release layer pattern to the tether breaking point, we can increase the release yield from $\sim$10% to $\sim$83%.

Another important problem to consider is the photoresist adhesion to the substrate. In order to improve the photoresist adhesion, it is important to spin-coat the photoresist immediately after patterning the release layer. Figure 3.9 shows that virtually all the released PDs lost their attachment during the release etch when the sample was left overnight, and the photoresist was spin-coated on the next day. This might have happened because the InP substrate layer gets covered with the a thin oxide layer over a longer period of time, which eventually impacts the

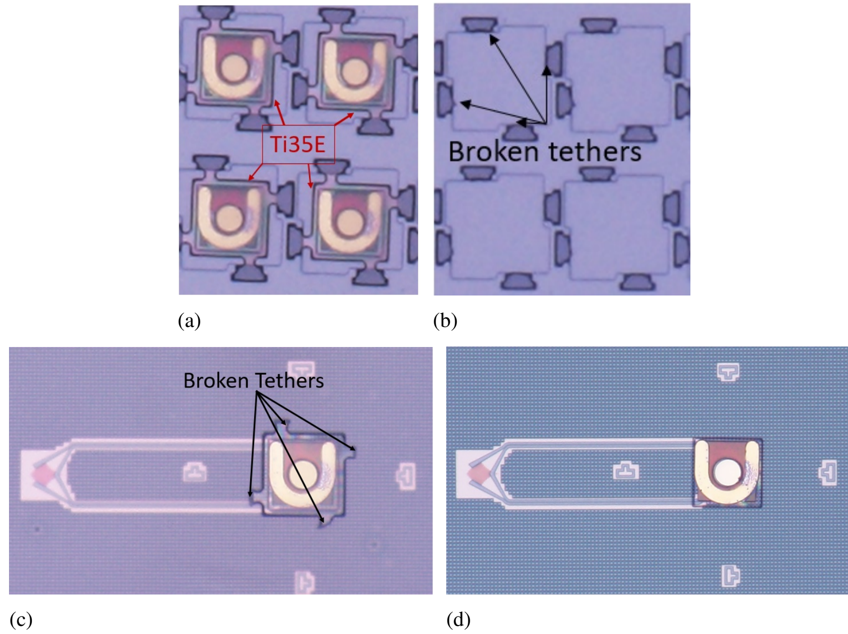


Figure 3.7: (a) Tethers patterned on the source wafer, (b) tethers broken on the source wafer when the coupon is picked up, (c) example of a coupon with broken tethers on the target wafer, (d) photoresist tethers removed from the target wafer after oxygen plasma treatment.

adhesion of the photoresist.

Typically ∼30 seconds ICP dry etching can solve this problem before spin-coating the photoresist layer.

3.4 Experiment

After we understood the release chemistry and tether properties, we focused on the transfer printing experiment. The main advantage of the transfer-printing is the parallel integration of the III-V components, that also do not require large bond pads, as needed for flip-chip integration. This enables a time- and material-efficient integration of III-V devices on 200 mm or 300 mm silicon photonics wafers.

In the next section, we will discuss the transfer-printing of arrays of III-V substrate-illuminated C-band photodiodes on silicon photonic waveguide circuits using a 2×2 array stamp. However, first, we will focus on the design and fabrication of source and target wafers.

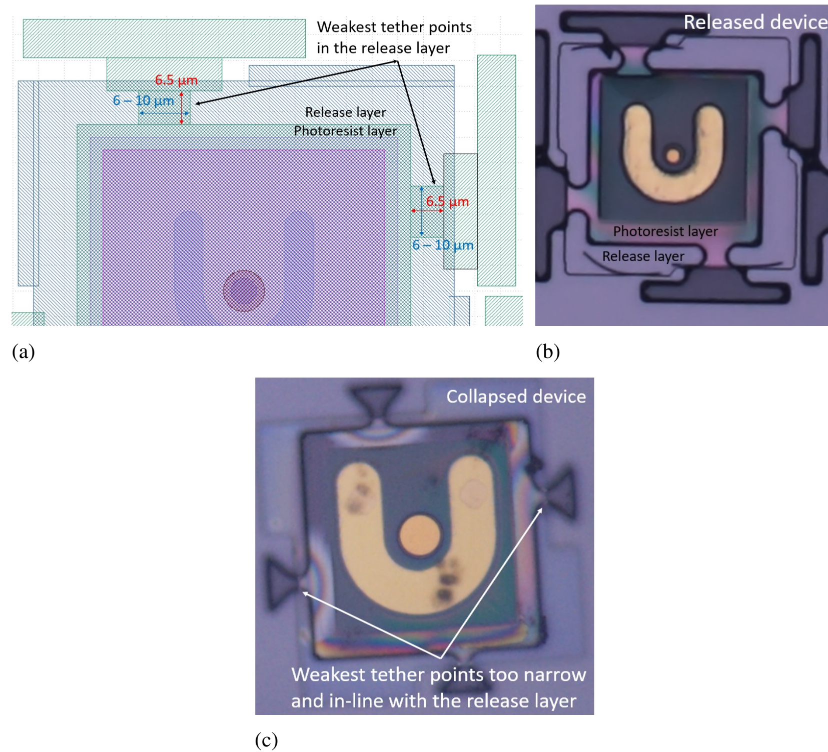


Figure 3.8: (a) Schematic design of the tether pattern, (b) device fabrication and release, this device is held in place by 4 tethers; (c) device released and collapsed on the source wafer using weak tethers.

3.4.1 Mask design of the target wafer

The silicon photonic target wafers were fabricated in imec's passive technology platform using a 220 nm thick silicon device layer, a 1 μm thick top oxide cladding (the oxide was not thinned down) and 70 nm, 150 nm and 220 nm etch depths [9]. The schematic layout of the target waveguide circuit is displayed in Figure 3.10. The circuit consists of arrays of 6$\times$14 C-band input and output grating couplers, placed with a 500 μm / 250 μm pitch in x- and y-direction. The top 42 grating couplers are 1D grating couplers (4.5 dB single mode fiber-to-chip loss per coupler at 1550 nm) and the bottom 42 are 2D grating couplers (6 dB single mode fiber-to-chip loss per coupler at 1550 nm). Tetris-brick alignment markers were added to aid to the high printing alignment accuracy as will be discussed later.

Figure 3.9: Example of bad adhesion of the photoresist tether to the source substrate.

3.4.2 Mask design of the source wafer

On the III-V source wafer, 55 μm $\times$55 μm square photodiodes with 23 μm circular apertures were designed in a dense array on a pitch of 100 μm and 125 μm in x- and y-direction respectively (Figure 3.11). The photodiodes are to be released and transfer printed using a 2$\times$2 arrayed with posts spaced by 500 μm in x-direction and 250 μm in y-direction, what matches the pitch on the target.

3.4.3 III-V PD fabrication: final process flow

III-V photodiode fabrication was performed in the Ghent University cleanroom and the full sequence is schematically depicted in Figure 3.12. We start with the full layer stack (Figures 3.12(a)) and used pure hydrochloric acid (HCl) wet etching for about 20 seconds to remove the InP cap layer (Figure 3.12(b)). Then, circular 21 μm diameter Ti/Au p-contacts were deposited (Figure 3.12(c)). By depositing and patterning a 150 nm thick plasma-enhanced chemical vapor deposition (PECVD) mixed frequency silicon nitride (MF-SiN$_x$), the p-metal was protected (Figure 3.12(d)), using the layer as a hard to mask to define the 23 μm circular mesa by etching it using inductively coupled plasma (ICP) using CH_4/H_2

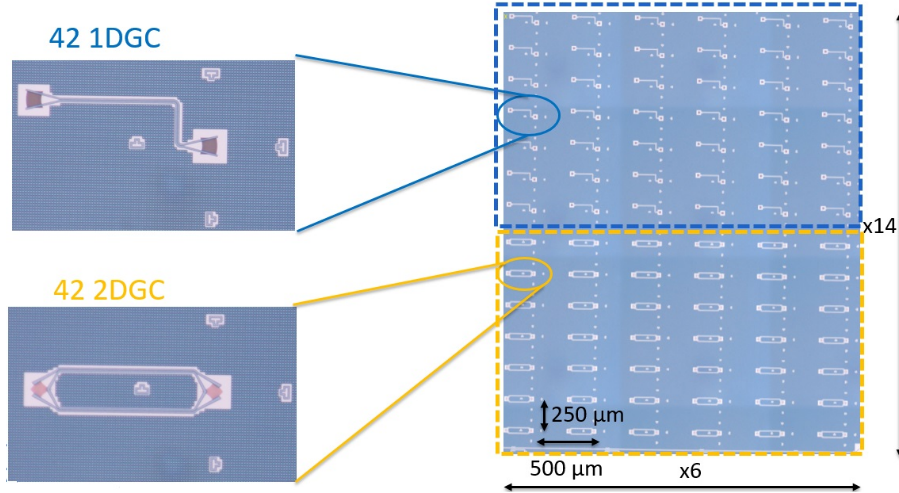


Figure 3.10: Schematic layout of the target wafer.

for 40 min. The etch was stopped on top of the n-InP layer and the residual intrinsic InGaAs was removed by dipping the sample into a Piranha 1:1:10 solution for 30 seconds (Figure 3.12(e)). Then, the U-shape Ni/Ge/Au n-contacts (Figure 3.12(f)) and an additional 150 nm of MF-SiN$_x$, which was patterned in square patterns of 50 $\times$ 50 μm was defined (Figure 3.12(g)). This MF-SiN$_x$ pattern was used as a hard mask to etch the n-InP layer and stop on the InGaAs release layer using a combination of ICP dry etching and HCl:H$_2$O 1:1 wet etching for 45 seconds (Figure 3.12(h)). $\sim$1.5 μm divinyl-siloxane-bis-benzocyclobutene (DVS-BCB) passivation was spin-coated, cured at 280°C and patterned (Figure 3.12(i)). Afterwards the release layer was patterned using ICP (Figure 3.12(j)) and the device was encapsulated using a $\sim$3 μm thick photoresist. After patterning the photoresist tethers (Figure 3.12(k)) the release was performed by placing the devices in an FeCl$_3$:H$_2$O (1 mg : 2 ml) solution at 6°C for about 55 minutes to underetch the InGaAs release layer and to make the devices free hanging, anchored to the substrate by the photoresist tethers (Figure 3.12(l)). The top view of a fabricated and released 20 $\times$ 7 array of InP/InGaAs photodiodes is depicted in Figure 3.13. As can be seen one coupon flew off from another part of the chip and redeposited on the array.

For the transfer priting we used square 60 μm $\times$ 60 μm PDMS posts in a 2x2 array on a pitch of 500 by 250 μm. Devices are picked when the stamp is laminated with the released devices and the tethers break at their weakest points. Devices are attached to the stamp (Figure 3.12(m)). For printing, the stamp is brought in close proximity of the target wafer and the devices are first aligned with respect to the

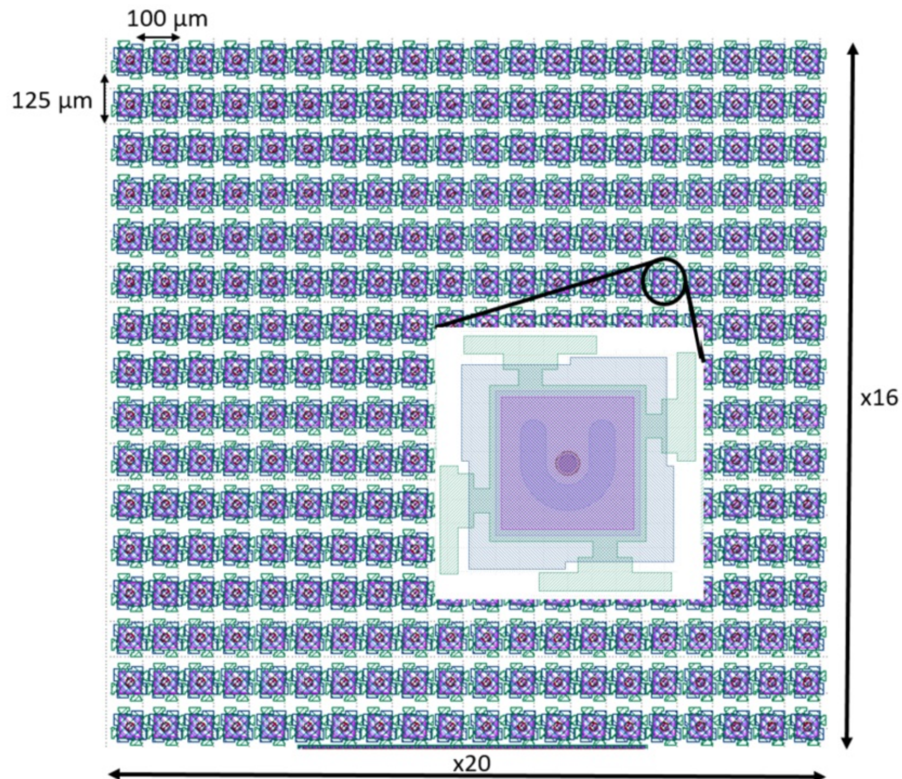


Figure 3.11: Schematic layout of the III-V source wafer.

target wafer (Figure 3.12(n)). Laminating the device against the ~50 nm thick DVS-BCB spin-coated target wafer and slowly moving the stamp in the vertical direction (Figure 3.12(o)) the devices stay attached to the target substrate.

3.4.4 Transfer printing in an automated mode

In this experiment transfer printing has been done in an automated mode with the arrayed 2×2 PDMS stamp with the pitch of 500×250 μm and the principle is schematically displayed in Figure 3.14(a). Before the transfer printing, the source substrate was inspected and one can program the uTP-100 transfer printing software to skip the positions of collapsed or broken devices [10] (marked 3 in the Figure 3.14(a)). Figure 3.14(b) shows the source substrate after the transfer printing. 84 devices were picked using the 2×2 arrayed printing and 80/84 devices were printed, clearly showing bad PDs in red. The 4 failed devices were populated on the target wafer by picking and printing using a 1×1 PDMS stamp (shown in

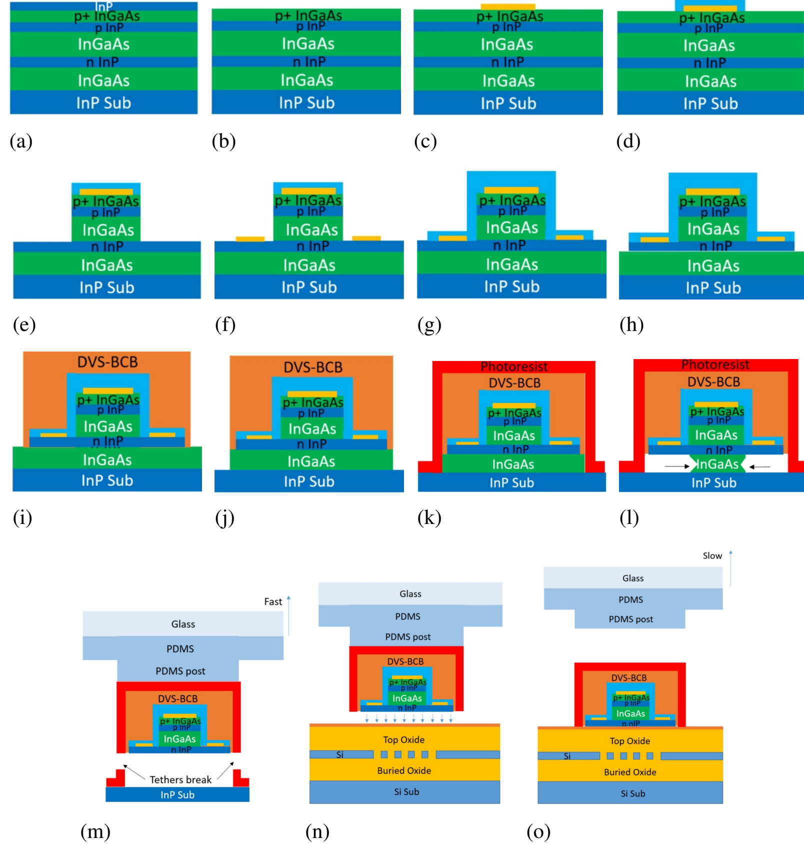


Figure 3.12: Schematic illustration of III-V photodiode fabrication and release process.

blue in Figure 3.14(b)), as a rework procedure.

3.4.5 Post-processing

After transfer printing arrays of devices on the target wafer, the photoresist encapsulation was reflown at 140°C for 10 minutes to improve III-V device adhesion and was then removed using O_2 RIE plasma (Figure 3.15(a)). The DVS-BCB was fully cured at 280°C after which a new thick $\sim 3\ \mu$m DVS-BCB layer was spin coated and cured at 280°C again (Figure 3.15(b)). Then using RIE (SF_6/O_2 gas mixture for $\sim$ 6 minutes), the DVS-BCB layer was etched back and the p- and n-electrode were opened (Figure 3.15(c)). After this $\sim$1 μm thick Au ground-signal-ground (GSG) tracks were defined for electrical device characterization (Figure 3.15(d)).

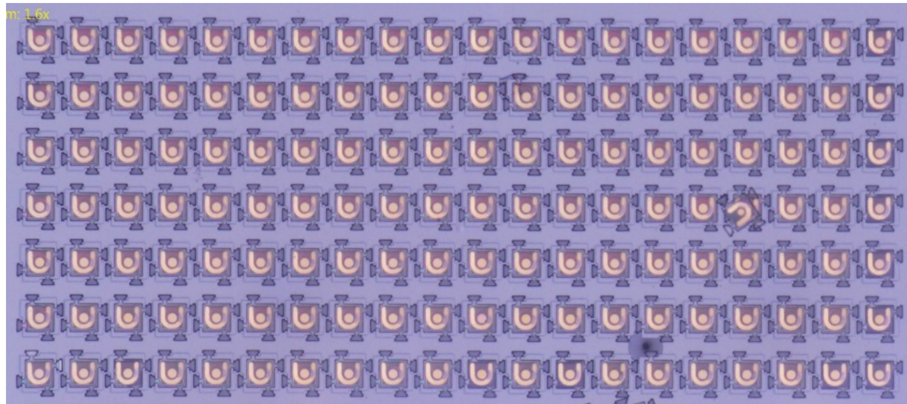
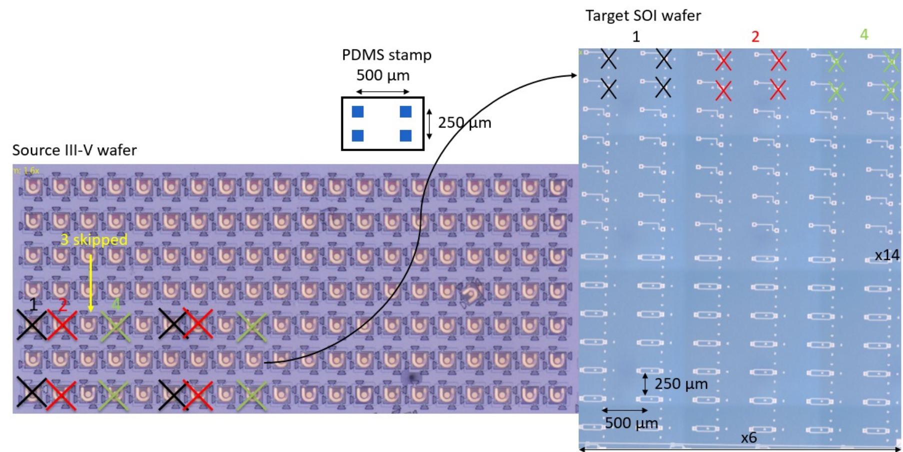
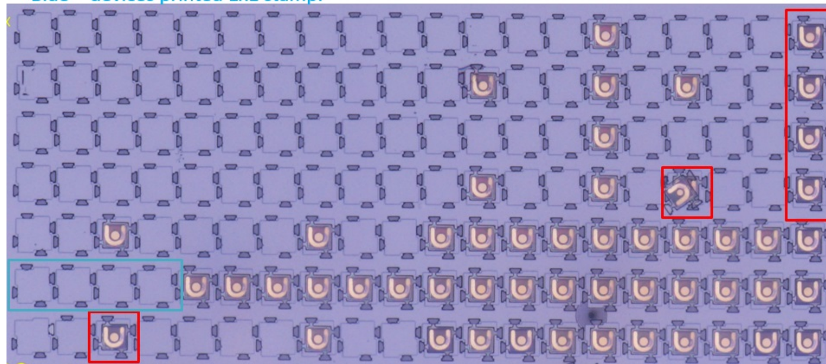


Figure 3.13: Top view of the fabricated and released 20×7 array of C-band photodiodes.

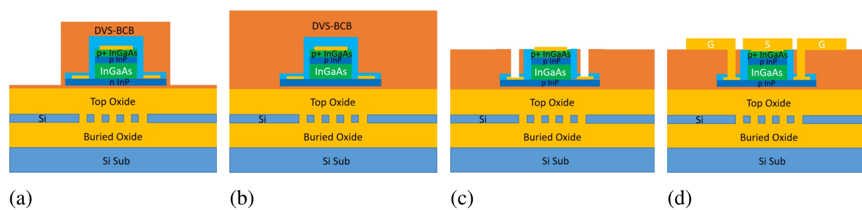


(a)



(b)

Figure 3.14: (a) Schematic representation of array transfer printing. Position 3 indicates a collapsed devices, which is therefore skipped. (b) Top view of the source wafer after completing the transfer printing. Collapsed or broken devices are shown in red which were skipped by the 2×2 array stamp. The blue rectangle indicates devices that were picked and printed in 1×1 mode.



(a) (b) (c) (d)

Figure 3.15: Schematic illustration of the post-processing of the target wafer.

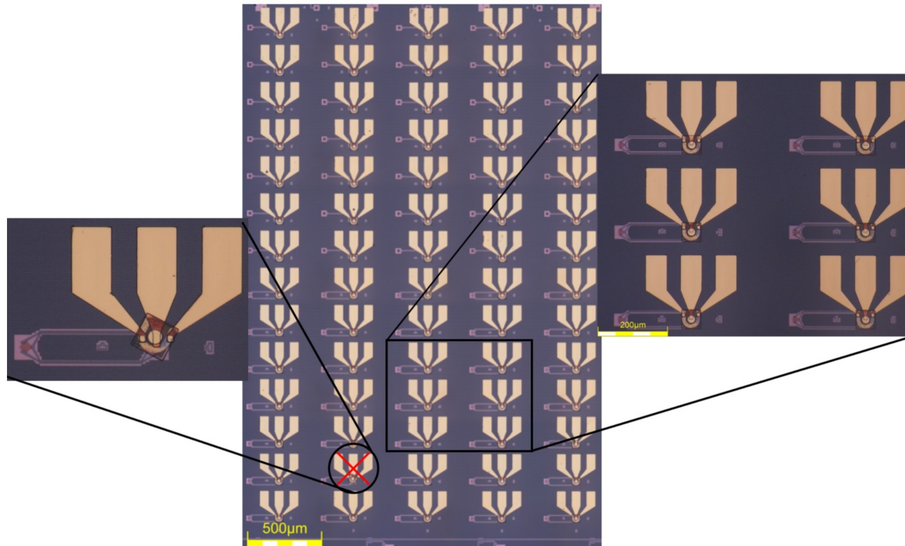


Figure 3.16: Transfer printed bottom-illuminated devices after completing the post-processing. The inset on the left depicts the only device transfer printed with poor alignment accuracy.

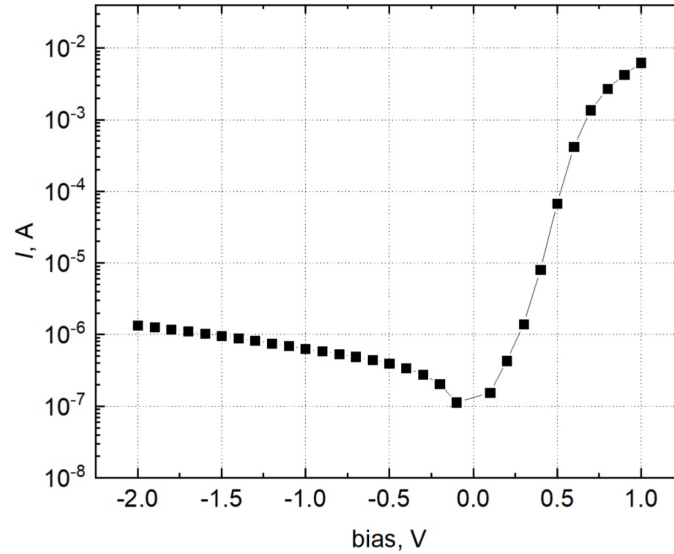
The target chip, after completing the post-processing is depicted in Figure 3.16. All devices were printed and metalized. One device on row 13, column 2 transfer printed with a clear noticeable rotational misalignment on the target (see the left inset in Figure 3.16). Characterization of all array-printed devices helped to determine the alignment accuracy. A more detailed study of alignment accuracy of array-printed devices however was not conducted but could be beneficial for the future experiments.

3.5 Characterization

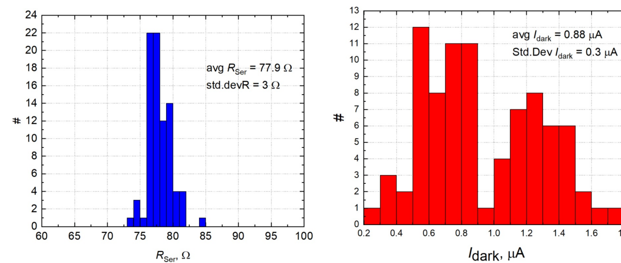
All the transfer printed devices were measured and the data was statistically analyzed by calculating the average and the standard deviation of responsivity, series resistance, dark current and bandwidth.

3.5.1 IV characteristics

The IV characteristics of all 84 integrated devices were measured using DC probes and a Keithley 2400 current-voltage source. A typical IV of one device is shown in Figure 3.17(a). Series resistance was calculated by measuring current at 1 V and at 0.5 V and the voltage/current difference then divided. All 84 devices show



(a)



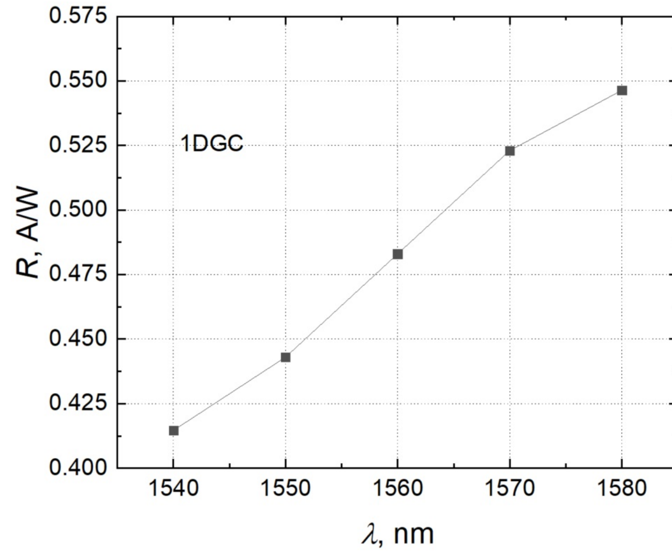
(b) (c)

Figure 3.17: (a) A typical IV curve of one transfer printed photodiode; (b) histogram of the series resistance of all 84 transfer printed photodiodes; (c) histogram of the dark current of all 84 transfer printed photodiodes.

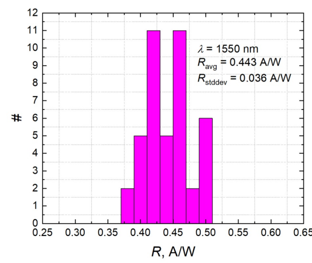
comparable IV characteristics with an average series resistance of 79 Ω (standard deviation 3 Ω) and an average dark current of 0.9 μA at -1V bias (standard deviation 0.3 μA). The histogram of series resistance and dark current are plotted in Figure 3.17(b) and (c) respectively.

3.5.2 Responsivity for devices integrated on 1DGCs

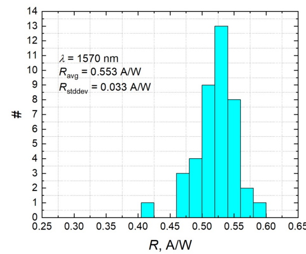
Using a Santec TSL510 tunable C-band laser and a 10 degree tilted single mode fiber, light was coupled into the silicon photonics chip (using a 1D or 2D grating coupler). Responsivity was measured by coupling optical power to the waveguide,



(a)



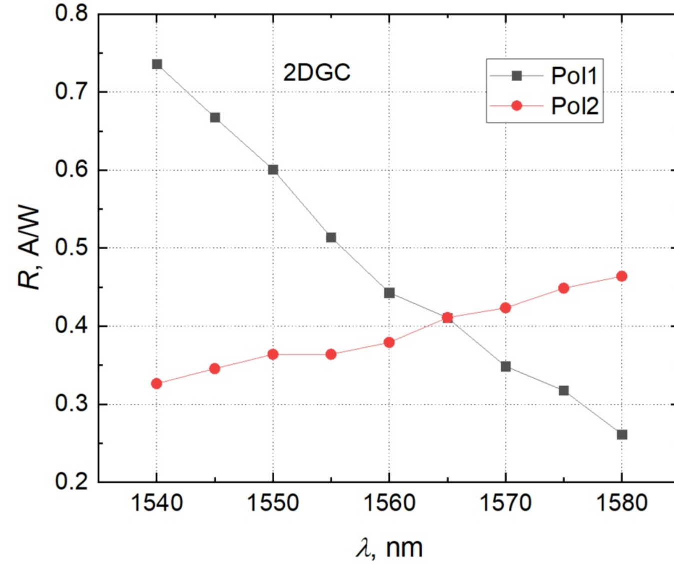
(b)



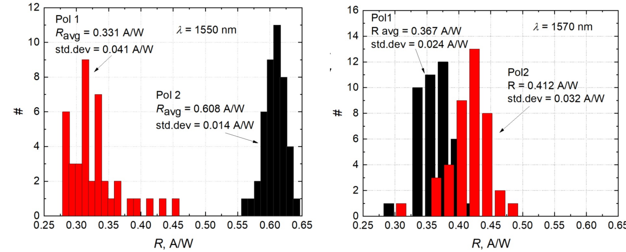
(c)

Figure 3.18: (a) Waveguide-referred responsivity for a typical device transfer printed on a 1D grating coupler. Histograms of the waveguide-referred responsivity at 1550 nm (b) and at 1570 nm (c) for the 42 photodiodes transfer printed on a 1D grating coupler.

measuring the photocurrent at the output. The results are presented cancelling the contribution of the grating. The waveguide-referred responsivity of the 42 devices integrated on 1D grating couplers and its dependence on wavelength for a typical device is presented in Figure 3.18(a). The responsivity increases with wavelength what is not in line with simulations. Figure 3.18(b) and (c) display the histograms of waveguide-referred responsivities of all 42 devices integrated on a 1D grating coupler at 1550 nm and 1570 nm respectively. Possibly higher responsivity values can be obtained thinning down the top oxide layer.



(a)

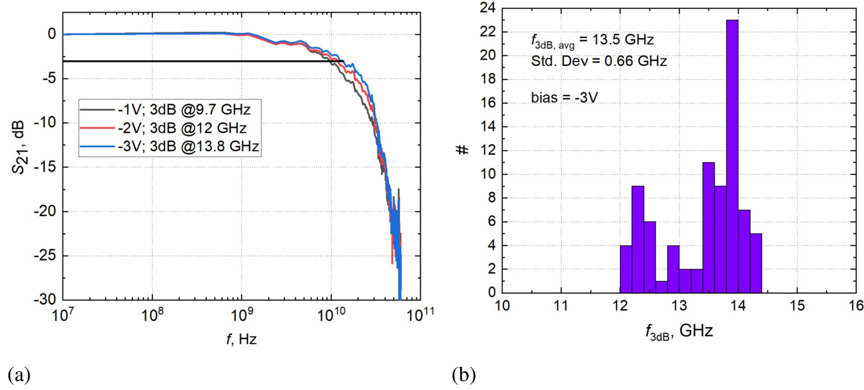


(b) (c)

Figure 3.19: (a) Waveguide-referred responsivity for a typical device integrated on 2D grating coupler measured for both states of polarizations. (b) histogram of responsivities at 1550 nm at polarization state 1 and 2; (c) histogram of responsivities at 1570 nm at polarization state 2.

3.5.3 Responsivity for devices integrated on 2DGCs

The waveguide-referred responsivity for photodiodes integrated on 2D grating couplers measured for two polarization states corresponding to the maximum and minimum response (denoted as Pol1 and Pol2) and its wavelength dependence is shown in Figure 3.19(a). This behavior is not well understood at the moment and numerical simulations are necessary to understand these dependencies better. Figure 3.19(b) and (c) show the histogram for the waveguide-referred responsivity at 1550 nm and 1570 nm for polarization states 1 and 2 respectively for all 41 devices



(a) (b)

Figure 3.20: (a) S_{21} curve measured for one representative printed photodiode at different bias voltages. (b) Histogram of 3dB bandwidths of 83 photodiodes, measured at -3V bias.

(the device printed with the noticeable misalignment was not taken into account).

3.5.4 Small signal measurement

The small signal response was measured using a vector network analyzer (VNA) using a Santec TSL510 tunable C-band laser and Mach-Zehnder modulator - similar to the schematics depicted in Figure 2.37. The S_{21} parameter for different photodiode bias is displayed in Figure 3.20(a). The histogram of the 3dB bandwidth of all the 83 transfer printed devices (3V reverse bias) is shown in Figure 3.20(b). The 3 dB bandwidth spans between 12 and 14.4 GHz with an average value of 13.5 GHz.

3.5.5 Conclusions

In this section of this chapter we demonstrated parallel transfer printing of substrate-illuminated III-V C-band photodetectors. We developed the photodiode fabrication and release process, as well as the proper tethering of the InP/InGaAs photodiodes. We exploited the automated picking and printing and a rework procedure to demonstrate a high yield arrayed transfer printing above 98%. This demonstration showcases the advantages of transfer printing technology for scalable III-V-on-Si integration.

3.6 Micro-transfer-printing of low dark current photodiodes for III-V/Si WDM receivers

Over the years a number of passive optical components have been developed on the silicon photonics platform to realize efficient tunable filters for wavelength-division multiplexing (WDM), monolitically integrated with high-speed active devices (Si modulators, Ge photodiodes, etc.). However, as explained previously the complete process involves over 30 mask level processing steps in a fab, which results in a significant turn-around time [11].

This is where the micro-transfer-printing approach can effectively come into play. In this case, III-V semiconductor devices are densely patterned on a III-V source wafer and released from its source wafer, allowing for a structured elastomeric PDMS stamp to selectively pick up the devices and print them on a passive SOI target wafer realizing potentially sparse integration in a massively parallel way. This allows to restrict the silicon photonics processing to passive silicon waveguide circuitry and adding the active functionality through transfer printing.

In this subsection we present the transfer printing of substrate-illuminated III-V photodetectors on a passive silicon photonic integrated circuit to realize a 4×25 Gbit/s receiver using a thermally tunable micro-ring demultiplexer circuit. Two types of receiver circuits will be discussed: a single-polarization (1D) with double ring (2RR) filter and polarization diversity receiver with single ring (1RR) filters.

3.6.1 WDM tunable ring filter receiver design

Both passive silicon circuits are designed in imec's passive technology platform decribed above and in [9]. The platform comprises a 220 nm thick silicon device layer, 70 nm, 150 nm and 220 nm etch depths and a 1 μm thick top oxide cladding.

3.6.1.1 Single-polarization receiver design and III-V photodiodes

The single polarization 4-channel receiver circuit is depicted in Figure 3.21. The light couples into the chip using a one-dimensional grating coupler. Each channel consists of a double ring filter which enables a flat-top filter response which will be tuned using integrated microheaters. The design and properties of the rings are more thoroughly described in [12]. Each microring is selected to have a coupling length of 9 μm, and a radius of 5 μm. The gaps are chosen to be 205 nm between the waveguide and the ring, and 340 nm between the rings. The ring resonators have a free spectral range of 11 nm with a full-width at half-maximum of 1.2 nm which is depicted in Figure 3.22.

In this experiment, an externally designed and fabricated C-band photodiode design was adapted to enable transfer printing (i.e. the inclusion of an InAlAs release layer below the p-i-n layer stack). Photodiodes with 10 μm aperture were

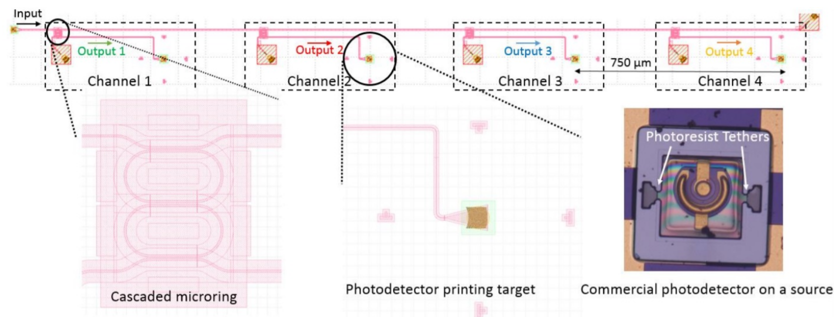


Figure 3.21: Schematic of the single polarization 4 channel tunable ring receiver, zooming in on the double ring filter used, the landing site for the photodetectors and a released photodetector on the III-V source wafer.

realized on a 75×75 μm coupon, which were released from the III-V substrate by underetching the InAlAs release layer, while being anchored to the substrate using photoresist tethers. Each photodiode is transfer printed on top of the output grating coupler of each individual channel of the WDM receiver. Tetris-brick alignment markers were added to aid the high-alignment accuracy micro-transfer-printing. Each photodetector target site is spaced on a 750 μm pitch for the possibility of wire-bonding with a trans-impedance amplifier (TIA) array in a later stage.

3.6.1.2 Dual-polarization receiver design

The 4-channel polarization diversity receiver design is depicted in Figure 3.23. The light couples into the chip using a 2D grating coupler (-6 dB coupling efficiency at 1550 nm, 40 nm 3dB bandwidth), which is etched 70 nm deep. It splits the two polarization states at the input grating coupler and also combines both polarizations at the transfer-printed photodiode. Similarly, thermally tuned 1RR add-drop ring resonator filters (fully etched) were used for wavelength demultiplexing. This receiver makes use of 8 identical rings with 5 μm radius and 9 μm directional coupler length [12]. The gap between the bus waveguides and the ring is chosen to be 295 nm. The Q-factor of the ring resonators is 4200 (3dB bandwidth of 370 pm) and their free-spectral range (FSR) is 10.7 nm. On-resonance the insertion loss of the ring resonators is 0.5 dB. The resonance wavelength of the rings is tuned through the integration of micro-heaters.

3.6.2 Post-processing

Post-processing schematics are displayed in Figure 3.24. We start by processing the micro-ring spiral-shaped heaters. On the SOI with the top oxide layer (Figure 3.24(a)) we deposit ∼350 μm length, 2 μm wide and 100 nm thick Ti

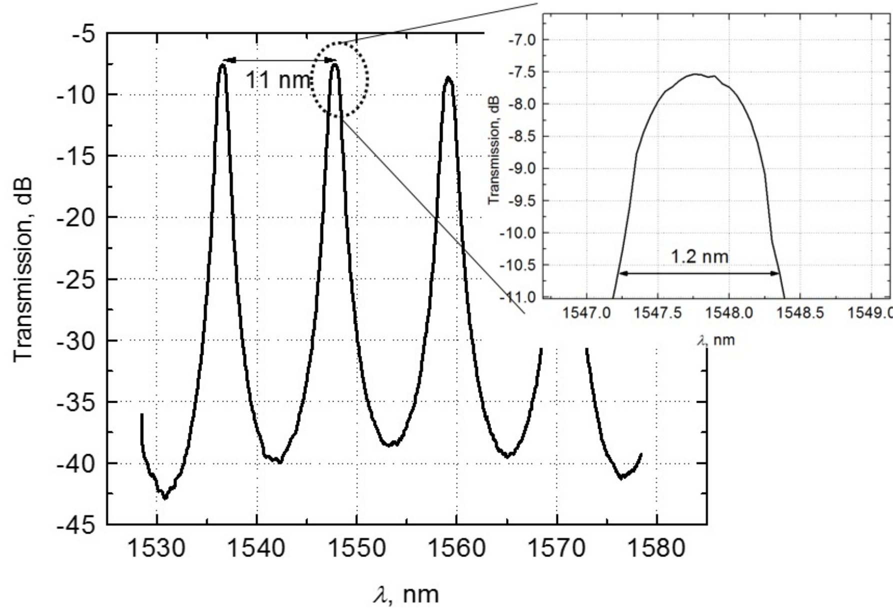


Figure 3.22: Fiber-to-fiber transmission spectrum of the double cascaded microring used in the experiment.

spiral-shaped wires locally on the micro-rings. Then we deposit 800 nm thick gold wires to connect the Ti heaters (see the inset on Figure 3.25) and form the DC contact pads (Figure 3.24(b)). In the second post-processing part the above described photodetectors were transfer printed onto the grating couplers at each channel output. We spin-coat a 50 nm thick DVS-BCB adhesive bonding agent, which was partially cured at 180°C (Figure 3.24(c)) and transfer print the detectors using the schematics we described in the previous sections (Figure 3.24(d)). After the transfer-printing, the top photoresist is removed by placing the sample for ∼35 minutes in an oxygen plasma (Figure 3.24(e)). Afterwards a new ∼4 μm thick layer of DVS-BCB is spin-coated and fully cured at 280°C (Figure 3.24(f)). Afterwards, the DVS-BCB is etched back using SF_6/O_2 to access the photodetector electrodes (Figure 3.24(g)) and thick (∼1 μm) Au is deposited to form GSG contact pads and the contact pads for the heaters (Figure 3.24(h)). Figure 3.25 shows the top-view of the single-polarization and dual-polarization receiver channel 1 after finishing the post-processing.

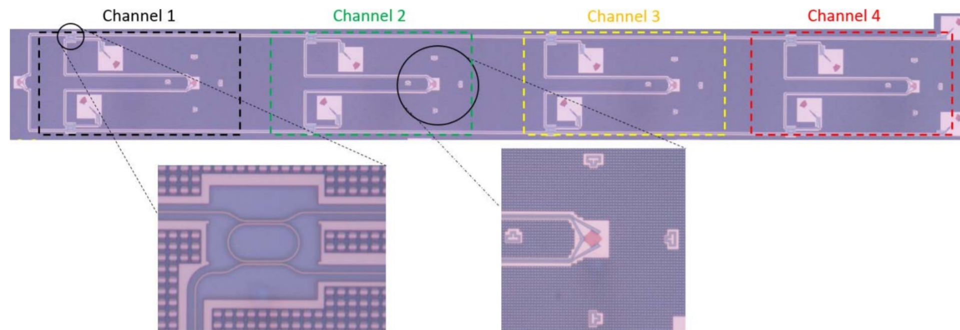


Figure 3.23: Microscope image of the passive 4-channel polarization multiplexed receiver circuit with a zoom-in on a ring filter and a 2D grating coupler to interface with a transfer printed photodiode.

3.6.3 Characterization

Both of the receivers were characterized both statically and dynamically. Static characterization includes the IV curve of the transfer printed PD and the responsivity dependencies on wavelength for a single-polarization and polarization-diversity receiver. Next we will focus on a small signal characterization and large signal characterization both for the single polarization and for the polarization diversity receiver.

3.6.3.1 IV characteristics

A typical IV curve of the transfer printed photodiode is depicted in Figure 3.26. The dark current of the device is about 20 nA at -2 V bias, while the series resistance is $\sim$4 Ω.

3.6.3.2 Responsivity

Using a Santec TSL-510 C-band tunable laser (TL) the waveguide-referred responsivity was measured for each channel for the polarization-diversity receiver. The resonance wavelength of the ring resonators in both arms of the polarization diversity circuit were aligned by applying a DC voltage on the integrated microheaters. 2.5 nm channel spacing is obtained. The result is displayed in Figure 3.27(a). A responsivity beyond 0.40 A/W from 1540 nm to 1585 nm for channels 1, 2 and 3 and above 0.30 A/W for channel 4 is obtained, increasing with the wavelength. The slightly lower responsivity of the 4-th channel is attributed to the off-resonance insertion loss of the ring resonators of channel 1-3.

Polarization dependent losses were estimated by measuring the received photocurrent versus the coupled optical power in the waveguide at the wavelengths of

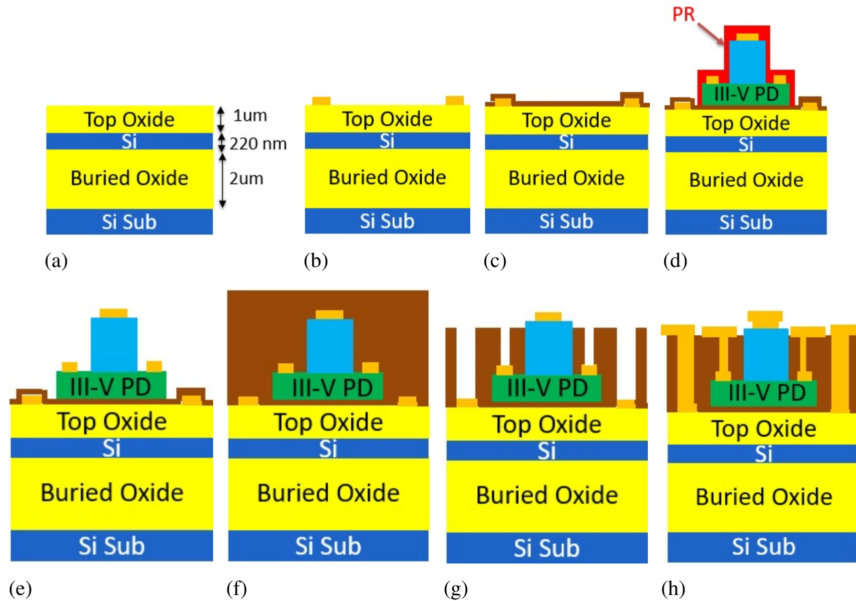


Figure 3.24: Post-processing schematics.

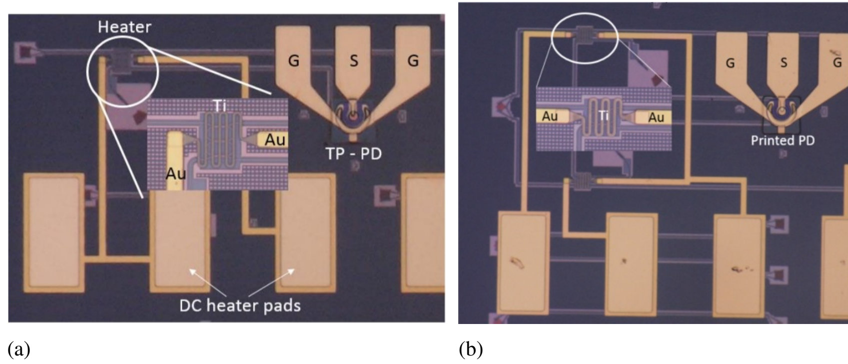
1551.18 nm, 1553.68 nm, 1556.18 nm and 1558.68 nm for each channel respectively. After measuring the maximum photocurrent value (polarization state 1) the polarization controller position was changed to obtain the minimum photocurrent value (polarization state 2) not changing the position of the fiber. The result is displayed in Figure 3.27(b). An average polarization dependent loss (ratio of the responsivity for the two polarization states) of 2 dB is estimated.

3.6.3.3 Small signal measurements

Small-signal measurements were carried out to assess the bandwidth of the transfer printed photodiodes, using a VNA. The measurement schematics are similar to the one depicted in Figure 2.37. We measured an S_{12} curve for the single-polarization receiver channel 1. No heater was used to tune the resonance of the filter. The result is depicted in Figure 3.28. A 3dB bandwidth of 8 GHz is measured for the transfer printed photodiodes.

3.6.3.4 Large signal measurement: single-polarization receiver

To verify the performance of the receiver, large-signal measurements were performed for both receivers for every receiver channel. The block diagram for the single-polarization measurement is depicted in Figure 3.29. An arbitrary wave-



(a) (b)

Figure 3.25: A microscope image of one receiver channel after post-processing. (a) single-polarization receiver; (b) dual-polarization.

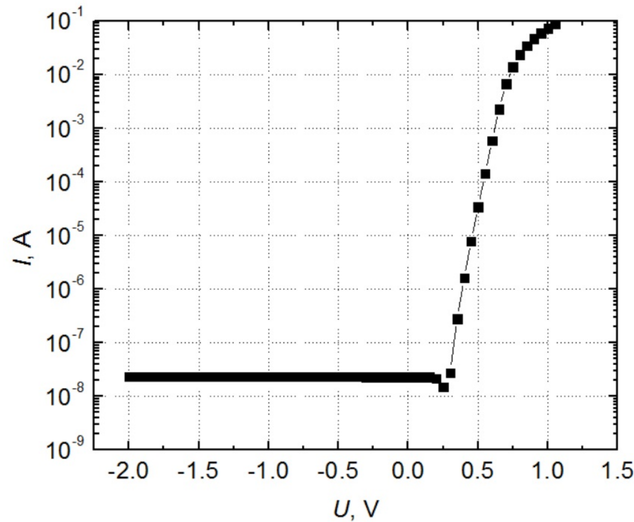
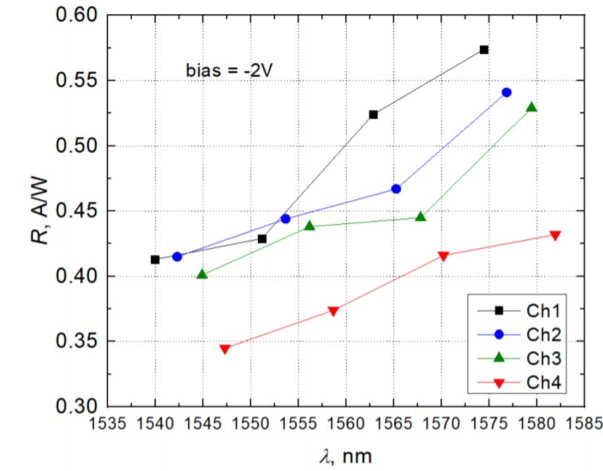
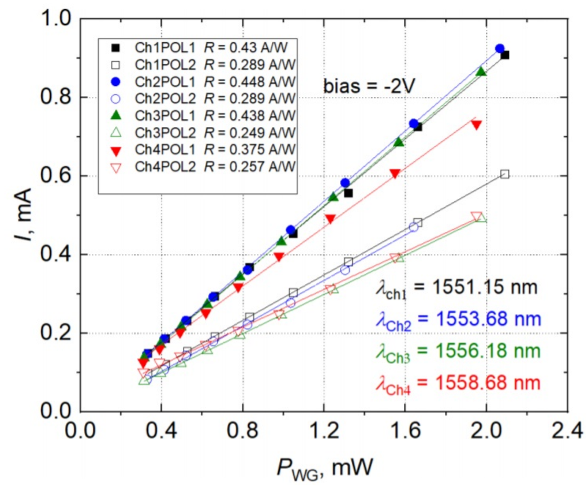


Figure 3.26: Typical IV curve of the transfer-printed III-V photodiode.

form generator (AWG) is used to generate a non-return-to-zero (NRZ) pseudo-random-bit-sequence (PRBS) with a pattern length of 2^9-1. A root-raised cosine (RRC) filter, and a peak-to-peak voltage of 7 V, by adding an RF amplifier, is generated. This signal is applied to the $LiNbO_3$ modulator at 25 Gbit/s. The photodiode was biased by -1.5 V DC voltage and the eye diagrams were observed using an oscilloscope. By applying a separate DC voltage on the heaters, the individual resonance wavelengths of the micro-rings were tuned and eye diagrams at all four channels were measured.



(a)



(b)

Figure 3.27: (a) Waveguide-referred responsivity measurement as a function of wavelength (-2 V bias) for all 4 channels of the receiver. (b) Photocurrent as a function of waveguide-coupled power for the 4 channels and for the two states of polarization resulting in maximum and minimum signal (-2 V bias). The ratio of the responsivity yields the polarization dependent losses.

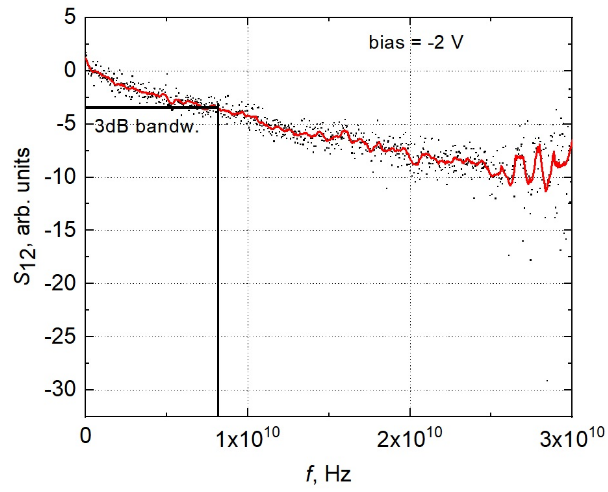


Figure 3.28: Small signal measurement for the transfer printed photodiode.

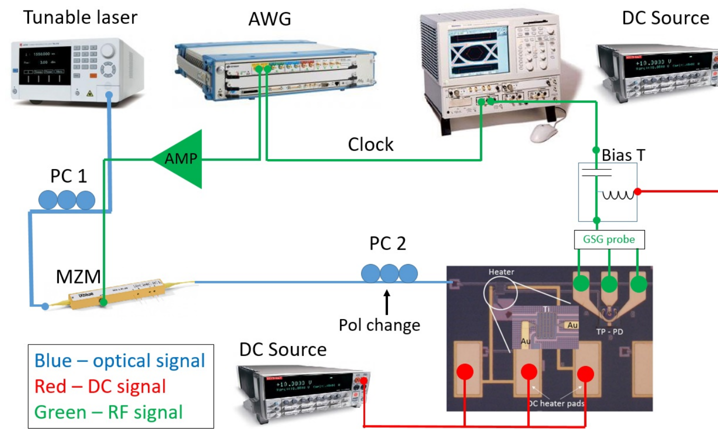
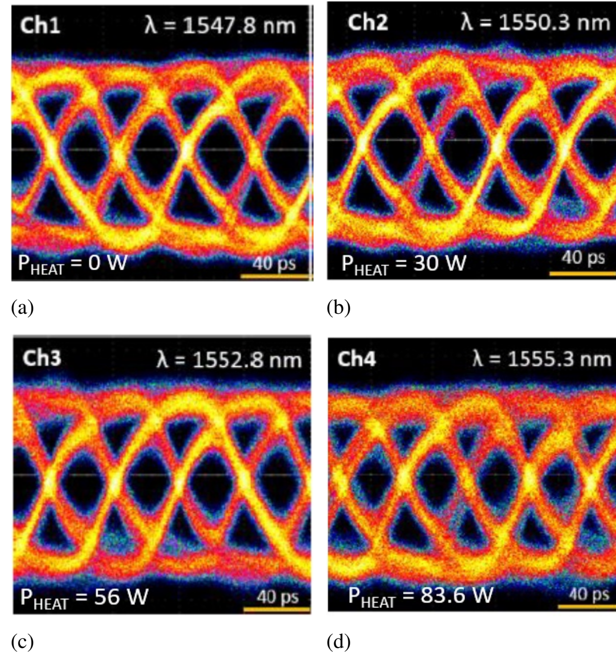


Figure 3.29: Large signal measurement schematics for a single-polarization receiver with transfer-printed photodiodes.



(a) (b)

(c) (d)

Figure 3.30: Eye diagrams of single-polarization receiver with transfer printed photodiodes on each channel at 25 Gbit/s by tuning the resonance of the micro-ring. The applied electrical power on the micro-ring heaters is indicated.

Figure 3.30 shows open eye-diagrams at 25 Gbit/s for every channel. The ring resonator resonances were tuned to achieve a channel spacing of $\Delta\lambda = 2.5$ nm. By applying 83.6 mW to the last heater on channel 4, a maximum resonance tuning of 7.5 nm was achieved, which corresponds to a tuning efficiency of about 11 mW/nm.

Using channel 1, eyes at different wavelengths were measured. Figure 3.22 shows the flat top response by the cascaded ring filter. One can see that while tuning the resonance wavelength from 1547.7 nm (Figure 3.31(b)) to 1548.1 nm (Figure 3.31(c)), the eye remains wide open. By tuning the laser wavelength to 1537.4 nm (Figure 3.31(a)) and to 1538.7 nm (Figure 3.31(d)), the filter transmission edges are reached and the eye starts to close.

3.6.3.5 Large signal measurement: polarization-diversity receiver

The large signal measurement schematics for the polarization diversity receiver are displayed in Figure 3.32. In comparison to Figure 3.29 the optical part consisting of the TL + MZM is additionally connected to an erbium-doped fiber amplifier (EDFA) generating a fixed 15 dBm optical input power to the receiver chip (with-

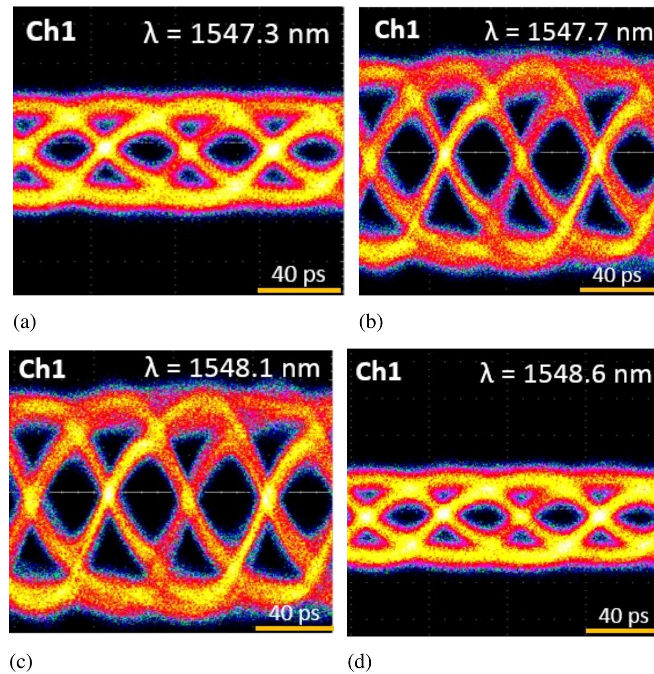


Figure 3.31: Eye diagrams on channel 1 of single-polarization receiver with transfer printed photodiodes of channel 1 at 25 Gbit/s tuning the laser wavelength. No voltage applied to the micro-ring heater.

out optical attenuation). The RF part is similar to the single-polarization receiver measurement: an AWG drives the MZM by applying a PRBS RRC filtered signal with a pattern length of 2^7-1 at 25 Gbit/s. The eye-diagrams of the four channels were measured by probing the devices and using a Tektronix CSA8000 oscilloscope. Because the receiver comprises of two tunable rings, two separate voltage sources are used to tune each ring filter individually.

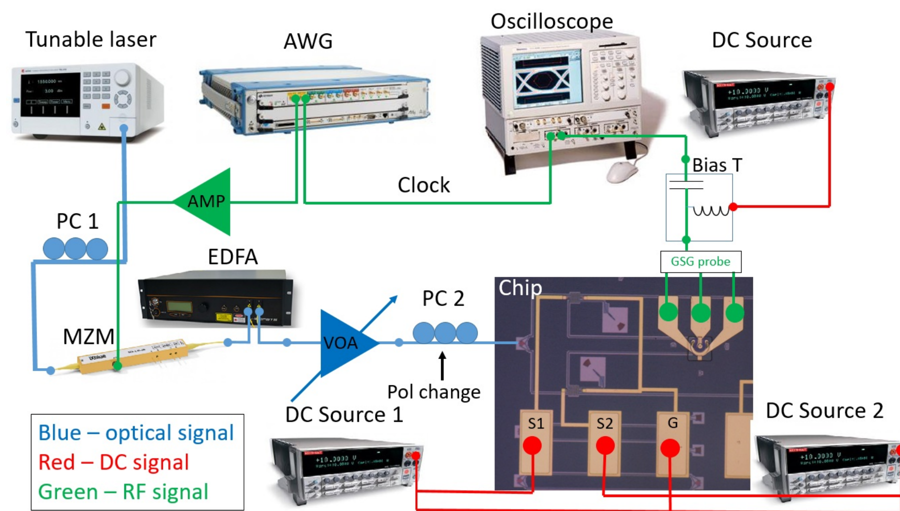
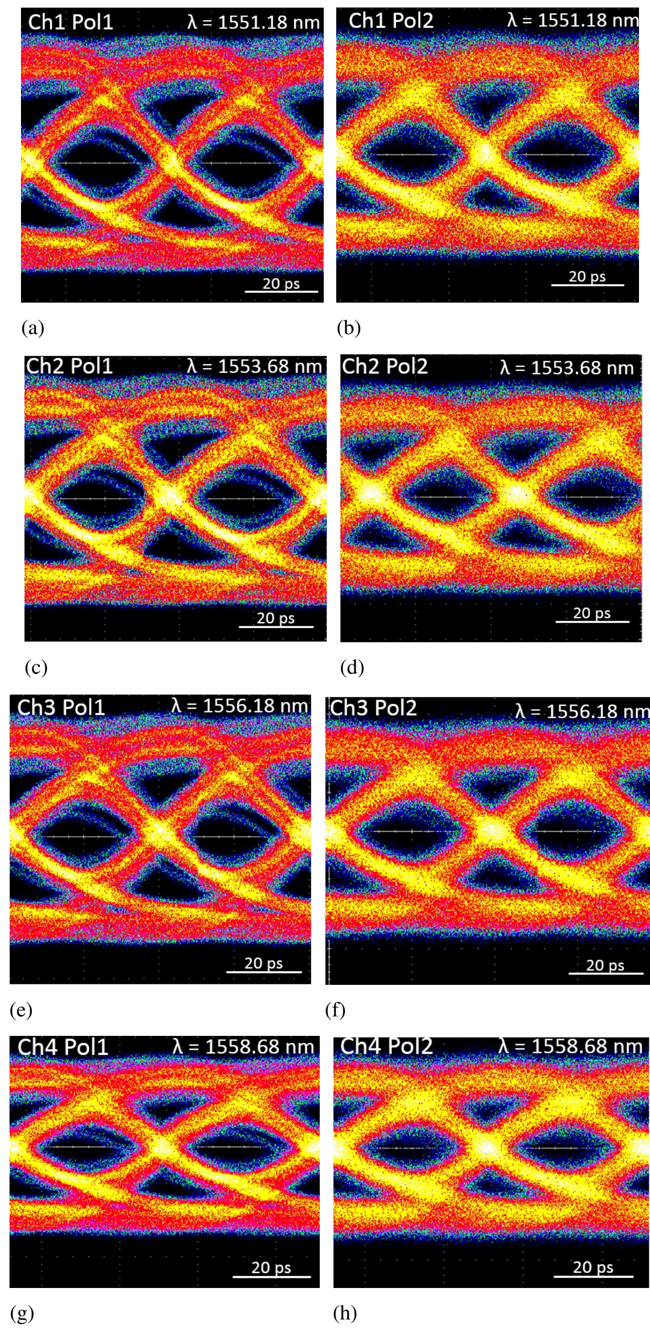


Figure 3.32: Large signal measurement schematics for polarization-diversity receiver with transfer-printed photodiodes.



(a) (b) (c) (d) (e) (f) (g) (h)

Figure 3.33: Eye diagrams of each channel at 25 Gbit/s for both polarizations by tuning the resonance of every micro-ring. In the left column eyes for polarization 1 are displayed, in the right column eyes for polarization 2. Heaters were tuned to obtain 2.5 nm channel spacing.

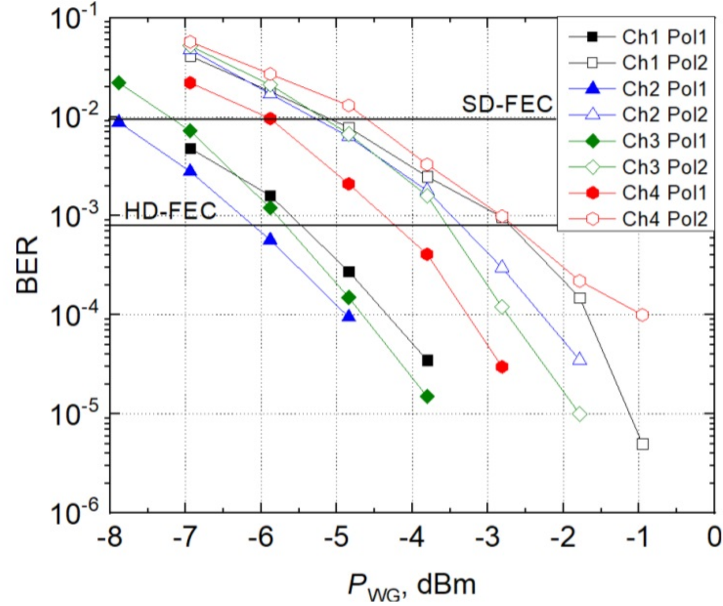
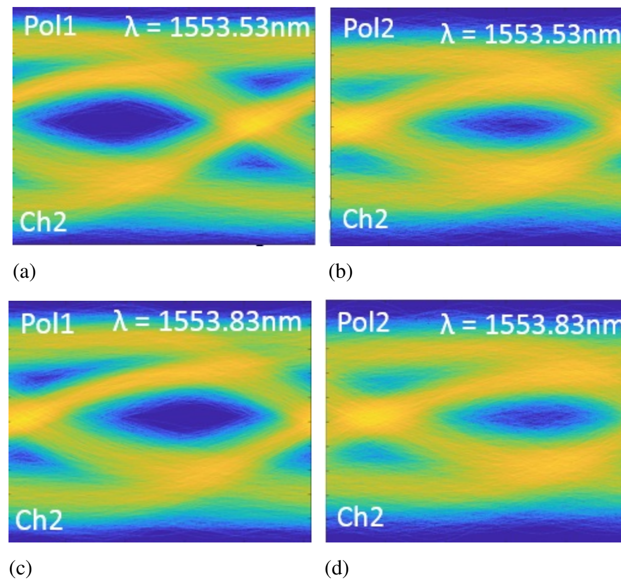


Figure 3.34: Bit error rate dependencies on the optical power in the waveguide at 25 Gbit/s operation for each channel of the receiver for both polarization states.

Open eye diagrams were measured for all 4 channels (at wavelengths of 1551.18 nm, 1553.68 nm, 1556.18 nm and 1558.68 nm respectively) and for both polarization states as shown in Figure 3.33. Next, we added a variable optical attenuator (VOA) to the optical link and a Keysight Real-Time Scope to measure the bit-error rate (BER) curves for each channel and for both polarization states. Figure 3.34 shows that at 25 Gbit/s transmission below the hard-decision forward-error correction (HD-FEC) threshold is obtained at about -5.5 dBm average waveguide referred input power for channels 1, 2 and 3 and -4.25 dBm for channel 4 for the polarization state 1. A power penalty of about 2 dB is obtained for the other polarization state.

Using channel 2 the laser wavelength (1553.68 nm) of the channel was detuned to reach the 3dB transmission edges of the filter. The eye diagrams for both polarizations were measured and displayed in Figure 3.35. Because the filters are single add-drop rings, the bandwidth of the channel is $\Delta\lambda$ = 0.3 μm. At the filter transmission edges polarization state 1 yields an open eye, while for polarization state 2, the eye is less open because of 2.5 dB polarization dependent losses (PDL).

BER measurements depicted in Figure 3.36 compare the operation at the channel 2 resonance wavelength and the detuned operation at the 3 dB transmission edge of the channel. The result proves that operation below HD-FEC for both



(a) (b) (c) (d)

Figure 3.35: Eye diagrams at 25 Gbit/s operation for detuning the resonance wavelength to reach the 3dB transmission edge of channel 2. In the left side eyes of polarization 1 are depicted. On the right hand side eyes for polarization 2 are depicted.

polarization states can be obtained.

3.7 Waveguide-coupled photodiodes

To achieve very high-speed operation, waveguide-coupled photodiodes (WGPDs) are indispensable components of optical receivers. The photodiode we aim to fabricate exploits the highly efficient grating coupler to couple the light in from the tilted fiber and a waveguide interface with the evanescent coupling scheme to the absorption layer.

During this PhD work, the fabrication and micro-transfer printing of WGPDs was attempted. However, in view of time, the complete fabrication was not finished. Thus, in this subchapter, we discuss the main findings of the process development for fabricating waveguide coupled photodiodes. This work was conducted together with Fabio Pavanello, who contributed with numerical simulation results.

3.7.1 Mask design

The photodiode structure is schematically displayed in Figure 3.37. The photodiodes are fabricated from the same III-V epitaxial material stack described in Table

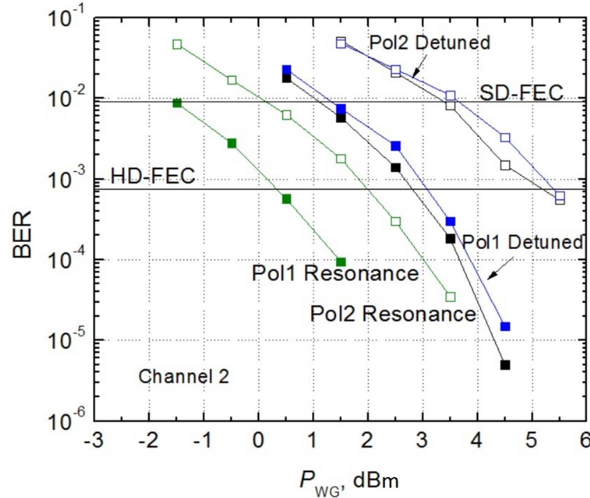


Figure 3.36: Bit error rate dependencies on optical power in the waveguide at 25 Gbit/s operation. Channel 2 on-resonance bit error rate compared with the detuned resonance for both states of polarization.

3.2. In this case we focus on the integration of a waveguide-coupled III-V photodiode on an underlying transimpedance amplifier. The schematic design of the WGPD is displayed in Figure 3.37(a). The waveguide trench and the grating are formed by etching 120 nm into the 300 nm n-InP layer. The light couples to the PD from the fiber using a grating coupler (GC). Fundamental TE mode coupling will be pursued using a grating coupler period of 649 nm with a 71% fill factor (FF). The simulated coupling efficiency for the fundamental TE mode coupling between the tilted fiber and the grating is about 80%. The WGPDs are to be transfer printed onto a silicon target substrate (mimicking the BiCMOS TIA die) that has a metal mirror and a SiO_x/DVS-BCB spacer layer. Locally, in the grating coupler printing area, the metal mirror is defined in a recess. The key part of the photodiode is the narrow, deep-etched mesa where the light is absorbed. In order to absorb the coupled light, a tapered absorption layer is formed, with a taper tip of 200 nm, tapering to 1 - 2 μm over a length of 20 to 50 μm (Figure 3.37(a)). 3 μm wide n-metal contacts are added to the sides of the mesa.

3.7.2 Fabrication: Main challenges

The design depicted in Figure 3.37 indicates that electron beam (e-beam) lithography must be used for the fabrication of the narrow structures, such as the 200 nm wide taper tip and the grating coupler for the waveguide-coupled PD. Two main challenges are identified in this work and are schematically displayed in Figure

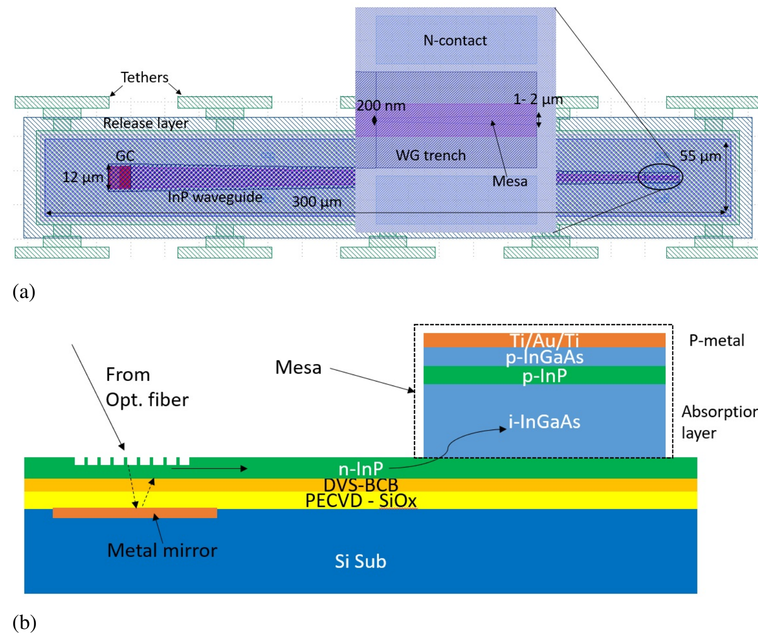


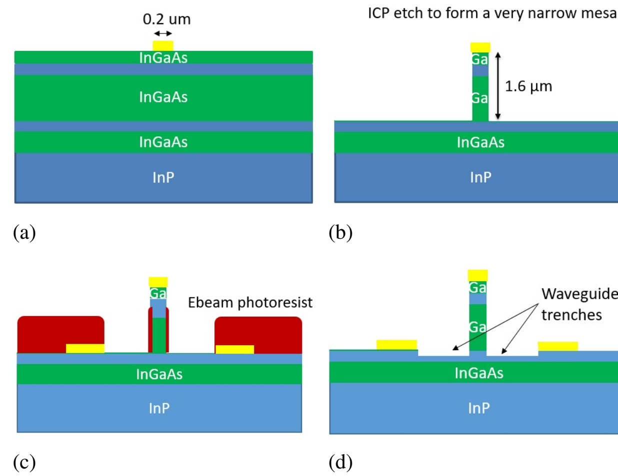
Figure 3.37: Waveguide-coupled photodiode schematic design. (a) schematic top design view; (b) schematic cross-section view of photodiode transfer printed on the silicon substrate with the defined metal mirror.

3.38: 1) to define a narrow mesa by using a metal hard mask (Figure 3.38(a) and (b)) and 2) to define the waveguide trenches and the grating coupler when the 1.6 μm mesa creates a large topography on the substrate for the ~650 nm thick e-beam resist (see Figure 3.38(c) and (d)).

3.7.2.1 Mesa fabrication

We started the process development with two blank InP substrates, which were prepared in two different ways: one substrate had a 10-minute oxygen plasma treatment, on which the e-beam resist AR-P-6200-13 [13] was directly spin-coated. Sample number two had the same 10-minute oxygen plasma cleaning, on which the Ti Prime adhesion promoter [14] was spin-coated, followed by the e-beam resist AR-P-6200-13.

Because the e-beam resist has a positive profile (the material is exposed by the electron beam and the developer will dissolve the regions that were exposed to electrons [15]), a Ti/Au/Ti metal combination can be directly deposited with thicknesses (20/50/100 nm) after the e-beam exposure and development. The optical microscope picture after the development is depicted in Figure 3.39. Here,



(a) (b) (c) (d)

Figure 3.38: Schematics of the envisioned waveguide-coupled photodiode process flow.

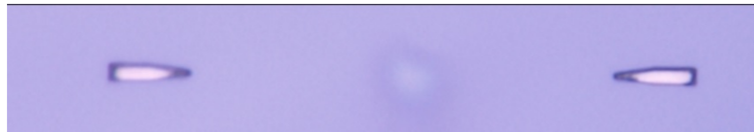


Figure 3.39: Microscope image of the formed Ti/Au/Ti metal mask after the lift-off.

narrow taper-like metal structures were formed. The taper tip widths have been swept between 100 to 500 nm.

Samples without any surface preparation had the resist stripped-off during the development. The other sample with the adhesion promotor was placed in the inductive-coupled plasma (ICP) chamber for about 35 minute InP etching, using a CH_4-H_2 plasma. The structures defined on the sample were then placed under the scanning electron microscope (SEM).

Figure 3.40(a) depicts the narrow taper tips of 150 nm using the 180 $\mu C/cm^2$ e-beam exposure dose. Figure 3.40(b) shows better quality metal tips of 200 nm using an e-beam exposure dose of 200 $\mu C/cm^2$. However, looking at Figure 3.40 in the vicinity around the narrow tapers, one can see a lot of unusual dots. Looking at the tilted SEM picture in Figure 3.41, one can see that "grass" is present around the formed mesa structure.

The explanation for this could be the Ti particles present in the Ti prime adhesion promotor layer, which adhere to the surface of the substrate, hence creating a masking effect when the substrate is dry etched. Using no Ti prime layer, however, leads to e-beam resist stripping, due to poor adhesion. The latter could be related to the fact that a thin oxide-layer forms on the surface of the blank InP substrate after

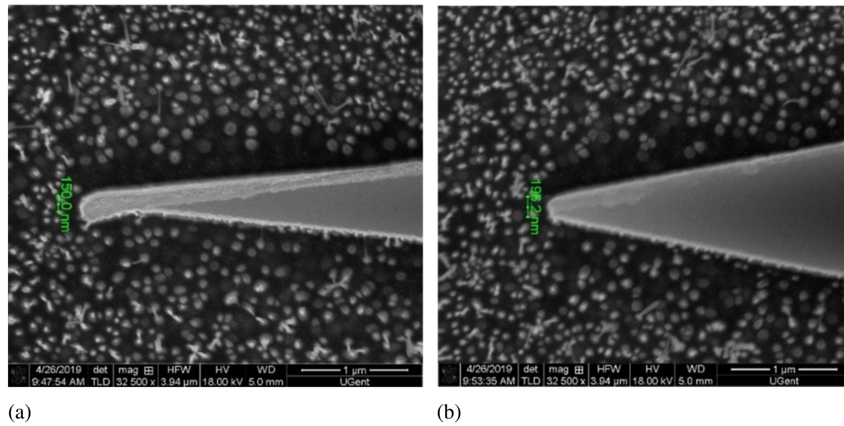


Figure 3.40: Scanning electron microscopy pictures of the defined taper tips. (a) 150 nm tip defined using 180 $\mu C/cm^2$ e-beam exposure dose; (b) 200 nm tips defined using 200 $\mu C/cm^2$ exposure dose.

the 10-minute oxygen plasma treatment, therefore a 5-second buried hydrofluoric acid (BHF) dip before spin-coating the e-beam resist might be an effective solution to the problem.

Figure 3.42 compares the surface of the InP substrate with the Ti prime adhesion promotor layer (Figure 3.42(a)) versus a BHF-dipped sample with no Ti prime layer after several cycles of ICP etching. The SEM image in Figure 3.42(b) clearly indicates a clean grass free surface when the 5-second BHF dip is applied.

Using this knowledge, we attempted the process on the real photodiode epitaxial III-V material stack. It is important to mention that stopping the ICP etch on the surface of the n-InP layer (see Figure 3.38(b)) and leaving no InGaAs layer is challenging, as the mesa is very narrow and using wet processing to remove the residual InGaAs similarly to the substrate-illuminated III-V PD fabrication might not be effective. This is demonstrated in Figure 3.43. Using only the ICP etch for ~35 minutes, the sidewalls are clean and narrow taper tips are easily formed (Figure 3.43(a)). To remove the residual InGaAs layer, one can dip the sample for 1 minute into a diluted piranha (1:1:50) solution, where the InGaAs layer is selectively etched. This is seen in Figure 3.43(b). This approach, however, might not be desired, as the wet etch reduces the mesa width. Immersing the epi in the piranha solution for only 3 minutes, the InGaAs layer can be fully removed. This is shown on the focused-ion beam (FIB) cross-section image in Figure 3.43(c).

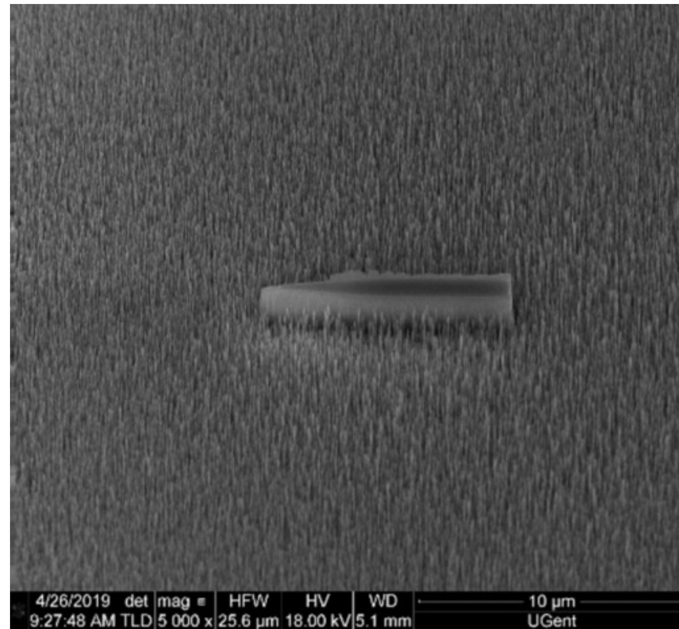


Figure 3.41: Side view scanning electron microscope picture of the "grass".

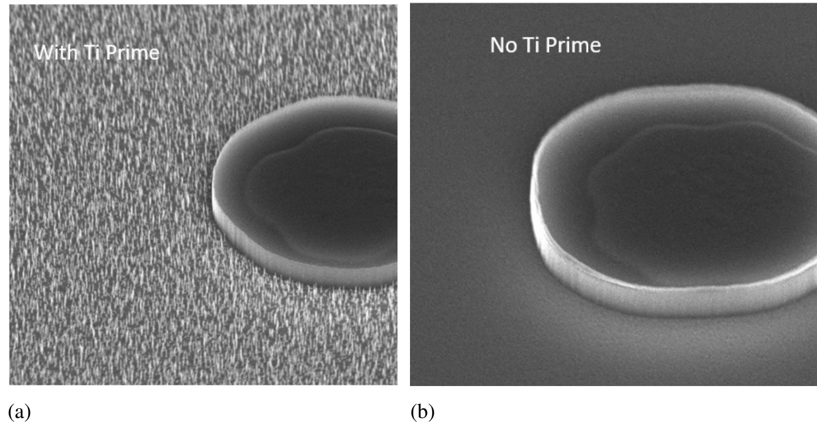
3.7.2.2 Forming waveguides and gratings

The challenge of the second processing step is to form gratings and waveguide trenches using only ∼650 nm thick resist. The difficulty is that the sample now has a high topography with the defined mesa height of about 1.6 μm.

In the previous subsection, we understood that Ti prime should be avoided in all cases. However, now with the mesa formed and Ti/Au/Ti electrodes present on the sample, which will later act as a metal contact, the HF dip should be avoided because it etches Ti.

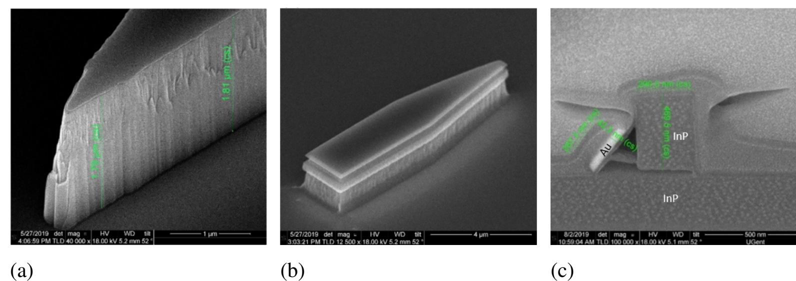
An initial attempt is depicted in Figure 3.38(c): we spin-coat the AR-P-6200-13 and use the e-beam resist as a mask to directly etch waveguides and gratings. Figure 3.44 depicts the problem of this approach: after patterning the resist and the e-beam resist becomes hard to remove, even after 40 minutes of oxygen plasma treatment (Figure 3.44(a)). Also a rough surface can be obtained (Figure 3.44(b)). The first processing attempt, however, illustrates that it is possible to form gratings and waveguide trenches even with high topography on the sample.

The solution is to replace the resist as a mask with a mixed-frequency silicon nitride (MF-SiN_x) mask. This material is widely applied for III-V device passivation [16] and is deposited using a plasma-enhanced chemical vapor deposition (PECVD) tool at 270°C. The schematic process flow is depicted in Figure 3.45.



(a) (b)

Figure 3.42: Scanning electron microscope image of two InP substrates with deposited Ti/Au/Ti mask with different surface preparations. (a) using Ti prime adhesion promotor; (b) using no Ti prime and using 5 second BHF dip.

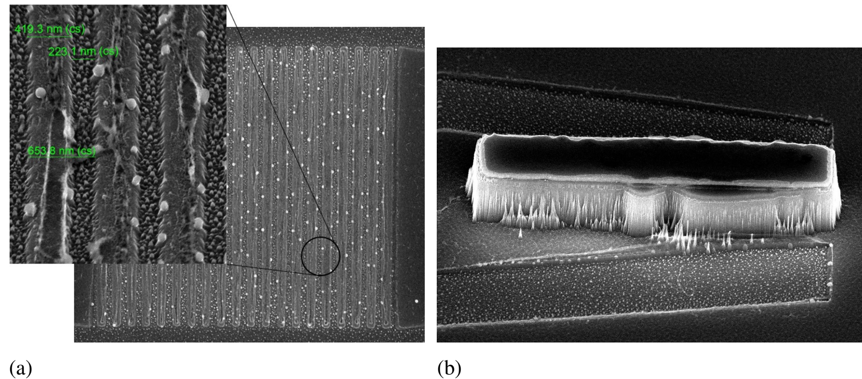


(a) (b) (c)

Figure 3.43: Scanning electron microscope images of the mesas defined on the III-V epitaxial layer stack. (a) using only ICP etching. (b) Using ICP etching complemented with 1-minute piranha 1:1:50 dip. (c) Focused ion beam image of the mesa using ICP complemented with a piranha 1:1:50 3-minute dip. We see that the chemical removes the InGaAs layers completely leaving the top metal collapsed.

We deposit MF-SiN$_x$ on two samples with different thicknesses (Figure 3.45(a)): one with 50 nm and the other with 200 nm MF-SiN$_x$. The resist was spin-coated and the gratings were written in the resist layer, then the MF-SiN$_x$ was etched using reactive ion etching (RIE) (CF_4-SF_6-H_2) for 1 and 3 minutes respectively (Figure 3.45(b)). Then we removed the photoresist and etched the InP in the ICP for 2 minutes (Figure 3.45(c)). After this the MF-SiN$_x$ was fully removed using RIE again (Figure 3.45(d)).

The surfaces of the chip of these two samples are depicted in Figure 3.46(a) and (b). The sample with the 200 nm MF-SiN$_x$ (Figure 3.46(a)) indicates poorly-written gratings after removing the hard mask. The sample with the 50 nm silicon



(a) (b)

Figure 3.44: Scanning electron microscope image after patterning e-beam resist hard mask. (a) grating definition; (b) waveguide trench definition close to the patterned mesa. The images clearly indicate resist residues present even after using lengthy oxygen plasma surface treatment.

nitride top layer yields cleanly defined gratings (Figure 3.46(b)) with an appropriate 120 nm etch depth in the grating region (Figure 3.46(c)).

It is crucial to form the gratings with the correct period and the proper FF. It is clear that with the high mesas in the vicinity, the spin-coated resist thickness might vary, therefore the grating dimensions have to be properly swept and measured with the SEM to assess the effect.

The period replicates the designed one. The result presented in Figure 3.47 measures the defined grating etch teeth using the e-beam processing versus the ones designed on the mask. The substrate with the 1.6 μm high mesa is compared with the flat substrate using an e-beam exposure dose of 175 μC/cm^2. The result demonstrates that the sample with the 1.6 μm topography has wider exposed teeth than the flat sample. For a grating slit of 100 nm on the mask, one has a 160 nm grating slit written on the flat sample and 200 nm grating slit written on the sample with the topography. This means that the topography present on the sample increases the thickness of the e-beam resist and the wider-exposed slit effect must be considered when designing the grating mask.

3.7.3 Process flow summary

We briefly summarise the main findings of the process development of the first two steps of waveguide-coupled photodiode processing and present the process flow. The cleaved III-V epi with the removed cap layer is cleaned for $\sim$10 minutes in oxygen plasma, after which a residual oxidation layer is removed by immersing the epitaxial material stack in BHF for 5 seconds. After this, an AR-P-6200-13 resist is spin-coated and the sample is exposed with e-beam using an exposure dose of

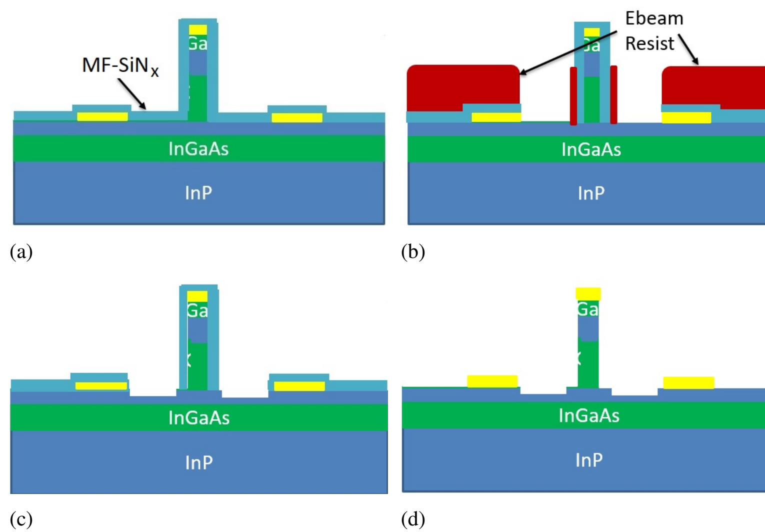


Figure 3.45: Process flow of grating and waveguide trench patterning using silicon nitride hard mask.

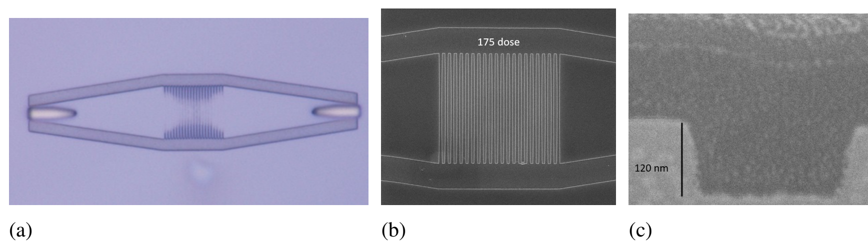


Figure 3.46: (a) Microscope image of poorly-patterned gratings using a 200 nm MF-SiN$_x$ mask layer. (b) Scanning electron microscope image of the patterned grating using the 175 μC/cm^2 exposure dose and a 50 nm SiN$_x$ mask. (c) focused ion beam cross-section of the patterned grating using 50 nm thick MF-SiN$_x$ hard mask.

200 μC/cm^2. After development, the Ti/Au/Ti metal with a thickness combination of 20/50/100 nm is deposited and lifted-off. Then the sample is placed in the ICP chamber for $\sim$35 minutes etching using CH_4-H_2.

After this, a thin 50 nm MF-SiN$_x$ layer is deposited using PECVD. A new layer of e-beam resist is spin-coated and the sample is exposed using a 175 μC/cm^2 dose. When developed, the resist is patterned and an RIE SF_6-CF_4-H_2 recipe is used for around 1 minute to pattern the gratings and the waveguide trenches in the MF-SiN$_x$ hard mask layer. Then an ICP 2-minute etch in CH_4-H_2 patterns the n-InP layer after which the silicon nitride hard mask is removed in RIE. When designing

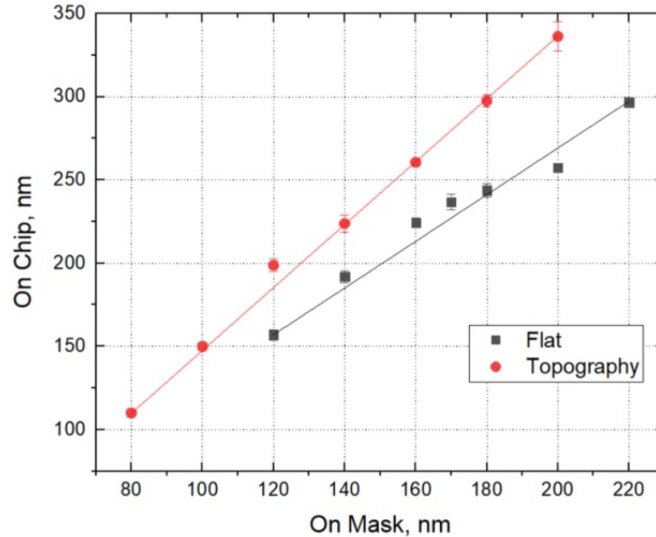


Figure 3.47: The etched grating teeth compared on the mask (x-axis) versus measured on the chip using scanning electron microscope (y-axis): flat sample versus the sample with the 1.6 µm high topography.

the grating mask, resist thickness and large topography must be considered and the grating slits should be chosen according to Figure 3.47.

The consequent processing, releasing and printing of waveguide-coupled photodiode devices is similar to the process flow described in section 3.4.

3.8 Conclusions

In this chapter we demonstrated micro-transfer-printing of III-V substrate-illuminated photodiodes onto silicon photonic integrated circuits. In the first part of the chapter we demonstrated parallel transfer printing of in-house fabricated substrate-illuminated III-V C-band photodetectors. We developed the photodiode fabrication and release processes, as well as the automated picking and printing of the devices to achieve a high transfer printing yield. In the second part of the chapter we demonstrated a single-polarization and a polarization-diversity tunable ring resonator receiver with transfer-printed III-V p-i-n detectors. We fabricated heaters to tune the resonance wavelength of each channel of both receivers (spaced by 2.5 nm). 4×25 Gbit/s operation is demonstrated for both receivers. The polarization-diversity receiver shows 2.5 dB polarization dependent losses and bit-error rate measurements show transmission below HD-FEC for both polarization states as well as for the 3dB detuned transmission edge of the filter. Finally, we discussed

the main findings of process development of III-V waveguide-coupled photodiodes. We fabricated a 1.6 μm high absorption mesa with the 200 nm wide taper tip and patterned a grating coupler in close proximity.

The results of this chapter showcase the potential of transfer printing technology for the cost- and time-effective realization of active photonic integrated circuits based on silicon photonic passive waveguide circuits. The concept is not limited to the integration of photodetectors but also enables the scalable, wafer-scale integration of other III-V devices including lasers.

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4
Conclusion and Prospects

4.1 Conclusion

As outlined in the introduction chapter, micro-transfer-printing is a novel, promising, heterogeneous integration technology for realizing cost- and time-effective wafer scale heterogeneous integration for complex photonic integrated circuits. The results of this thesis demonstrate the key advantages of the technique.

We demonstrated the high alignment accuracy of micro-transfer-printing by designing, fabricating, releasing, and transfer-printing passive silicon photonic optical structures with an alignment accuracy better than ± 1 μm. We transfer-printed a device with an adiabatic taper operating at 1310 nm and a device with a directional coupler optical structure operating at 1600 nm. The coupling loss measurements yielded -1.5 dB $\pm$ 0.5 dB for a single interface for the adiabatic taper coupler at 1310 nm and -0.5 dB $\pm$ 0.5 dB for the directional coupler at 1600 nm.

We demonstrated the versatility of the micro-transfer-printing technique by releasing and transfer printing iSIPP25G SiGe photodiodes onto a silicon photonic integrated circuit. We obtained 0.66 A/W responsivity and demonstrated data reception at 50 Gbit/s at 1550 nm. This demonstration paves the way for a solution to the long turnaround time and expensive fabrication problem of active silicon photonic integrated circuits in the CMOS fab.

We demonstrated the parallel micro-transfer-printing process by designing, fabricating, and releasing large arrays of III-V substrate-illuminated photodiodes. Using a 2×2 arrayed PDMS stamp, we exploited the automated picking & print-

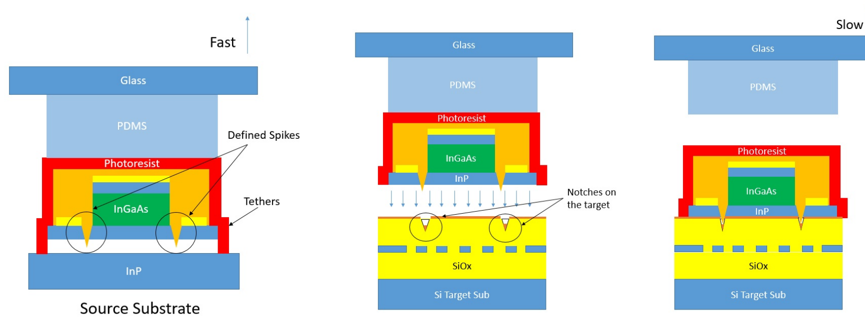

Figure 4.1: Envisioned schematics of mechanical alignment. The example depicts micro-transfer-printing of grating-assisted photodiodes.

ing, and rework procedures to demonstrate high yield arrayed transfer-printing.

Finally, we demonstrated cost- and time-effective, scalable III-V-on-Si integration for realizing complex receivers by micro-transfer-printing commercial IIIV photodetectors on silicon photonic WDM tunable ring receivers. We fabricated and characterized single polarization and polarization-diversity receivers; 4×25 Gbit/s operation was demonstrated for both receivers. The polarization-diversity receiver demonstrated 2.5 dB polarization dependent loss and obtained bit-error rate measurements below the HD-FEC for both states of polarization.

4.2 Prospects

Several routes are identified to continue the work on the micro-transfer-printing on a technology level.

Submicron alignment accuracy micro-transfer-printing. Even though we demonstrated continuous alignment better than ±1 micrometer in this thesis, the technique was applied by printing one device at a time. One of the biggest challenges of the technology so far is the limited alignment accuracy printing large arrays of (long) devices.

A step to improve the alignment accuracy for large arrays of devices would be to apply a mechanical alignment scheme. The idea is depicted in Figure 4.1. Spikes of solid filled material are defined sticking out of the bottom of the released coupon, and locally etched areas (notches) are defined with the same pitch on the target wafer. By picking the coupon, aligning it with the target using visual alignment and printing it, the spikes on the device are expected to slide into the notches of the target wafer leading to alignment accuracy better than ± 500 nm.

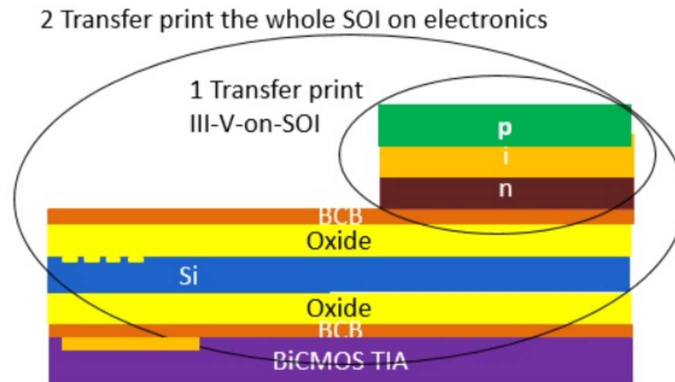

Figure 4.2: Schematics of micro-transfer-printing as a "constructor" principle.

Micro-transfer-printing as a "constructor" principle. By developing the transfer printing of III-V devices on SOI circuits and the micro-transfer-printing of SiGe devices, new research ideas can be proposed. For example, the development of micro-transfer-printing as a "constructor" principle, as depicted in Figure 4.2. In the first processing step, we can transfer print a III-V active device (e.g. p-i-n PD) on top of the silicon PIC (1). Then, we can release and transfer print the complete SOI stack together with the transfer printed III-V device from the previous step on e.g. a BiCMOS trans-impedance amplifier or other electronic interfaces (2).