GaAs VCSEL Integration on SiN Waveguide Circuits: Design, Technology and Devices

Integratie van GaAs-VCSELs op SiN-golfgeleidercircuits:
ontwerp, technologie en componenten

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Proefschrift ingediend tot het behalen van de graad van
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List of Abbreviations

A

AFM	Atomic force microscope

B

BCB	Benzocyclobutene
BER	Bit error rate

C

CMOS	Complementary metal oxide semiconductor
CS	Cross-sectioning
CSL	Current spreading layer

D

DAC	Digital to analog converter
DBR	Distributed Bragg reflector

E

EBL	Electron-beam lithography
EEL	Edge-emitting laser
ELO	Epitaxial lift-off
ER	Extinction ratio

F

FBMS	Fixed beam moving stage
FDTD	Finite difference time-domain
FIB	Focused ion beam
FP	Fabry-Perot

G

GC	Grating coupler

H

HCG	High contrast grating

I

ICP	Inductively coupled plasma
IPA	Iso-propyl alcohol

L

LED	Light-emitting diode
LPCVD	Low pressure chemical vapour deposition

M

MES	Mesitylene
MOCVD	Metal organic chemical vapour deposition
MQW	Multiple quantum wells

O

OF	Optical feedback
OOK	On-off keying

P

PECVD	Plasma enhanced chemical vapour deposition
PICs	Photonic integrated circuits
PM	Power meter
PR	Polarization rotator
PRBS	Pseudo random bit sequence

Q

QWs	Quantum wells

R

RIE	Reactive-ion etching

S

SC-1	Standard clean-1
SEM	Scanning electron microscope
SiP	Silicon photonics
SCH	Separate confinement heterostructure
SMSR	Side mode suppression ratio
SOI	Silicon on insulator

T

TE	Transverse electric
TM	Transverse magnetic
TMM	Transfer matrix method

V

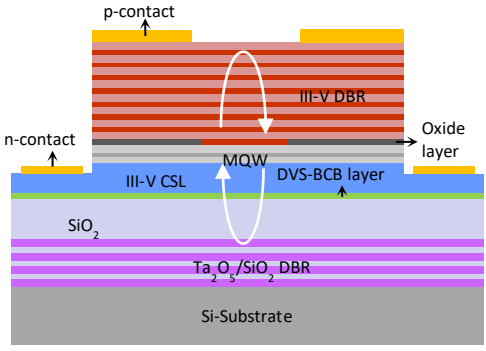
VCSEL	Vertical cavity surface emitting laser
VCSIL	Vertical cavity silicon-integrated laser
VGC	Vertical grating coupler
VNA	Vector network analyzer
VOA	Variable optical attenuator

Nederlandse samenvatting –Summary in Dutch–

In de afgelopen jaren zijn aanzienlijke investeringen gemaakt in onderzoek, ontwikkeling en industrialisatie van silicium-gebaseerde fotonica. Bijgevolg heeft deze technologie zich ontplooid voor optische tele- en datacommunicatie op 1310 en 1550 nm golflengte. Echter, voor applicaties waar kortere golflengtes noodzakelijk zijn, is Si gelimiteerd door de inherente materiaalabsorptie bij golflengte korter dan 1.1 µm. Daarentegen kan siliciumnitride (SiN) gebruikt worden als een vervanger voor Si, waarbij een gelijkaardige miniaturisatie kan bereikt worden door middel van het relatief hoge brekingsindexcontrast tussen SiN (n~2) en siliciumdioxide (SiO_2, n~1.5). Verder is dit materiaalplatform volledig compatibel met dezelfde *complementary metal oxide semiconductor* (CMOS) fabricagetechnologie als diegene die gebruikt wordt voor Si [1]. In het bijzonder is SiN relevant voor biomedische toepassingen omdat de materiaalabsorptie miniem is in het therapeutische golflengtegebied (van zichtbaar licht tot het nabij-infrarood). In dit golflengtedomein zijn de schade aan biologische cellen en de absorptie van water beide minimaal. En hoewel er een ontwikkeling heeft plaatsgevonden van passieve componenten op het SiN-platform zoals de realisatie van golfgeleiders [2], spectrometers [3] en andere componenten, is het momenteel nog een grote uitdaging om geïntegreerde lichtbronnen te maken op SiN. De moeilijkheid ligt in het gebrek aan lichtemissie van SiN. Tot dusver zijn de ontwikkelingen op SiN gerealiseerd met externe lichtbronnen. Bijgevolg biedt een geïntegreerde on-chip laser als lichtbron een enorm potentieel voor *point-of-care* applicaties of implantaten die lichaamsfuncties continu kunnen opmeten zoals continue glucosemetingen of sensoren ingebouwd in smartphones. De meest belovende aanpak om laserfunctionaliteit op de chip te verwezenlijken op korte termijn is de heterogene integratie van III-V materialen door middel van binding van deze materialen met een tussenliggend, klevend materiaal zoals benzocyclobuteen (BCB) [4].

De *vertical cavity surface emitting laser* (VCSEL), waarbij het licht uit het oppervlak van de structuur schijnt, heeft verschillende unieke voordelen zoals een kleinere benodigde oppervlakte op de chip, een efficiënte conversie van elektriciteit naar licht, en een laag energieverbruik dat interessant is voor mobiele applicaties. De nieuwste en beste VCSEL heeft vandaag een conversie-efficiëntie van meer dan 60% [5], een modulatiebandbreedte van meer dan 30 GHz [6],

datasnelheden boven 70 Gb/s [7], en een energiedissipatie van minder dan 100 fJ/bit voor datasnelheden tot 50 Gb/s [6,8] waarbij een elektrische stroom van slechts enkele milliampère gebruikt wordt voor de sturing van de VCSEL. Om deze redenen zal de integratie van VCSELs op het SiN platform verdere ontwikkelingen mogelijk maken van applicaties in de telecommunicatiesector en de biomedische sector resulterend in deze meer geïntegreerde oplossingen die relevant zijn voor industrieën. Het is dus daarom de doelstelling van dit doctoraat om een nieuw GaAs-VCSEL concept voor te stellen, te ontwerpen, te ontwikkelen en te karakteriseren op een SiN geïntegreerd fotonisch circuit.

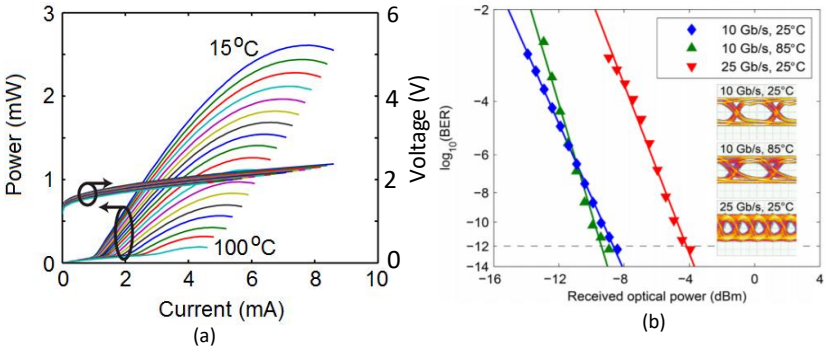


Figuur. 1 Schematische doorsnede van de Gen1-VCSEL (emissie van het licht via het topoppervlak).

Om deze doelstelling te realiseren, hebben we nauw samengewerkt met Chalmers University of Technology. Samen hebben wij het design voorgesteld van de hybride-caviteit VCSELs (HC-VCSELs), waarbij een epitaxiaal gegroeide GaAs half-VCSEL bestaande uit een spiegel, een actieve laag en een stroomverdelingslaag in zijn geheel geïntegreerd wordt op een andere diëlektrische spiegel (boven op een Si-substraat) met behulp van een tussenliggende DVS-BCB-bindingslaag zoals geïllustreerd in figuur 1. In verdere ontwikkelingen kunnen we het licht horizontaal uitkoppelen naar een SiN-fotonisch circuit door een zwakke diffractiekoppelaar te introduceren in de VCSEL-caviteit. In de eerste fase van dit doctoraat is de technologie ontwikkeld in de vorm van een eerste generatie (Gen1 HC-VCSELs) hybride VCSEL. Deze structuren bevatten geen diffractiekoppelaar, waardoor het licht nog langs de bovenzijde van de VCSEL uitstraalde. De Gen1-VCSELs dienden als een validatiemodel om de prestaties van de hybride half-VCSEL te karakteriseren, waarbij onderzocht werd wat de invloed was van de divinylsiloxaan-bis-benzocyclobuteen (DVS-BCB) bindingslaag en de diëlektrische spiegel op de optische karakteristieken van de HC-VCSEL.

De GaAs half-VCSEL werd geïntegreerd op een diëlektrische spiegel op Si door middel van een dunne laag DVS-BCB. Na de binding werd het GaAs-substraat verwijderd door middel van een natte, selectieve ets, waarna de VCSEL gemaakt werd via een standaard fabricagemethode [9].

Met deze technologie hebben we werkende VCSELs aangetoond die licht uitstraalden op 850 nm golflengte met een drempelstroom kleiner dan 1 milliampère. Het vermogen van het uitgestraalde licht was groter dan 2 mW (figuur 2-(a)), waarmee een modulatiesnelheid van 25 Gbits/s behaald is (figuur 2-(b)).



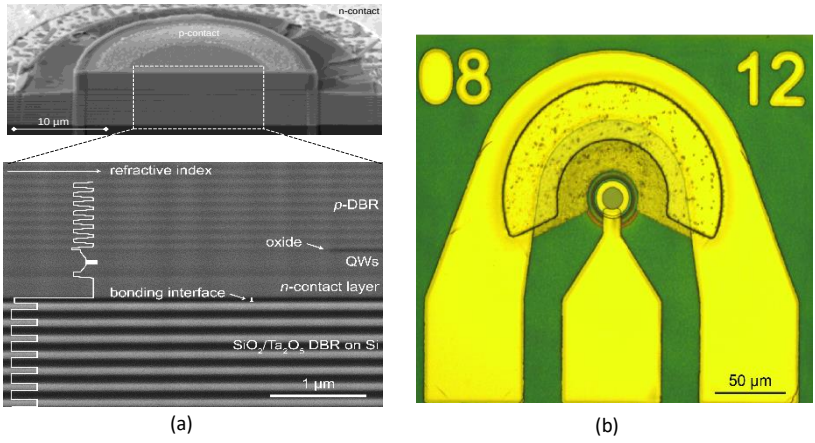
Figuur 2 (a) Het lichtvermogen en de elektrische spanning versus de stroom voor een VCSEL met een bindingslaagdikte van ~65 nm en een oxide-apertuur van 10 µm, gemeten van 15 tot 100 °C in stappen van 5 °C. (b) Een opgemeten bit error rate (BER) tegenover het ontvangen optische vermogen voor een VCSEL met een 5 µm oxide-apertuur en eenzelfde bindingslaagdikte van ~65 nm, voor snelheden tot 25 Gbit/s bij 25 °C en 10 Gbit/s bij 85 °C. De inzet toont bijbehorende optische oogdiagrammen, schaal 100 mV/div en 20 ps/div.

Een doorsnede van de VCSEL-structuur is weergegeven in figuur 3-(a), waar de diëlektrische spiegel oftewel de diëlektrische Braggreflector (DBR) wordt getoond, samen met de bindingsinterface en de III-V half-VCSEL met oxide-apertuur. Coplanaire grond-signaal-grondelektrodes zijn gemaakt voor de hogesnelheidsmetingen, zoals weergegeven in figuur 3-(b). Experimenteel hebben we ook vastgesteld dat de dikte van de bindingslaag geoptimaliseerd kon worden naar een bepaalde prestatie-indicator, zoals bijvoorbeeld optimale werking op een gegeven temperatuur of een minimale variatie van de prestaties over een bepaald temperatuursbereik [10].

Om vervolgens het verticaal versterkte licht horizontaal uit te koppelen in een SiN-golfgeleider hebben we een SiN-golfgeleider met bijbehorende

diffractiekoppelaar toegevoegd aan de VCSEL-caviteit, bovenop de onderste diëlektrische spiegel. De diffractiekoppelaar is gedefinieerd met een ondiepe ets, bovenop de SiN-golfgeleider, voorafgaand aan de binding met de GaAs halve VCSEL. Van zodra deze VCSELs geïntegreerd zijn op een SiN-golfgeleidercircuit, benoemen we deze structuren als Gen2 verticale-caviteit Si-geïntegreerde lasers (Gen2-VCSILs). De voordelen van een dergelijke intra-caviteit diffractiekoppelaar zijn veelvoudig [11]:

- De voorgestelde koppelaar maakt een volledige heterogene integratie mogelijk zoals diegene ontwikkeld voor Gen1-componenten.
- De koppelaar maakt het mogelijk om als een polarisatiefilter te werken en zodoende de TM-mode te onderdrukken en de TE-mode te ondersteunen.
- Dit laat ook toe om de transversale mode te controleren.
- Een hoge koppelingsefficiëntie naar de golfgeleider kan bereikt worden.
- Zoals aangetoond in [9], wordt de alignering bepaald door de lithografiestappen in de VCSEL fabricage na het integreren van de halve VCSEL.

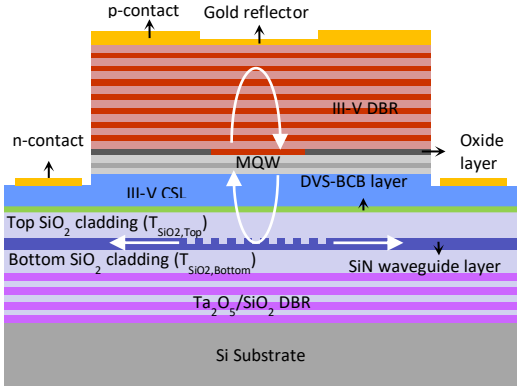


Figuur. 3 SEM-afbeeldingen van een *focused ion beam* doorsnede (links) en een microscoopafbeelding van de bovenzijde (rechts) van een gefabriceerde HC-VCSEL.

Een schematische voorstelling van een Gen2-VCSIL is weergegeven in figuur 4. De reflectie en koppelingsefficiëntie (links of rechts) van deze koppelaar plus onderste diëlektrisch spiegel hangen af van de grootte van de oxide-apertuur

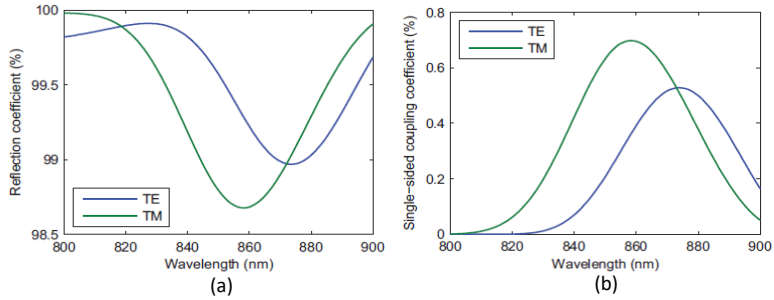
van de GaAs VCSEL. Een VCSEL met oxide-apertuur > 4µm is noodzakelijk om polarisatieselectiviteit te bekomen via de intra-caviteit diffractiekoppelaar waarbij een voldoende hoge reflectie en koppeling van de TE-mode naar de golfgeleider behaald worden.

Voor de Gen2-VCSIL met een apertuur van 5 µm, is de reflectie en de enkelvoudige koppelingsefficiëntie van de koppelaar/spiegel-combinatie, waarbij de koppelaar periode 530 nm is met een duty cycle van 50 % (DC, slot-versus-tandverhouding in een enkelvoudige periode) en een etsdiepte van 50 nm, weergegeven in figuur 5. Vanuit de experimentele karakterisatie van de Gen1-structuren hebben we geleerd dat de VCSELs het best werken op 855 nm bij kamertemperatuur op gebied van optisch vermogen en drempelstroom [10]. Daarom zijn de Gen2-VCSILs ontworpen om op deze golflengte te werken.

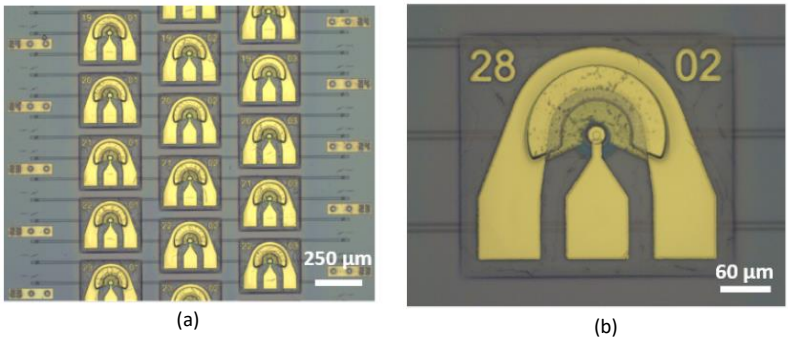


Figuur. 4 Schematische doorsnede van de Gen2 VCSIL structuur met horizontale uitkoppeling naar een SiN-golfgeleider.

Uit figuur 5(b) kunnen we afleiden dat de diffractiekoppelaar zodanig ontworpen is dat de Bragg-golflengte van de roosterkoppelaar voor de TE-mode (waar het elektrisch veld parallel staat met de geëtste lijnen van de koppelaar) ver weg staat van de operationele golflengte van de VCSEL (855nm). Doordat de TM-mode (waar het elektrisch veld loodrecht staat op de geëtste lijnen van de koppelaar) dichter bij de Bragg-conditie werkt dan de TE-mode, zal meer licht uitgekoppeld worden, waardoor de totale reflectie van de TM-mode lager is dan die van de TE-mode. Als gevolg gaat de TM-mode meer verlies ervaren in de VCSIL-caviteit en onderdrukt worden ten opzichte van de TE-mode.



Figuur. 5 (a) De gesimuleerde reflectiecoëfficiënt en (b) de enkelvoudige koppelingsefficiëntie van de diffractiekoppelaar plus diëlektrische spiegel in functie van de golflengte voor TE en TM polarisaties. (koppelaarperiode = 530 nm, DC = 50%).

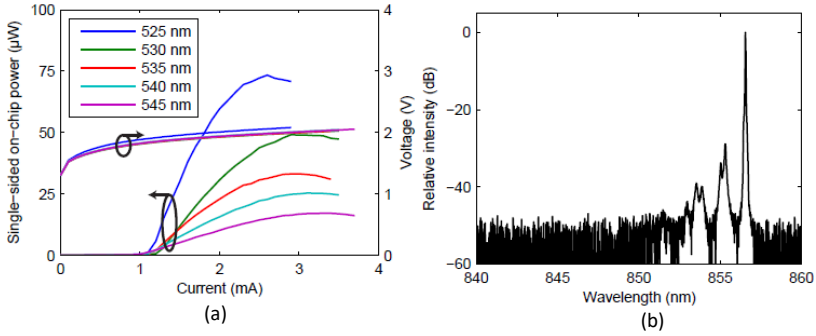


Figuur. 6 Microscoopafbeelding van (a) een set van volledig gefabriceerde Gen2-VCSILs en (b) van een enkele Gen2-VCSIL, waarbij de SiN-golfgeleiders zichtbaar zijn op de chip.

Wij hebben succesvolle werking gedemonstreerd van Gen2-VCSILs, werkende bij een golflengte van 856 nm waarbij het laserlicht in de golfgeleiders opgemeten is als zijnde TE-gepolariseerd. Figuur 6 toont microscoopafbeeldingen van de volledig gefabriceerde Gen2-VCSILs bovenop de intra-caviteit-diffractie-koppelaars en golfgeleiders. Een Gen2-VCSIL met 5 µm oxide-apertuur heeft een drempelstroom van 1,13 mA en produceert een maximaal uitgangsvermogen van ongeveer 73 µW (figuur 7(a)) met een onderdrukking van naburige modes (side mode suppression ratio (SMSR)) van 29 dB (figuur 7(b)).

De prestatie van zowel de Gen1-VCSEL en de Gen2-VCSIL waren in zekere mate gelimiteerd door de hoge thermische impedantie van de onderste, diëlektrische spiegel. De thermische impedantie van beide componenten met een 5 µm apertuurdiameter zijn 3 tot 4 keer hoger dan die van standaard VCSELs met

een gelijkaardige apertuurgrootte [12]. De Gen1-VCSELs presteren beter dan de Gen2-VCSILs door additionele caviteitsverliezen die wij toeschrijven aan een onvoorziene ruwheid in de lagenstructuur en materiaalabsorptie van de spiegel. Om dit te verbeteren kan in de toekomst een onderste diëlektrische spiegel gebruikt worden die een hoger index contrast heeft (bv. Si/SiO_2) waardoor een kleiner aantal DBR paren nodig zijn in de spiegel en het probleem van ruwheid geminimaliseerd wordt. Ook kunnen metallische warmtespreiders geïntegreerd worden om de thermische impedantie van de componenten te verbeteren.



Figuur.7 (a) Golfgeleidergekoppelde licht-spanning-stroom karakteristiek voor 5 µm oxide apertuur diameter VCSILs met een wisselende intra-caviteit diffractie-koppelaarperiode van 525 – 545 nm (na goud depositie op het bovenste spiegeloppervlak). (b) Spectrum voor de 525nm VCSIL, bij 2.5 mA.

Doorheen dit werk is het ontwerp en de fabricage van het SiN fotonisch geïntegreerd circuit (PIC) en het heterogene integratieproces van de GaAs half-VCSEL met de SiN-PIC uitgevoerd door de auteur. Het ontwerp van de volledige VCSEL is gedaan door Johan Gustavsson van Chalmers University of Technology. Na de heterogene integratie van de half-VCSELs, is de fabricatie van de Gen1- en Gen2-VCSELs uitgevoerd door Emanuel P. Haglund in het kader van zijn doctoraatsonderzoek.

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English summary

Over the past years, considerable efforts have been invested in research, development and industrialization of silicon (Si) photonics. As a result Si photonics has emerged as a mature technological platform for optical datacom and telecom applications at 1310 and 1550 nm. However, for applications requiring shorter wavelengths, Si cannot be used due to the absorption in Si below 1.1 µm wavelength. Instead silicon nitride (SiN) can be used as a substitute of Si, providing similar circuit compactness, resulting from the relatively high refractive index contrast between SiN (n~2) and silicon dioxide (SiO_2, n~1.5), and it can be manufactured using the same complementary metal oxide semiconductor (CMOS) fabrication infrastructure as Si [1]. SiN has particular relevance for life science applications, because of the therapeutic window at visible and very near-IR wavelengths for biological media, where the photo-damage of cells is minimal and water absorption is negligible. While there has been a rapid development of different optical components such as low-loss waveguides [2] and spectrometers [3] on the SiN platform, the realization of integrated light sources on SiN is still a major challenge. Difficulties arise from the lack of light emission from SiN. So far, the research efforts in this field have been realized with external light sources. Hence, an integrated laser source in such densely integrated systems would provide immense potential for applications such as medical point-of-care devices, body implants for monitoring of glucose levels, and sensing devices integrated into smartphones. To bring laser functionality to SiN waveguide circuits, the most promising short-term approach is the heterogeneous integration of III-V materials using adhesive bonding [4].

Vertical cavity surface emitting lasers (VCSELs) have several unique advantages such as small footprint, a possible single mode output, the ease with which they can be formed into an array, and their low power consumption. State-of-the-art discrete VCSELs today have been demonstrated with power conversion efficiencies exceeding 60% [5], modulation bandwidths up to 30 GHz [6], data rates exceeding 70 Gbit/s [7], and energy dissipation less than 100 fJ/bit at data rates up to 50 Gbit/s [6,8] with drive currents of only a few milliamperes. Therefore, bringing these distinct features of VCSELs on SiN waveguide circuits by heterogeneous integration technology will benefit applications such as on-chip short-wavelength optical interconnects and life science applications. Therefore, the main goal of this PhD is to propose, design, fabricate and demonstrate a heterogeneously integrated GaAs vertical cavity laser source on a SiN waveguide circuit.

To fulfil this goal we worked in close collaboration with Chalmers University of Technology. Together we proposed a design of hybrid-cavity VCSELs (HC-VCSELs), where an epitaxial GaAs half VCSEL containing a reflector, an active region and a current injection layer can be attached to a dielectric DBR deposited on a Si substrate, using adhesive bonding. Further, the vertically amplified light can be coupled to an in-plane SiN waveguide by placing a weak diffraction grating connected to a SiN waveguide inside the cavity. We took the first step towards the realization of such a device by developing a technology to demonstrate a 1st generation of hybrid-cavity VCSELs (Gen1 HC-VCSELs) on Si without any grating inside the cavity [9], see Fig. 1. While these lasers were still surface emitting, the purpose was to develop the integration technology and to study the impact of the dielectric DBR and divinylsiloxane-bis-benzocyclobutene (DVS-BCB) bonding layer on the optical performance of the HC-VCSEL.

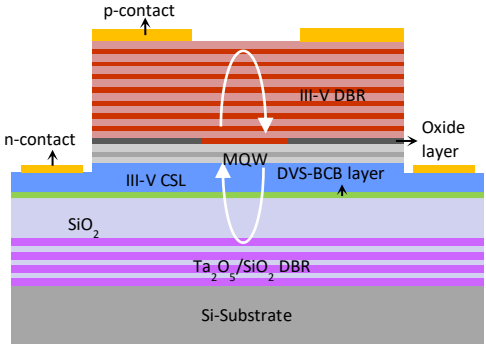

Fig. 1 Schematic cross-section of the Gen1 VCSEL device (surface emission).

The GaAs half VCSEL was bonded to a dielectric DBR on Si using a thin layer of DVS-BCB. After bonding, the GaAs bulk substrate was removed using complete wet chemical etching and the GaAs VCSELs were fabricated using standard VCSEL processing steps [9].

With this technology, we successfully demonstrated high performance Gen1 HC-VCSELs operating at 850 nm with surface emission having sub-mA threshold current, >2 mW output power (Fig. 2(a)), and 25 Gbit/s modulation speed (Fig. 2(b)). A cross-section of the device structure is shown in Fig. 3(a), showing the dielectric DBR, the bonding interface and the III-V half VCSEL with oxide aperture. Coplanar ground-signal-ground electrodes were defined for high-speed characterization as shown in Fig. 3(b). We also saw experimentally that the bonding layer thickness can be used to optimize a certain performance parameter

at a given temperature or to minimize the variation of performance over temperature [10].

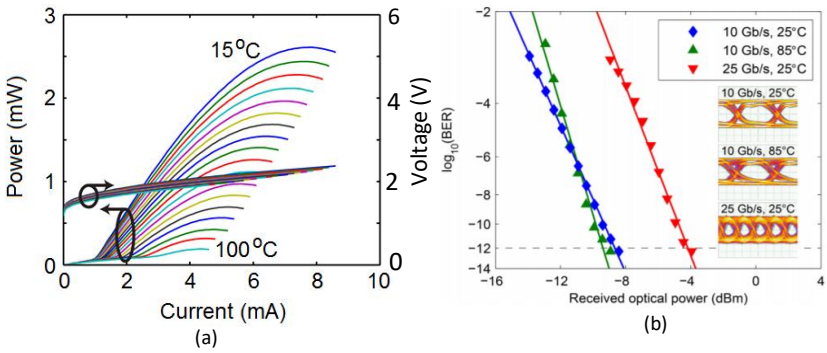

Fig. 2 (a) Output power and voltage versus current for a device with a ~65 nm bonding layer thickness and 10 µm oxide aperture, measured at ambient temperatures ranging from 15 to 100 °C in steps of 5 °C. (b) Measured BER versus received optical power for a 5 µm oxide aperture device with a ~65 nm bonding layer thickness at data rates up to 25 Gbit/s at 25 °C and 10 Gbit/s at 85 °C. Insets: corresponding optical eye diagrams (scales: 100 mV/div and 20 ps/div)

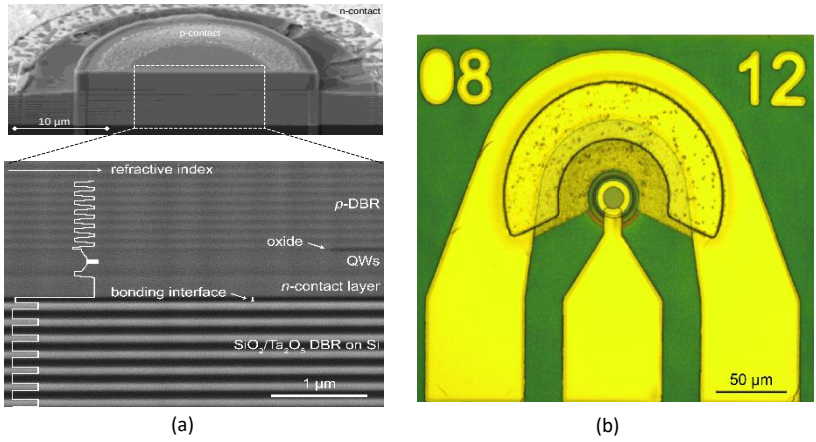

Fig. 3 SEM images of a focused ion beam cross-section (left) and microscope top image (right) of a fabricated HC-VCSEL.

Further, to be able to couple the vertically amplified light into a SiN waveguide, the next step is to add a SiN waveguide structure with shallow etched grating on top of the dielectric DBR, before adhesively bonding the GaAs half

VCSEL. Therefore, we numerically investigated the possibility of coupling the output of the HC-VCSEL to an in-plane SiN waveguide using an intra-cavity diffraction grating. As these VCSELs are integrated with a SiN waveguide, we refer to it as Gen2 vertical cavity Si-integrated lasers (Gen2 VCSILs). We proposed a design of an intra-cavity grating/dielectric DBR combination with following advantages [11]:

- It allows the heterogeneous integration of GaAs-based vertical cavity light sources on a SiN waveguide circuit,
- It selects the polarization state of the light generated by the VCSIL,
- It can provide good transverse mode control
- High efficiency waveguide coupling can be obtained
- As demonstrated in [9], the alignment is determined by lithography after the heterogeneous integration of the III-V material.

A schematic of a Gen2 VCSIL is shown in Fig. 4. The reflection (fraction of incident light that is reflected) and single-sided coupling coefficient (fraction of incident light that is coupled to one side of the SiN waveguide) of these grating/dielectric DBR combinations depend on the size of the oxide aperture of the GaAs VCSIL and a VCSIL with aperture size > 4µm is required to have a polarization selective intra-cavity grating/dielectric DBR combination with sufficient reflection and coupling of the fundamental transverse electric (TE) mode into the SiN waveguide.

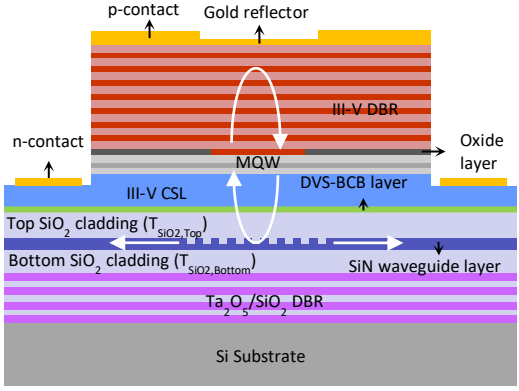

Fig. 4 Schematic cross-section of the Gen2 VCSIL device with in-plane out-coupling into a SiN waveguide.

For a Gen2 VCSIL with aperture size of 5 µm, the reflection and single-sided coupling coefficient of the grating/dielectric DBR combination with a grating period of 530 nm, 50% duty cycle (DC) and etch depth 30 nm is shown in Fig. 5.

From the characterization results of surface emitting Gen1 VCSELs, we found that the VCSELs operating at 855 nm have superior room temperature performance in terms of optical power and threshold current [10]. Therefore, we designed the Gen2 VCSIL to operate at 855nm.

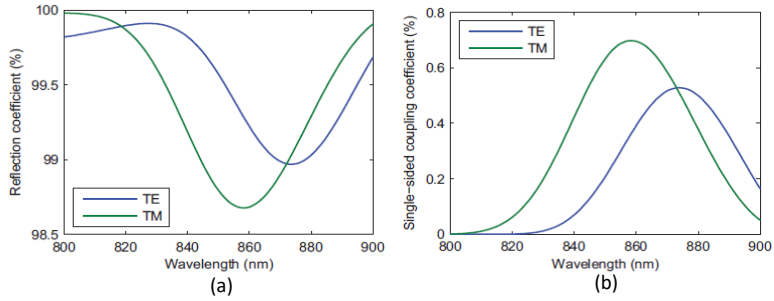

Fig. 5 (a) Simulated reflection coefficient and (b) single-sided coupling coefficient of the intra-cavity grating/dielectric DBR combination as a function of wavelength for TE and TM polarizations. (grating period = 530 nm, DC = 50%)

From Fig. 5 (b) it can be seen that the grating is designed to operate far from the center Bragg wavelength for coupling the vertically propagating light into the SiN waveguide. In particular the TE mode (electric field parallel to the grating lines) operates further away from the Bragg wavelength than the TM mode (electric field perpendicular to the grating lines). This results in higher cavity losses for the TM mode, which can be used to suppress the TM mode from lasing, i.e. set the lasing polarization state of the VCSIL to TE.

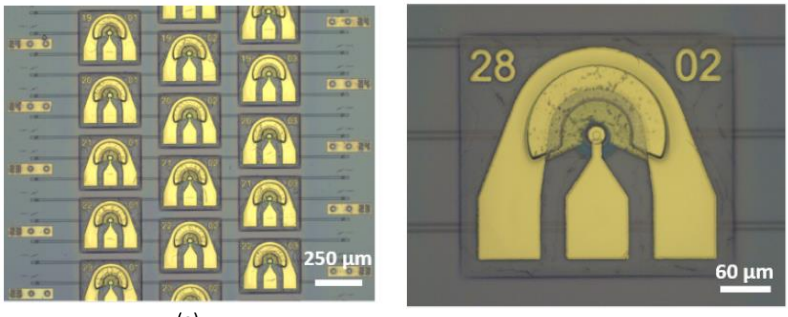

Fig. 6 Optical micrographs of (a) an array of fully processed Gen2 VCSILs and (b) a single Gen2 VCSIL.

We successfully demonstrated Gen2 VCSILs operating at ~856 nm with TE polarized laser output coupled into SiN waveguides. Fig. 6 shows microscope images of fully fabricated Gen2 VCSILs on top of intra-cavity gratings and waveguide structures. A Gen2 VCSIL with a 5 µm oxide aperture diameter has a threshold current of 1.13 mA and produces a maximum single-sided waveguide-coupled output power of about 73 µW (Fig. 7(a)) with side mode suppression ratio (SMSR) of 29 dB (Fig. 7(b)).

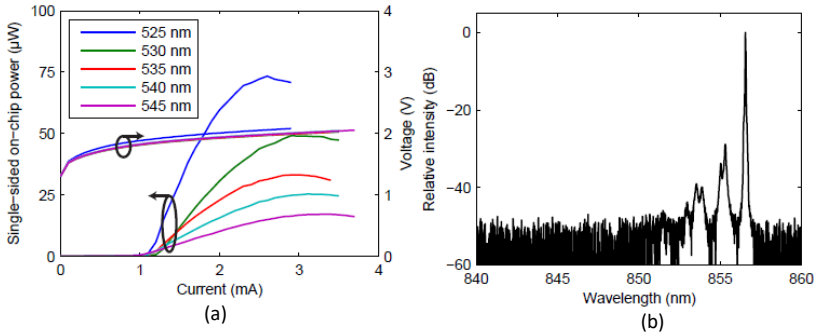

Fig. 7 (a) Waveguide-coupled light-current-voltage characteristics for 5 µm oxide-aperture diameter VCSILs with intra-cavity grating periods ranging from 525 - 545 nm (after gold deposition on surface). (b) Spectrum for the 525 nm device operated at 2.5 mA.

The performance of both the Gen1 VCSEL and Gen2 VCSIL was to a large extent limited by the high thermal impedance due to the dielectric DBR. The thermal impedance of the Gen1 VCSEL and Gen2 VCSIL with 5 µm aperture size are 3 and 4 times higher than that of an ordinary VCSEL of the same aperture size respectively [12]. Further, the performance of the Gen2 VCSILs is inferior to Gen1 VCSELs due to additional unexpected cavity losses, which we attribute to surface roughness associated excess scattering. To improve the performance of these integrated VCSELs, the dielectric DBR can be replaced by a DBR with high index contrast, such as an a-Si/SiO_2 DBR, thereby reducing the number of DBR pairs required and by integrating a metallic heat spreader to improve the thermal impedance of the device.

Throughout this work, the design and fabrication of SiN photonic integrated circuits (PICs) and the heterogeneous integration process to attach GaAs half VCSELs to SiN PICs were done by the author. The design of the complete VCSEL was done by Johan Gustavsson from Chalmers University of Technology. After heterogeneous integration of the GaAs half VCSEL epitaxy, the fabrication of the Gen1 VCSEL and Gen2 VCSEL together with its characterization was done

by Emanuel. P. Haglund, Chalmers University of Technology as part of his PhD work.

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1

Introduction

The goal of this thesis is to demonstrate on-chip integrated lasers on a silicon nitride (SiN) waveguide circuit, operating in the near-infrared (NIR) wavelength range. In general, an ideal light source offers: a wide tuning range, a narrow linewidth, high output power, low power consumption, reliable performance over a long period, compactness, and low sensitivity to temperature. It is challenging to meet all these requirements at once. Different types of lasers such as edge emitters (Fabry-Perot laser diodes, distributed feedback (DFB) lasers, external cavity lasers) and monolithic vertical cavity surface-emitting lasers (VCSELs), exist covering the visible, near-infrared and mid-infrared spectral range. VCSELs, compared to edge-emitting lasers, are very suitable as devices for optical interconnects on Si platforms. The success of the VCSEL arises from a combination of unique properties. The most important are:

- low threshold currents smaller than 1mA and correspondingly small driving currents for required optical output powers in the mW range, thus minimizing power consumption and making the design of electronic driver circuits easier,
- excellent digital modulation behavior for data rates nowadays >70 Gbit/s,
- high power conversion efficiencies of more than 60% and thus low power dissipation,
- circular beam profiles with small divergence angles, simplifying the design of beam-shaping optics,
- a wide operational temperature range exceeding +125°C that enables uncooled operation, even in automobiles,

- the straightforward formation of homogeneous one- and two-dimensional laser arrays as the key to compact space division multiplexed data transmission,
- complete testing and device selection on wafer level, yielding enormous cost reduction compared to edge-emitting laser diodes,
- the use of mounting and packaging technology that are well known from light-emitting diode (LED) production, and finally
- very high reliability with projected lifetimes on the order of ten million hours at room temperature.

In this thesis, we limit ourselves to VCSELs, and in particular to GaAs VCSELs due to their relevance in the field of biophotonics and short-wavelength optical interconnects.

1.1 Photonic applications of integrated VCSELs

1.1.1 Optical spectroscopy

Optical spectroscopy has gained wide acceptance in several fields due to its proven effectiveness as a technique for non-destructively analyzing chemical content of samples in development or production. The traditional optical spectroscopic systems rely on expensive and bulky instrumentation prohibiting their dissemination in non-laboratory environments. In recent years, there has been a large demand for hand-held devices such as medical point-of-care devices, body implants for monitoring of glucose levels, and sensing devices integrated in smartphones that are capable of accurate, sensitive, and in situ spectroscopic detection of a variety of substances. If key parts of the optical functionality could be integrated in the form of a chip, the route would be opened to miniaturized low-cost systems, with the potential of massive parallelism and multiplexing [1-7]. An integrated photonics approach using a high index contrast material can provide a compact solution enabling integration and miniaturization of several active and passive optical components on a single chip. The most prominent high-index contrast photonic integration platform is Si photonics. By leveraging the well-established CMOS manufacturing infrastructure, Si photonics allows for mass-producible, high-yield photonic chips. Fig. 1.1 shows an example of an on-chip multi-degree of freedom sensor to detect the presence of biological substances using micro-ring resonators.

Currently, the field of on-chip spectroscopy is still very immature as compared to free-space spectroscopic systems, but the progress is very rapid. There have been reports on various of proof-of-concept on-chip demonstrations for absorption [5], fluorescence [6] and Raman spectroscopy [7] using an external

light source. In spite of all the promise, there also remain enormous challenges to integrate efficient light sources with PICs (e.g., Si photonics) in order to realize the dream of on-chip spectroscopic systems.

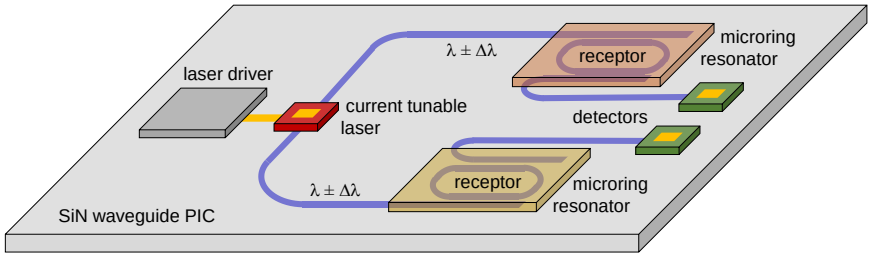

Fig. 1.1 Multi-DoF (degree of freedom) sensor on chip, reproduced from [8].

1.1.2 Optical interconnect

Another application of integrated laser sources relevant to this thesis, is short-reach optical interconnects. A brief comparison between electrical and optical interconnects is given in [9]. Until recently, interconnects were based on electrical copper cables. However, fundamental limitations of copper as an interconnect medium in terms of loss, dispersion, and crosstalk are becoming significant as interconnect density and speed is rocketing. The ever-growing demand for the data has forced the move to optical interconnects, where higher data rates, longer reach, and lower power consumption are achieved by optical links [10]. It is believed that the optical interconnect has the potential of shortening delays over the electrical interconnect [11], as it can provide larger bandwidth density for buses and networks than electrical interconnects and an increased data capacity can be provided by wavelength division multiplexing [12]. The typical light source in such optical interconnects is the directly modulated GaAs-based vertical-cavity surface-emitting laser (VCSEL), due to its low-cost fabrication, energy-efficient operation, and high bandwidth at low drive currents [13]. Commercial VCSELs capable of data rates up to 28 Gbit/s are currently available from several manufacturers [14]. However, data rates of 40, 50, and even 100 Gbit/s are expected in future standards, which will require even faster VCSELs.

One expected roadmap for optical interconnects is illustrated in Fig. 1.2. It shows how optical interconnects are replacing copper interconnects in the communication distance versus volume frame. To date, most of the optical interconnect range from a few meters up to a few hundred meters, but the majority of the links are below 30 m. In the future, it is expected that even shorter links, e.g., board-to-board, chip-to-chip, and on-chip interconnects would benefit from

the higher speed and efficiency of the optical interconnects. However, this requires tighter integration between the electronic and the photonic integrated circuits (PICs). Since the material of choice for electronic circuits, Si, cannot be used to produce efficient light sources, one possible route is the heterogeneous integration of GaAs-based VCSELs on a Si-based platform for PICs, compatible with standard CMOS fabrication.

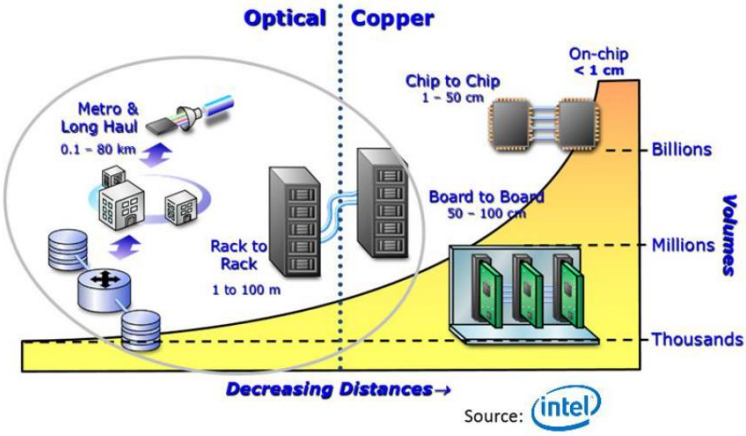

Fig. 1.2 Optical interconnects roadmap in data communication networks.

1.2 Relevance of the NIR wavelength range

An optical spectroscopic technique employs either the visible (VIS), the ultraviolet (UV) or the infrared (IR) electromagnetic spectrum. The most prominent among these is the IR wavelength region. The infrared wavelength region refers to wavelengths longer than visible but shorter than the microwaves. It can be further divided into 5 subsections: near-infrared (NIR, 0.7-1.0 μm), short-wave infrared (SWIR, 1.0-3.0 μm), mid-wave infrared (MWIR, 3.0-5.0 μm), long-wave infrared (LWIR, 8.0-12.0 μm), far infrared (FIR, 12.0-30.0 μm). These definitions are not strict and the wavelength boundaries can vary slightly. Most biological species and processes are probed in the visible and near-infrared (400-1000 nm wavelength), and of particular interest is the therapeutic window in the very-near-infrared (750-930 nm wavelength) where there is minimal photo-damage to cells and negligible water absorption. Furthermore, in this wavelength range, there is a large availability of light sources with high performance and low cost as well as high-performance Si-based photodetectors. Therefore, the NIR wavelength range is particularly relevant for Raman spectroscopy and fluorescence spectroscopy.

For applications in optical data transmission, there are three main wavelength windows: (a) 750–900 nm, (b) 1260–1360 nm, and (c) 1460–1625 nm. These three wavelength windows have negligible OH absorption in fiber. Therefore, for applications in telecommunication, window (b) and (c) are mainly used whereas window (a) cannot be used due relatively large Rayleigh scattering. However, window (a) can still be used for short-distance data communications where scattering loss can be ignored.

Due to the overlap of interest in optical sensing and short-reach datacom applications in the NIR wavelength range, 850 nm wavelength devices integrated on a Si-based photonic platform are of particular interest in this thesis.

1.3 Passive waveguide platform for near-infrared (NIR) wavelengths

Tremendous efforts have been invested in research, development, and industrialization of Si photonics over the past decades. As a result, Si photonics has emerged as a mature technological platform for optical datacom and telecom applications at 1300 and 1550 nm. Over the past few years, we have witnessed Si photonics products finding their way in the market. However, for applications requiring shorter wavelengths, Si cannot be used due to the absorption in Si below 1.1 μm. Instead, silicon nitride (SiN) can be used as a substitute of Si, providing similar circuit compactness, resulting from the moderately high refractive index contrast between SiN ($n \approx 2$) and silicon dioxide (SiO_2, $n \approx 1.5$). It can also be manufactured using the same CMOS fabrication infrastructure as Si. The material stack used for SiN-based photonics is similar to SOI-based silicon photonics. The only difference is that the guiding Si layer is replaced by a layer of SiN, which can either be deposited by Low Pressure Chemical Vapour Deposition (LPCVD) at high temperature (>700 °C) or by Plasma Enhanced Chemical Vapour Deposition (PECVD) at low temperature (<400 °C) [15]. LPCVD-based SiN is typically close to stoichiometric Si_3N_4. However, it has large internal tensile stress. LPCVD SiN provides an excellent control over the homogeneity of material index and thickness. PECVD-based nitride has a composition that depends strongly on the deposition conditions and can be Si-rich (higher refractive index) or nitrogen-rich (lower refractive index). A review of Si and SiN-based PICs for application in spectroscopic sensing can be found in [2] and a detailed comparison between the two platforms was published in [4].

Using PECVD SiN, a waveguide loss of ~1.5 dB/cm has been demonstrated for the visible and the very near IR wavelength range for strip waveguides [15]. All the essential passive optical components such as grating couplers [16-18], planar concave gratings [19], arrayed waveguide gratings [20], Mach-Zehnder

interferometer filters [21,22], ring cavity filters [23] and Bragg gratings [24] have also been demonstrated on a SiN-based photonics platform. However, the realization of integrated light sources on SiN is still a major challenge.

The fact that SiN can be deposited by a LPCVD or PECVD deposition technique implies that there is a lot more flexibility to combine the SiN waveguides with other photonic structures than is the case for SOI waveguides. As an example, one can deposit the waveguide layer on top of a DBR-mirror or metal mirror and thereby boost the efficiency of standard grating couplers [17], [18]. In [17], this approach has led to the demonstration of fiber-chip coupling efficiencies of ~60% for focusing grating couplers operating at 0.66 μm wavelength.

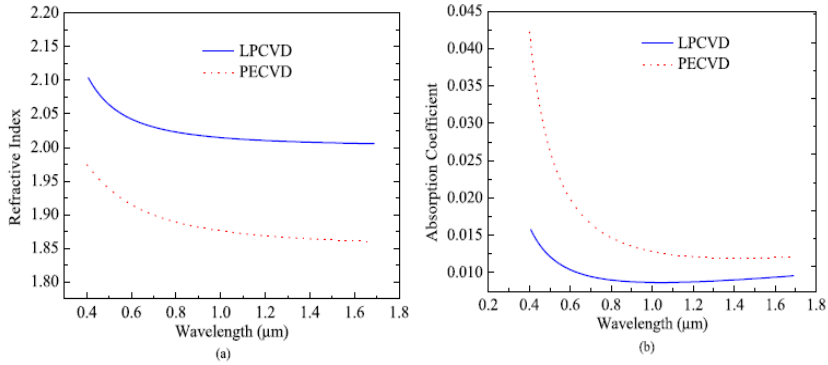

Fig. 1. 3 (a) Refractive index and (b) the absorption coefficient of typical LPCVD and PECVD SiN for wavelengths ranging from 0.4 μm to 1.68 μm, reproduced from [4].

In this thesis, the Si_3N_4 waveguide circuits are fabricated on top of Ta_2O_5/SiO_2 dielectric DBRs deposited on 200 mm diameter Si wafers with a thickness of 700 μm. The Si_3N_4 as well as the SiO_2 are deposited by PECVD and the waveguide structures are defined with e-beam lithography and subsequently etched by a reactive ion etching process to get the final structure.

1.4 Integration approaches

In spite of all the unique advantages that Si photonics has to offer, the indirect bandgap of Si and its compatible compounds, such as SiN and SiGe hampers efficient light emission. Over the years, many approaches have been proposed to bring coherent light onto the Si PIC. Therefore, to couple light into the Si chips the following options are available:

- through coupling an external light source to the SOI chip, but this is not an attractive solution due to the high packaging costs involved.
- through epitaxial growth of high quality, defect-free films of III-V on a Si substrate. Recently an optically pumped epitaxially grown InP DFB laser [25] and a quantum dot laser on Si [26] has been demonstrated.
- through light generation in Si itself by making use of the nonlinear effects in Si (e.g., super continuum sources) [27].
- through heterogeneous integration of III-V materials such as GaAs, InP, etc. that are excellent light emitters [28].

Because of the direct bandgap and high optical gain in III-V materials, it is highly appealing to integrate III-V lasers on Si. Directly mounting pre-fabricated III-V lasers using flip-chip or pick-and-place technology is currently preferred by the industry [29-31]. It allows the pre-selection of known-good lasers, but the limited alignment tolerance and the high packaging cost make it unsustainable for further scaling. On the other hand, the direct epitaxial growth of III-V materials on Si holds promises for high integration density and low cost [25,26] but is not yet very mature in terms of yield and device performance. As an intermediate step, wafer bonding based heterogeneous integration has been widely explored in the past decade and has proven to be the most successful approach up to now for III-V laser integration on Si. Several bonding techniques, such as direct bonding (using Van der Waals forces) and adhesive bonding, have been utilized to demonstrate various laser sources on Si. A review of the wide range of heterogeneously integrated devices obtained through adhesive bonding is presented in [28]. In the past few years, heterogeneously integrated III-V/Si lasers have evolved at a rapid pace with considerable enhancement in laser performance.

A semiconductor laser that is nowadays widely used for data communication, sensing, and high power applications is the vertical-cavity surface-emitting laser (VCSEL). Its success stems from the small optical mode and gain volume, which enables efficient operation and high-speed modulation at low currents. Another advantage is the vertical geometry giving surface emission, which enables low-cost fabrication and testing. This raises the question whether VCSELs, or VCSEL-like lasers, can be used as light sources for Si photonics, thereby bringing advantages of conventional VCSELs in terms of low currents, high efficiency, and small footprint to Si photonics. This challenging problem forms the central goal of this PhD work.

1.5 State of the art on Si integrated VCSELs

One of the hybrid integration approaches is to flip chip commercial VCSELs to a Si/SiN PIC. Flip-chip integration of long-wavelength (InP-based) and short-

wavelength (GaAs-based) VCSELs over optical coupling elements (gratings or mirrors) on Si photonic PICs has indeed been explored for light source integration [29-31]. To flip chip VCSELs onto Si, the use of vertical grating couplers (VGC), where light is coupled in perpendicular to the surface, is the most straightforward solution with ease in fabrication. However, a VGC suffers from a second order diffraction and limits the maximum coupling efficiency to 50%. A flip chipped VCSEL on such a VGC was reported in [29]. A solution to avoid the unwanted second order reflection in case of a VGC is to tilt the incident light by a small angle with respect to the surface normal direction [32]. This makes the fabrication process challenging. To overcome this challenge, a VCSEL was flip-chipped onto a polymer micro prism incorporated on top of the grating coupler using laser ablation [30] and at a tilted angle [31]. However, the coupling efficiency was still low in the above reported integrated VCSELs due to the polarization uncertainty of the VCSEL. To further improve the coupling efficiency, a grating with optical feedback to control the polarization of the VCSEL can also be used. Another hybrid integration was demonstrated in [33] where a commercial VCSEL was bonded to an apodized vertical grating coupler (VGC) providing external optical feedback (OF) to maintain the polarization state. Despite having an advantage of pretesting of lasers prior to assembly with the Si/SiN PIC, these techniques suffer from not being wafer scale processes and require accurate and time-consuming alignment of individual devices.

Another integration approach is heterogeneous integration with the advantage of being a wafer scale process. A Si-based high-contrast grating (HCG) gained interest in order to form a hybrid cavity VCSEL with advantages such as polarization selection with transverse mode control, a substantial reduction in epitaxial material thickness and larger fabrication tolerance. There have been demonstrations of a heterogeneously integrated optically pumped VCSEL with output coupled to in-plane Si waveguides using a 1D HCG [34] and a 2D polarization independent HCG [35]. Another flip-chipped electrically pumped hybrid VCSEL with Si HCG was demonstrated in [36]. In this thesis, we report the first demonstration of a heterogeneously integrated electrically-pumped VCSEL with coupling to a SiN-based waveguide.

Table 1.1 shows the comparison of present VCSELs integrated on Si-based waveguides by flip-chip and heterogeneous integration in terms of threshold current, maximum power, maximum slope efficiency, and side mode suppression ratio (SMSR).

Table 1.1. Comparison with other VCSEL-on-SiP assemblies.

	Wavelength (nm)	Threshold current (mA)	Max. on-chip optical power (mW)	Max. slope efficiency (W/A)	SMSR (dB)	Laser aperture radius (μm)
This work	855 nm	1.1	0.146 at 3mA	0.17	29	5
VCSEL on Si HCG[1] [35]	1570 nm	3	0.013 CW at 4.4 mA*	NA	>40	8
VCSEL on Si HCG[2] [36]	1580 nm	9	1 at 17 mA	0.3	>60	NA
VCSEL on SiP[3] [29]	NA	1.6	0.066 at 10 mA	NA	NA	NA
VCSEL on SiP[4] [30]	1550 nm	1	NA	NA	45	NA
VCSEL on SiP[5] [31]	1547 nm	1.25	0.138 at 13.5 mA	0.012	35	NA
VCSEL on SiP[6] [33]	1333 nm	0.7	0.126 at 3.7 mA	0.064	49	<6

*power converted from 1.15×10^6 photon counts at 115 μW optical **pulsed** pumping.
[1]: VCSEL was bonded with Si HCG (optically pumped);
[2]: VCSEL was flip-chip bonded with Si HCG;
[3]: VCSEL was flip-chip bonded with VGC;
[4]: VCSEL was flip-chip bonded with grating coupler using laser-fabricated microprism;
[5]: VCSEL was flip-chip bonded with grating coupler at tilted angle;
[6]: VCSEL was bonded with a chirped VGC with external optical feedback;

1.6 Outline of the thesis

The thesis is organized as follows. Semiconductor lasers, and in particular VCSELs, are introduced in Chapter 2, while the design of hybrid-cavity VCSELs by attaching a GaAs half VCSEL to SiN PICs on Si-integrated dielectric DBRs is presented in Chapter 3. The technologies to realize SiN PICs on Si-integrated dielectric DBRs are presented in Chapter 4, while the heterogeneous integration technology and the VCSEL fabrication processes are presented in Chapter 5. Chapter 6 describes the characterization of the VCSELs, and finally, a future outlook is given in Chapter 7.

1.7 Contributions in this PhD thesis

The work presented in this thesis was done in collaboration with Chalmers University of Technology. The SiN building blocks to integrate GaAs half VCSELs to a SiN waveguide on a dielectric DBR mirror on a Si substrate were designed and fabricated by the author at UGent. The heterogeneous integration process to attach the GaAs VCSEL to the Si-based photonic integrated circuits via adhesive bonding was developed and performed by the author at UGent. The

process to fabricate GaAs VCSELs and their characterization was carried out at Chalmers University of Technology.

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2

VCSEL Fundamentals

2.1 Introduction

Vertical Cavity Surface Emitting Lasers (VCSELs) are the most power efficient low current/low power semiconductor lasers available with demonstrated power conversion efficiencies exceeding 60% [1]. The success of the VCSEL arises from a combination of unique properties such as the possibility of a single mode output, excellent digital modulation with data rates exceeding 70 Gbit/s [2], operation over wide ambient temperature range exceeding +125ºC, small footprint, and inexpensive wafer scale processing and testing. Further, VCSELs operating in the NIR wavelength range have their importance in the field of optical spectroscopy and short-reach optical interconnects. In this chapter, the fundamentals of VCSELs will be presented in detail.

2.2 Semiconductor lasers

"Laser" is an acronym for Light Amplification by Stimulated Emission of Radiation. In general, every laser system essentially has an active/gain material placed between a pair of optically parallel and highly reflecting mirrors with one of them partially transmitting, and an energy source to pump the active medium. Amplification (or gain) achieved in a gain medium is a quantum mechanical process, where an incident photon can stimulate the emission of an identical photon (same wavelength, phase, direction) by de-exciting an electron from a high energy state to a lower energy state where the energy difference is the same as the energy of the incident photon. The emitted photon further oscillates between two

mirrors and passes every time through the gain medium attaining considerable amplification and emits through one of the transmitting mirrors. To ensure there is population inversion in the gain material, electrical or optical pumping of the active region must be used.

Lasers can be categorized in several different ways including wavelength and material type (such as gas, liquid, solid-state, and semiconductor lasers). In this thesis, we will restrict ourselves to semiconductor lasers. Semiconductor lasers are the smallest, cheapest, can be produced in mass, and are easily scalable. The gain medium in an electrically pumped semiconductor laser usually consists of a thin undoped (intrinsic) direct bandgap semiconductor sandwiched between *p*-and *n*-doped cladding layers with higher bandgap. These direct bandgap semiconductors are typically III-V semiconductor compounds (such as AlGaAs, InGaAs, and InGaAsP). The bandgap can be adjusted by varying the material composition of the ternary and quaternary compounds, which enables variation in the operating wavelength and thereby covers most of the visible, near-infrared and mid-infrared spectral range. When this junction is forward biased, electrical carriers (electrons and holes) start to accumulate in the active (intrinsic) region and radiative transitions can occur. To achieve lasing, the gain must be high enough to compensate all losses. At a certain current, referred to as the threshold current, the optical gain equals the cavity losses (mirror losses and internal losses), and the lasing threshold is reached. The material gain required to reach threshold (g_{th}) can be expressed as:

$$g_{th} = \Gamma \left[\alpha_i + \frac{1}{2L}\ln\left(\frac{1}{R_1 R_2}\right)\right] = \Gamma\left[\alpha_i + \alpha_m\right] \tag{2.1}$$

where Γ is the confinement factor, α_i is the internal absorption, α_m the mirror loss, L the cavity length, and R_1 and R_2 denote the respective mirror power reflectivities. Eq. 2.1 is referred to as the amplitude condition since it states that the amplitude of the electrical field must be the same after one round-trip in the cavity. At current injection levels exceeding the threshold current, all carriers injected in excess of the threshold carrier concentration are consumed by stimulated emission and contribute to the laser output. This leads to a self-regulating mechanism in the laser that clamps the carrier concentration and the gain at their threshold values and the output power increase rapidly at currents beyond the threshold.

For lasing to occur, the phase of the electric field must also repeat itself after one round-trip in the cavity, yielding the resonance condition:

$$\exp\left(-j\frac{2\pi}{\lambda_0/n_{eff}}\,2L\right) = 1 \;\Rightarrow \lambda_0 = \frac{2Ln_{eff}}{m} \tag{2.2}$$

where λ_0 is the lasing wavelength (in a vacuum), n_{eff} is the effective refractive index of the cavity, L is the length of the cavity and m is an integer number. The simplest possible semiconductor laser is the Fabry-Perot (FP) laser, which is an edge-emitting laser (EEL) where the cavity is formed in the plane of the active layer either by cleaving or etching the semiconductor crystal with the resulting semiconductor/air interfaces functioning as mirrors. The reflections at the cleaved facets, due to the high refractive index contrast between the semiconductor material and air, give enough feedback to achieve lasing together with the high gain over a relatively long distance along the cavity.

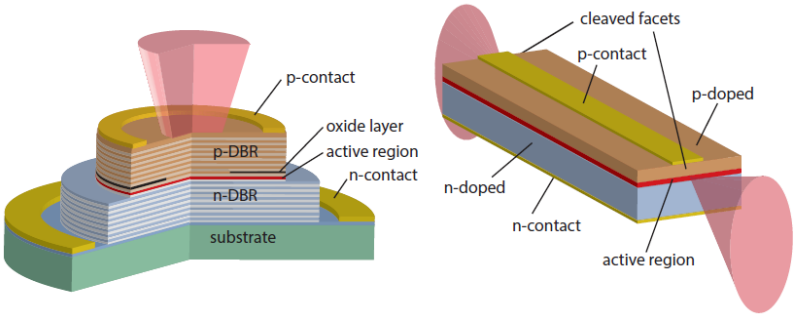

Fig. 2.1 (a) Cut-through VCSEL sketch. (b) Edge-emitting stripe laser.

Contrary to the EEL, the VCSEL, shown schematically in Fig. 2.1 (a), has a resonant cavity formed perpendicular to the plane of the active region layers. Feedback is provided by highly reflective DBR mirrors above and below this region, resulting in a very short effective resonator length (typically ~1 μm). Because of the short cavity length, VCSELs are fundamentally different from their FP EEL counterparts. The separation between the resonance wavelengths of an optical cavity (free spectral range) is inversely proportional to the length of the optical cavity. EELs with relatively long cavity lengths (100s of λ) have many longitudinal cavity modes that fall within the gain spectrum. In contrast, the short optical cavity length of a VCSEL (typically a single or few λ) implies that only one resonance will overlap with the laser gain bandwidth. However, a VCSEL typically has a relatively large cavity diameter **(**≈ 5-20 μm**),** which may permit numerous transverse spatial modes. Therefore, the VCSEL emission consists of a single longitudinal mode, but with possibly multiple transverse optical modes.

The small volume of the active region and the laser cavity give advantages in terms of low threshold and operating currents and high modulation bandwidth at low currents. Surface emission allows for a circular output beam cross-section and efficient coupling to an optical fiber. Even though the epitaxial growth of VCSELs

is complicated with low tolerances for error, the small footprint allows a large number of components to be fabricated on a single wafer (up to 6") in one single process run. Combined with the possibility of on-wafer testing before dicing and packaging, this can reduce high-volume fabrication costs dramatically compared to EELs. Surface emission also allows for simple integration of components into 1D or 2D arrays, making e.g., compact multi-channel data transmission [3] or power scaling from a typical ~10mW in a single VCSEL to well above 100W [4] possible for 2D arrays.

2.3 Bragg reflectors

Because of the short gain length, VCSEL mirrors must have a high reflection coefficient (>99%). Mirrors that can provide these levels of reflectivity are DBRs and high contrast gratings (HCGs). A DBR consists of an alternating sequence of high and low refractive index layers with thicknesses of one-quarter of the material wavelength. Multiple reflections at the interfaces of the DBR and constructive interference of multiple reflected waves increases the reflectivity with increasing number of pairs. The reflectivity of a DBR with m quarter wave pairs at the Bragg wavelength is given by

$$R_{DBR} = |r_{DBR}|^2 = \left(\frac{\left(\frac{n_1}{n_2}\right)^{2m} - \left(\frac{{n_1}^2}{n_0 n_t}\right)}{\left(\frac{n_2}{n_1}\right)^{2m} + \left(\frac{{n_1}^2}{n_0 n_t}\right)} \right)^2 \tag{2.3}$$

where n_0, n_1, n_2 and n_t are the respective refractive indices of the originating medium, the two alternating layer in DBR, and the terminating medium. The high-reflectivity bandwidth or stop-band of a DBR depends on the difference in refractive index of the two constituent materials, Δn. The spectral width of the stop band is given by

$$\Delta\lambda_{stop\ band} = \frac{2\lambda_{Bragg}\Delta n}{\pi n_{eff}}, \tag{2.4}$$

where n_{eff} is the effective refractive index of the mirror, given by

$$n_{eff} = \left(\frac{1}{n_1} + \frac{1}{n_2}\right)^{-1}, \tag{2.5}$$

Typically DBRs for VCSELs are either epitaxially grown semiconductors or consist of dielectric materials. The materials available for epitaxial DBRs have

relatively low refractive index contrast, which requires 20–30 DBR pairs for sufficient reflectivity, while dielectric materials have the possibility for much larger refractive index contrast and typically require less than 20 DBR pairs for sufficient reflectivity. Current transport through the semiconductor DBR mirror is an important issue. Although the hetero interfaces providing a large index difference are necessary for high DBR reflectivity, they also imply that many large energy band offsets are present. These discontinuities in the conduction and valence energy bands form potential barriers that impede current flow and can lead to high resistance. To avoid this problem, the hetero-interfaces between the DBR layers can be modified using composition grading along with specific doping profiles. A variety of compositional profiles between the DBR layers have been reported, including staircase [5], linear [6, 7] and parabolic [8] hetero-interface grading.

2.4 Matrix method and standing-wave pattern

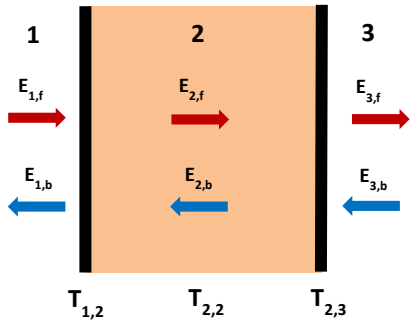

Fig. 2.2 Transmission matrices for a stack consisting of three media 1, 2 and 3 and two interfaces.

For the design of high-performance VCSELs, it is important to know the reflectivity spectra of the Bragg mirrors and the electric field distribution in the resonator. A commonly used model for one-dimensional calculations is the transmission or transfer matrix method [9]. The transfer matrix formalism handles plane waves and uses the fact that each interface between two isotropic dielectric media as well as each layer can be represented by 2 x 2 matrices, which are called transmission or transfer matrices T. Each transmission matrix relates forward and backward propagating field amplitudes $E_{1,f}$ and $E_{1,b}$ on one side of the interface or layer with the forward and backward propagating fields $E_{2,f}$ and $E_{2,b}$ on the other side:

$$\begin{pmatrix} E_{1,f} \\ E_{1,b} \end{pmatrix} = \begin{pmatrix} T_{1,1} & T_{1,2} \\ T_{2,1} & T_{2,2} \end{pmatrix} \begin{pmatrix} E_{2,f} \\ E_{2,b} \end{pmatrix} = T \begin{pmatrix} E_{2,f} \\ E_{2,b} \end{pmatrix} \tag{2.6}$$

The great advantage comes into play by using the transfer matrix method for multi-layered structures. For the complete stack of layers, one can simple multiply the corresponding T_i matrices of each individual layer and interface and so get the T_S matrix for the whole stack:

$$T_s = T_1 . T_2 \dots \dots T_i \dots \dots T_{N-1} . T_N \tag{2.7}$$

where N is the total number of layers and interfaces. This idea together with the definitions of the forward and backward directions is illustrated in Fig. 2.2. The transmission matrices can be easily calculated for plane waves and for the case of normal incidence for an interface between two media with refractive indices n_1, and n_2, and also for a layer with thickness L according to Equations 2.8 and 2.9, respectively,

$$T_{interface} = \frac{1}{t_{1,2}} \begin{pmatrix} 1 & r_{1,2} \\ r_{1,2} & 1 \end{pmatrix} \tag{2.8}$$

$$T_{layer} = \begin{pmatrix} e^{-j\beta L} & 0 \\ 0 & e^{j\beta L} \end{pmatrix} \tag{2.9}$$

with $r_{1,2}$ and $t_{1,2}$ given by the following equations:

$$r_{1,2} = \frac{n_1 - n_2}{n_1 + n_2} \tag{2.10}$$

$$t_{1,2} = \frac{2n_1}{n_1 + n_2} \tag{2.11}$$

The transfer matrix method is very simple to use and does not require noticeable computational power. Using this formalism in the present work 1D-simulations for DBR reflectivity spectra, cavity dip positions and field distributions inside of the cavity were carried out. One of the first tasks while designing a VCSEL is to decide how many DBR pairs for the top and the bottom mirror should be grown. This determines the reflectivity of both mirrors. Fig. 2.3(a) shows the reflectivity and phase spectra for the top $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$ DBR with 24 pairs used in the 845 nm QW-VCSELs. The second important task for a proper VCSEL design is to match the cavity wavelength to the desired value. For the VCSEL fabricated in this work, it was 845 nm. For this purpose, the position of the cavity dip was calculated with the transfer matrix method. Therefore, the reflection from

the complete VCSEL structure was simulated. If necessary, the thickness of the cavity should be adjusted in order to match the dip position to the desired wavelength. Fig. 2.3(b) shows the calculated cavity dip position for the 845 nm QW-VCSEL.

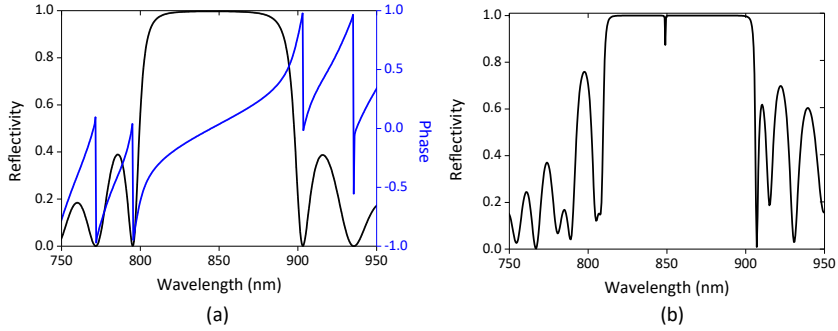

Fig. 2.3 (a) Reflectivity and phase as a function of the wavelength for 24 pairs of an $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$ DBR with air interface, (b) full VCSEL cavity dip position at 845 nm. The single narrow longitudinal resonance is seen at 845 nm.

2.5 Transverse confinement

As discussed above the VCSEL emission consists of a single longitudinal mode due to the short cavity length, but with possibly multiple transverse optical modes. To suppress higher order transverse optical modes in a VCSEL, the optical field needs to be confined in the transverse direction. Furthermore, the electrical current must be confined to pump only active material overlapping with the lasing mode. In most VCSEL designs the electrical and optical confinement originate from the same feature. Some examples of standard transverse confinement schemes are: etched air posts [10], the regrown buried mesa, ion implantation [11], buried tunnel junction (BTJ) [12], and oxide aperture [13], as illustrated in Fig. 2.4. Early VCSELs used the simple etched air-post structure shown in Fig. 2.4 (a) where the large refractive index difference at the semiconductor/air interface results in a strong index guiding of the optical field in the transverse direction. However, mesa etching incurs scattering losses for the optical field and may cause reliability problems from carrier recombination at the semiconductor-air interface. A further development from this basic structure is the regrown buried mesa VCSEL seen in Fig. 2.4 (b). By regrowing semi-insulating semiconductor material around the etched mesa, problems associated with the semiconductor/air interface can be eliminated, but the regrowth process is challenging.

Proton implantation has been the first method employed to fabricate commercial VCSELs with an excellent life time, reproducibility, and reliability [14,15]. By selectively implanting ions into the semiconductor material, it can be rendered electrically isolating, and the flow of the injected current can be controlled. Different ion species have been used, but protons (H+) are the most common choice. The proton implant confines the current, but it does not provide any inherent index guiding of the optical field. Instead, optical confinement is provided by gain guiding and thermal lensing (the temperature rise associated with the drive current produces a refractive index difference which gives rise to index guiding of the optical mode). However, this guiding is relatively weak and results in drive current dependent mode behavior [16]. Oxide-confined GaAs-based VCSELs (Fig. 2.4 (d)) utilize selective oxidation of high Al-content AlGaAs-layers to form the oxide apertures, which provides both electrical and optical confinement since the resulting oxide is isolating and has lower refractive index than the non-oxidized material. The selective oxidation introduces lower optical losses in the cavity and has led to a leap in VCSEL performance [17-20]. The vast majority of commercial VCSELs nowadays relies on oxide confinement.

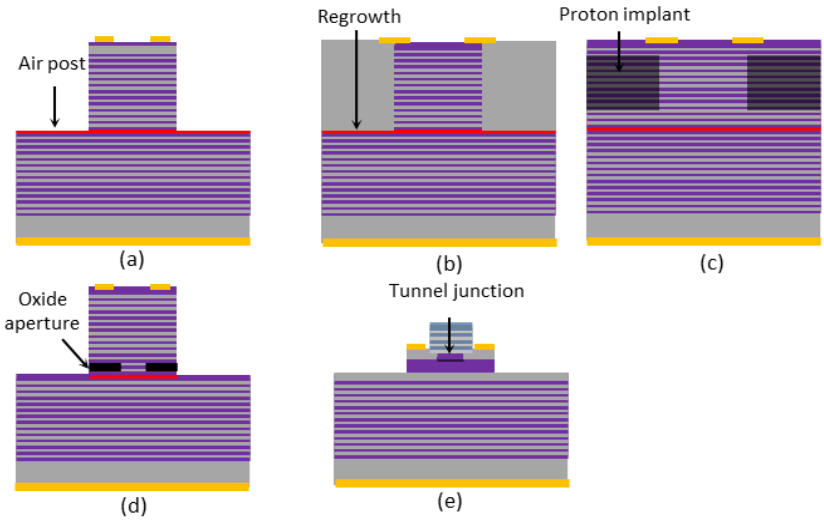

Fig. 2.4: Different electrical and optical confinement methods: (a) etched air post, (b) regrown mesa, (c) proton implantation, (d) oxide aperture, and (e) buried tunnel-junction.

For long wavelength InP-based VCSELs emitting at 1.3 and 1.55 µm, a buried tunnel junction is used for electrical and optical confinement since no high-quality oxide exists in this material system, see Fig. 2.4 (e) [12]. This technique is not

commonly used for electrical and optical confinement in GaAs-based VCSELs because of the difficulty to design effective tunnel junctions, the complex regrowth process required, and the excellent properties of oxide-confined VCSELs.

2.6 Thermal effects

Caused by the short optical resonator, the emission wavelength λ of a VCSEL is determined by the cavity resonance and not by the gain peak as in conventional EELs. Hence, the spectral alignment between the cavity resonance and the laser gain peak profoundly influences the performance of the VCSEL. Note that as temperature increases both the cavity resonance and the laser gain peak shifts to longer wavelengths. The thermal shift in cavity resonance is governed by a change in refractive index in the resonator due to resistive Joule heating by injected carriers. Consequently, the shift in cavity resonance depends on the material composition of the Bragg reflectors and the inner cavity. For a GaAs-based VCSEL, the thermal shift in the cavity resonance is typically found to be $\partial\lambda/\partial T \approx 0.06–0.09$ nm/K [21]. On the other hand, the active QWs show a shift of the gain peak wavelength λ_p according to $\partial\lambda_p/\partial T \approx 0.32$ nm/K mainly due to bandgap shrinkage [21].

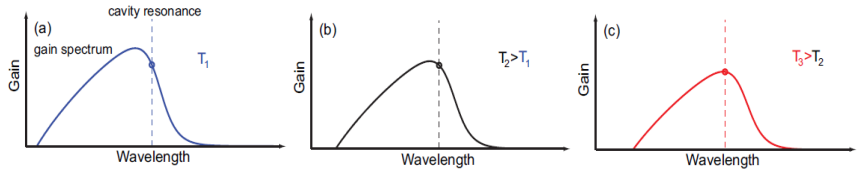

Fig. 2.5: Resonance/gain peak detuning with increasing temperature.

The best situation arises when the cavity resonance is aligned with the gain peak, where the lowest threshold current is obtained, but the differing shift rates with increasing current (and thus device temperature) leads to a spectral misalignment between the cavity resonance and the gain peak, leading to degradation of laser performance. Therefore, the cavity resonance is often intentionally designed to be at a slightly longer wavelength relative to the laser gain peak at room temperature, so that at higher current injection and thus, higher operating temperature, the laser gain peak shifts into alignment with the cavity resonance to yield optimal VCSEL performance [22]. Therefore, during epitaxial growth of the VCSEL, the cavity resonance/gain alignment can be designed to obtain low threshold or high output power at a particular temperature or to

produce relatively invariant threshold properties over a wide range of operating temperatures.

2.7 Dynamic effects

The intrinsic dynamics of semiconductor lasers is governed by the resonant interaction between the photons in the lasing modes and the injected electron-hole pairs in the active region. Therefore, for analyzing the intrinsic dynamic behavior of semiconductor lasers, a set of two coupled rate equations is formulated (Equations 2.12 & 2.13); one for the carrier density in the active region, and one for the photon density of the lasing mode in the cavity [9]. While these equations hold for a single mode laser, for a multimode laser one needs to introduce a rate equation for every lasing mode. However, with regards to total output power, the dynamic behavior of index guided multimode VCSELs with highly overlapping transverse intensity fields have uniform transverse carrier and photon densities [23]. Also, they exhibit a single resonance frequency very similar to a single mode VCSEL. This means that, in good approximation, it is sufficient to use only two rate equations, which are [9]

$$\frac{dN}{dt} = \frac{\eta_i I}{qV_a} - (AN + BN^2 + CN^3) - v_g GS, \tag{2.12}$$

$$\frac{dS}{dt} = \Gamma v_g GS - \frac{S}{\tau_p} + \Gamma \beta BN^2 \tag{2.13}$$

where N is the carrier density in the active region, η_i the internal quantum efficiency, I is the injected current, q is the elementary charge, V_a is the active region volume, which is equal to the oxide aperture area times the total thickness of the QWs, $AN+BN^2+CN^3$ is the recombination rate from spontaneous and non-radiative recombination, where A is the Shockley-Read-Hall recombination coefficient (Defect-related non-radiative recombination.), B is the radiative recombination coefficient, and C is the Auger recombination coefficient, v_g is the group velocity of the lasing mode, G the material gain, S is the photon density of the lasing mode, τ_p is the photon lifetime which is related to the cavity losses through $\tau_p = v_g.[\alpha_i + \alpha_m]$, and β is the fraction of photons generated by spontaneous emission that goes into the lasing mode.

2.7.1 Small signal frequency response

From the standard coupled rate equations (Equations 2.12 and 2.13), the intrinsic small signal modulation response of a single mode laser is a damped second order

system, which can be conveniently described in terms of a modulation transfer function:

$$H_i(f) = \eta_d \frac{hc}{\lambda_0 q} . \frac{{f_r}^2}{{f_r}^2 - f^2 + j\frac{f}{2\pi}\gamma} \frac{1}{1 + j\frac{f}{f_p}} \tag{2.14}$$

where $\eta_d$is the differential quantum efficiency.

Further, the electrical parasitics can be accounted for by an *RC*-filter modeled as an extra pole with cut-off frequency f_p [9]. The total modulation transfer function (intrinsic modulation response combined with electrical parasitics) can therefore be written as [9]:

$$H(f) = const. \frac{{f_r}^2}{{f_r}^2 - f^2 + j\frac{f}{2\pi}\gamma} \frac{1}{1 + j\frac{f}{f_p}} \tag{2.15}$$

The relaxation resonance frequency is given by

$$f_r = \frac{1}{2\pi}\sqrt{\frac{v_g . (\partial g/\partial n) . S}{\tau_p . (1 + \varepsilon S)}} \tag{2.16}$$

Where $\partial g/\partial n$ is the differential gain and ε is the gain compression factor. The increase of the resonance frequency with the current is typically quantified by the *D*-factor defined as

$$D \equiv \frac{f_r}{\sqrt{I - I_{th}}} \tag{2.17}$$

where $I - I_{th}$ is the injected current above the threshold.

The damping factor in (2.14) is given by [9]

$$\gamma = K . {f_r}^2 + \gamma_0 \tag{2.18}$$

where γ_0 is the damping offset and the K-factor is given by.

$$K = 4\pi^2 \left(\tau_p + \frac{\varepsilon}{v_g . (\partial g/\partial n)}\right) \tag{2.19}$$

2.7.2 Bandwidth limitations

The total modulation transfer function (2.15) has three parameters: the relaxation resonance frequency f_r, the damping factor γ and the cut-off frequency of electrical parasitics f_p. Accordingly, there are three types of limitations for the high-speed operation of a semiconductor laser. The damping limited 3dB intrinsic bandwidth (without parasitics and thermal effects) is limited by the K-factor [9] through:

$$f_{-3dB,damping} = \frac{2\pi\sqrt{2}}{K} \approx \frac{8.89}{K} \tag{2.20}$$

This limits the speed from the fact that the damping factor increases with the squared relaxation resonance frequency (2.18), while the bandwidth increases only approximately linear to it. Starting from some point, an increase in the damping factor overcomes the increase in the relaxation resonance frequency, and the bandwidth of the laser begins to decrease.

The second limitation is caused by the thermal effects, in fact by the internal laser heating, leading to an increase of the temperature of the active region. This is the so-called thermal limitation. Because temperature affects nearly each of the laser parameters used in the rate equations, the relaxation resonance frequency saturates at some current and starts to decrease at larger currents. Looking at (2.17) one can say that the D-factor and the threshold current are temperature dependent, and the D-factor decreases with temperature, while the threshold current increases. Thus there is a limit for the relaxation resonance frequency, and it becomes limited by a maximum value $f_{R,max}$. The thermally limited bandwidth ($f_{-3dB,thermal}$), estimated from [9] is:

$$f_{-3dB,thermal} \approx \sqrt{1+\sqrt{2}} \times f_{R,max} \approx 1.55 f_{R,max} \tag{2.21}$$

The third type of limitations is caused by the presence of electrical parasitic elements inside of the laser, mostly parasitic resistances and capacitances. These electrical parasitics build a low pass filter, preventing high-speed operation. With a given cut-off frequency of the electrical parasitics f_p, the maximum achievable bandwidth limited by electrical parasitic elements, estimated from [24] is:

$$f_{-3dB,parasitic} = (2+\sqrt{3}) f_p \approx 3.73 f_p \tag{2.22}$$

Fig. 2.6 shows the results of a typical near- 30 GHz VCSEL from [25], where the intrinsic bandwidth exceeds 60 GHz while it is reduced to less than 30 GHz after adding the effects of self-heating and electrical parasitic effects. Clearly, the speed of the VCSEL is largely limited by a combination of thermal effects and parasitic effects.

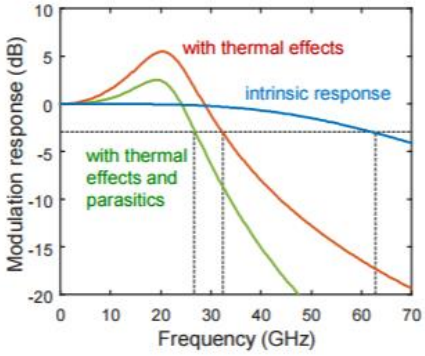

Fig. 2.6: Impact of thermal effects and parasitics on the VCSEL modulation response. Reproduced from [25].

2.8 VCSEL Modal Characteristics

The development of VCSELs has brought attention to the possibility of using it in integrated circuits. As a result, VCSELs are already an established transmitter in applications such as data communication and sensing. A single mode VCSEL with a polarization stable output power coupled into a waveguide is highly desirable in these fields. Unfortunately, VCSELs are surface emitting devices and they inherently have multiple-transverse modes due to their large lateral extent and an unpredictable polarization state as a result of the symmetric device layout and material isotropy. Below we will elaborate on various techniques that have been implemented for achieving single-mode, polarization-stable, and waveguide- coupled VCSELs.

2.8.1 Large area single-mode VCSELs

For a VCSEL to be referred to as single mode, a side-mode suppression ratio (SMSR) larger than 30 dB is typically required. As discussed in section 2.5, the lateral transverse mode confinement of GaAs VCSELs is done by a standard selective oxidation technique. However, higher order modes still exists when the waveguiding structure allows for it, generally above 3μm oxide aperture size. These higher order modes lase at slightly different wavelengths than the

fundamental mode, compromising the spectral purity of the laser, which is detrimental in sensing applications or mid and long distance optical communications links. Additionally, under modulation, the output power switches between the various modes, which is problematic for high-speed modulation in a dispersive environment. Thus, to achieve single mode devices for these applications, a small aperture size is typically used, precluding higher order modes. The drawback is that this also limits the maximum output power to a much lower value than could be achieved with a larger aperture. A small oxide aperture can also increase the diffraction losses, leading to higher threshold current, increase in differential resistance and lower output power. Further fabrication of small oxide aperture VCSELs requires a reproducible and uniform oxidation process. Since the oxidation rate is exponentially dependent on the temperature, a temperature variation across the wafer below 0.5°C is required [26]. Thus, there has been a search for ways to increase the size of the oxide aperture in a VCSEL, also increasing the power output, without losing the single mode optical characteristic.

One approach to engineer the waveguiding of the structure is by etching holes in the structure similar to a photonic crystal fiber [27] to force larger apertures to be single mode. This tends to also increase resistance and threshold of the device as well as add fabrication complexity. The use of an extended cavity also allows for single-mode emission from oxide-confined VCSELs with a large oxide aperture because of increased diffraction losses for higher-order modes with larger diffraction angles [28]. The large aperture reduces the electrical resistance which delays thermal roll-over and enables high single-mode power. However, such VCSELs are not truly single-mode since higher-order modes appear at high currents. With the thick cavity spacer needed for high single-mode power, such VCSELs are also susceptible to longitudinal mode switching because of the reduced longitudinal mode spacing. An alternative approach to eliminate the higher order modes is to add some differentiation in the loss seen by the fundamental and higher order modes. This can be achieved by etching of a shallow surface structure, called a mode filter, in the top layer of the VCSEL structure [29]. With this technique, single-mode operation can be achieved for devices with oxide aperture diameters as large as 7 μm.

Another approach to achieve a large area single mode device is to design a mirror for which the reflection is dependent on the angle of the incoming light. This can be achieved by using a one-dimensional (1D) subwavelength grating made of materials with a large refractive index contrast, hence named a high-contrast grating (HCG), [30]. The reflectivity for waves propagating in the surface-normal direction to the plane of an HCG can be designed to vary with incident angle, which has been shown to be effective in transverse mode control

[31]. Further, an HCG is capable of providing an extraordinarily broad bandwidth of high reflectivity for waves propagating in the surface-normal direction to the plane of gratings. Therefore, in an extreme case, the complete Bragg mirror of a VCSEL can be replaced by just a single layer HCG.

2.8.2 Polarization-stable VCSELs

Due to the complete isotropic nature of the gain material in the plane of the gain layer and the circularly symmetric resonator transverse geometry, the polarization direction of emitted light is random and is easily switched due to stress [32], injected current [33], or reflections [34]. Since a stable polarization is required for almost all sensing and some datacom applications, extensive and in-depth investigations have been undertaken during the last twenty years in order to stabilize the polarization of VCSELs without affecting their favourable operation parameters. Polarization control of VCSELs can be achieved by introducing a polarization-dependent gain, an asymmetric resonator, or mirrors with a polarization-dependent reflectivity.

The in-plane isotropy of the quantum well gain can be broken by introducing material gain anisotropy by growing VCSELs on GaAs (113) A and (113) B planes [35-39]. An active medium consisting of quantum wires [40] or structurally anisotropic quantum dots [41] can also provide a polarization-dependent gain under certain circumstances. However, the drawback is the rather difficult processing. Introducing a transverse anisotropy into the VCSEL cavity can also induce polarization dependent loss. Dumbbell-shaped [42], rectangular [43], or elliptical [44] mesas were the first representatives of this technique. They all aimed at polarization dependent scattering losses inside the laser cavity. However, these polarization dependent losses are weak.

Besides anisotropic gain and transverse anisotropy in a mesa structure, a mirror with a polarization-dependent reflectivity is also an attractive approach to control the polarization of VCSELs. Over the last few years, reliable polarization control of VCSELs by utilizing surface gratings has been proven not only in academic research [45] but has found its way into high-volume commercial products [46]. A polarization dependent reflectivity can be realized by patterning a properly designed grating with wavelength scale period [47] or a subwavelength grating on the top layer of a DBR [48]. This causes one polarization to see much higher loss within the structure, effectively preventing it from lasing. This concept has been demonstrated over the past few years. However, a grating with wavelength scale period has the drawback of diffraction losses introduced by the grating. Consequently, the threshold current is increased and the maximum output power are decreased. A subwavelength grating, on the other hand, is very attractive as it only allows the zeroth transmitted and reflected order to propagate.

Consequently, these gratings do not cause any diffraction (and therefore laser losses). However, the fabrication of gratings with such a small period is more challenging. Such subwavelength grating polarization stable VCSELs have been realized in [48]. Another subwavelength grating that can be used to realize a polarization stable VCSEL is an HCG grating which can provide an inherent reflectivity difference between TM and TE polarized light. This results in a largly polarization-dependent modal loss in the VCSEL cavity. Besides controlling the polarization and transverse mode of the VCSEL output, such gratings (HCGs) can also be used to realize tunable VCSELs [30].

2.8.3 Waveguide-coupled VCSELs

Gratings are an essential component for an integrated photonic circuit. They are often used to couple light in and out of an optical waveguide. Therefore, a grating can also be used to tap off the vertically amplified output of the VCSEL into an in-plane waveguide. There have been reports on flip-chipped VCSELs on a Si grating coupler to couple the vertical emission from a VCSEL to an in-plane Si waveguide [49-52]. As discussed in previous sections, the use of a grating can also control the polarization and transverse mode of the VCSEL. Recently a hybrid cavity vertical-cavity laser (VCL) with single-mode output coupled to an in-plane Si waveguide using a high contrast grating (HCG) has been demonstrated [53-55]. The heterogeneously integrated VCSELs presented in [53,54] were optically pumped with an output coupled to in-plane Si waveguides using a 2D polarization independent HCG [53] and a polarization dependent 1D HCG [54]. In [55] a flip chipped electrically pumped single-mode, polarization stable, hybrid cavity VCL with 1D Si HCG was demonstrated. The coupling between the vertical cavity and the in-plane waveguide is enabled by having a hybrid cavity, i.e. that the standing wave optical field extends over both the III-V material, containing the gain region, and the Si-based structure, containing the waveguide. A Si-based HCG gives an advantage of polarization selection with transverse mode control with a substantial reduction in epitaxial material thickness and large fabrication tolerance [56]. However, to operate at NIR wavelength, SiN is required [57]. SiN provides relatively low index contrast compared to Si, which requires the SiN high contrast grating to be free standing. This makes such a hybrid cavity approach very complicated in terms of fabrication [57].

In this thesis, we use an approach where a weak diffraction grating placed inside the VCSEL cavity can be used to tap off the vertically amplified output into an in-plane waveguide. This approach requires fabricating a grating within the cavity itself though, which enables integration of GaAs half VCSEL with SiN waveguide circuits using a hybrid integration approach. A similar approach has previously been explored for an all III-V semiconductor based design [58]. A brief

discussion on the design of such hybrid cavity VCSELs will be presented in Chapter 3.

2.9 Conclusion

In this chapter, a brief introduction to semiconductor lasers, in particular, VCSEL was presented. The optical, thermal, and dynamic effects in a VCSEL were also presented. We also addressed the issue of multimode VCSEL output and unstable VCSEL polarization with a review on various methods to overcome this. A review on techniques to integrate VCSELs with in-plane waveguides with polarization and transverse mode control were presented. A grating placed inside the cavity to control the polarization and transverse mode of the VCSEL is found to be an attractive route for heterogeneous integration of VCSELs and thus will be used in this thesis.

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3

Design of Si-integrated Hybrid Cavity VCSELs

3.1 Introduction

To facilitate a Si-based platform with an energy efficient laser source such as a VCSEL, a hybrid integration approach is required. In this chapter, we will describe the concept and design of such hybrid-cavity lasers. The chapter starts with a description of hybrid-cavity vertical cavity lasers followed by a design, where a GaAs half VCSEL is attached to a dielectric distributed Bragg reflector (DBR) on Si substrate, providing a surface emitting output. Further, this design is modified by implementing a weak diffraction grating in the hybrid cavity to tap off power to an in-plane SiN waveguide. The epitaxial layers of the GaAs half VCSEL and the VCSEL cavities were designed at Chalmers University of Technology using a home built software based on the conventional transfer matrix method, whereas the SiN PICs were designed at UGent using a commercially available finite-difference-time-domain (FDTD) software, Lumerical.

3.2 Hybrid-cavity vertical cavity laser (HC-VCL)

As discussed in Chapter 2, a hybrid-cavity VCL can be formed by attaching a GaAs half VCSEL to an optical reflector on the Si wafer.

Our approach to form a hybrid cavity laser is to bond an epitaxial half-VCSEL structure onto a dielectric distributed Bragg reflector (DBR) on a Si substrate, forming a hybrid cavity. By placing a waveguide with a weak diffraction grating

inside the cavity, between the dielectric DBR and the half-VCSEL, it is possible to tap off light into in-plane waveguides. As a first step in this direction, we designed a short wavelength VCSEL on Si, where a GaAs-based "half-VCSEL" is attached to a dielectric DBR on Si using ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB). These VCSELs are still surface emitting, and the sole purpose of such a design is to demonstrate a hybrid vertical-cavity laser suitable for development and implementation of the integration technique. It also allows for evaluating the impact of the high thermal impedance dielectric reflector on Si on the performance of heterogeneously integrated hybrid cavity VCSELs. We refer to this device as a Gen1: Hybrid-cavity Vertical Cavity Surface Emitting Laser (HC-VCSEL). The Gen1: HC-VCSEL was further modified by implementing a weak diffraction grating in the hybrid cavity to tap off power to an in-plane SiN waveguide. As these lasers were not surface emitting, we refer to it as a Gen2: Vertical-Cavity Si-Integrated Laser (VCSIL).

3.3 Gen1: Hybrid-cavity Vertical Cavity Surface Emitting Laser (HC-VCSEL)

3.3.1 Laser structure

The schematic of the Gen1 hybrid-cavity VCSEL is shown in Fig. 3.1. The structure comprises two distinct parts referred to as the top half-structure and the bottom half-structure. The top half-structure is a GaAs-based half-VCSEL, and the bottom half structure is the dielectric DBR on Si. A divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding layer is used to attach the top half-structure to the bottom-half structure.

3.3.2 GaAs half VCSEL

A GaAs-based half-VCSEL consists of a III-V active region with multiple quantum wells (MQWs), sandwiched between a III-V top DBR and a III-V current spreading layer (CSL). A layer to form an oxide aperture is also positioned in the top DBR mirror pair closest to the active region to provide current confinement and optical confinement in the VCSEL.
Therefore, the epitaxial device layers of GaAs half-VCSEL are as follows:

- The top GaAs p-contact layer has a thickness of $\lambda/2$, thereby producing an anti-phase reflection at the surface to facilitate post process tuning of the photon lifetime.
- The top DBR has 23 mirror pairs of p-doped $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$ layers with linearly graded interfaces and modulation doping.

- The III-V active region is a 1-λ-thick separate confinement heterostructure (SCH) containing a gain region with five 4 nm thick $In_{0.10}Ga_{0.90}As$ quantum wells (QWs) separated by 6 nm $Al_{0.37}Ga_{0.63}As$ barriers. The room temperature photoluminescence (PL) peak from the QWs is at 840 nm.
- The CSL is a 1-λ-thick n-doped $Al_{0.12}Ga_{0.88}As$ layer.
- The layer positioned in the top DBR mirror pair closest to the active region to form an oxide aperture via selective oxidation is a 30-nm-thick layer of $Al_{0.98}Ga_{0.02}As$.

Apart from the device layers, the epitaxial layers also contained etch stop and sacrificial layers, included at both sides of the device layers to ensure a clean surface prior to bonding and to enable substrate removal after bonding. More discussion about these layers will be presented in chapter 5.

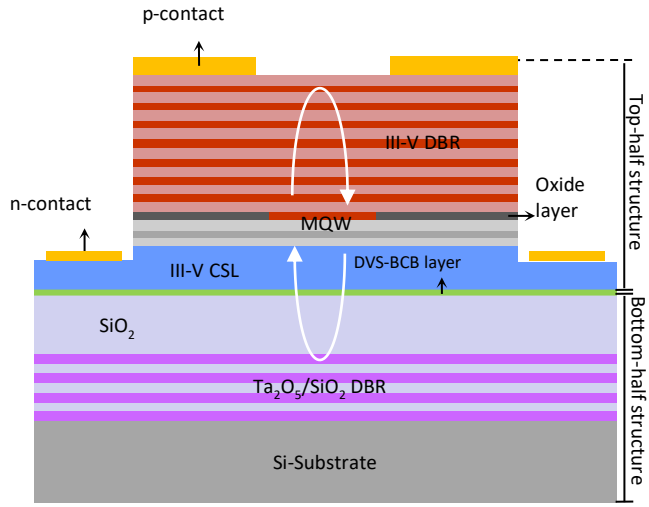

Fig. 3.1 Schematic cross section of the 845-nm-wavelength Gen1 HC VCSEL.

3.3.3 Dielectric DBR on Si

In this thesis, we used dielectric DBR layers on Si to replace the bottom III-V DBR. As discussed in chapter 2, VCSELs require DBRs with R >99 %. Therefore, a number of strict requirementss are placed on the material to be used. For example, the contrast in refractive index in the DBR layer must be high enough, there must be low optical loss in the materials, and the DBR interface must be

abrupt. In addition, the DBR materials should be able to be easily incorporated into existing processing technology.

A higher index contrast between the DBR layers results in higher reflectance and wider stopband with less DBR pairs. In comparison to semiconductor DBRs where losses arise from the free carrier absorption, dielectric DBRs are electrically insulating providing negligible extinction coefficient.

Table 3.1 List of dielectric materials transparent at 850nm

Material	Refractive index (n) at λ= 850 nm
a-Si	3.6
TiO_2	2.488
Ta_2O_5	2.12
SiN	1.93
SiO_2	1.47

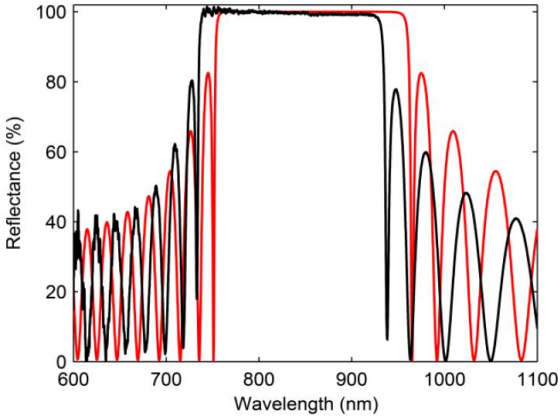

Fig. 3.2 Simulated (red) and measured (black) spectral reflectance for the 20-pair SiO_2 /Ta_2O_5 dielectric DBR on Si substrate, reproduced from [1].

For the low index material in the dielectric DBR, SiO_2 is a natural choice due to its extensive use in the CMOS industry. The refractive index of the SiO_2 used in this case is 1.47. As a higher index material in the DBR, few dielectric materials were explored and are listed in table 3.1. After careful analysis of the availability of the dielectric material to us, we proceeded with a Ta_2O_5/SiO_2 DBR. The DBR wafer with 20 pairs of Ta_2O_5/SiO_2 DBR layers deposited on polished Si was purchased from JDS Uniphase Corporation.

Fig 3.2 shows a comparison of simulated and measured reflectance spectra of the dielectric DBR with good agreement in terms of the width of the stopband

(~200 nm) and a slight blue-shift of the measured centre wavelength (~20 nm) relative to simulations.

3.3.4 VCSEL design

As can be seen from Fig 3.1, the GaAs half VCSEL and dielectric DBR pairs on Si substrate can be attached via adhesive bonding using a DVS-BCB layer, to form a hybrid VCSEL. An important task for a proper VCSEL design is to match the resonance wavelength of the cavity to the desired value. For the VCSEL fabricated in this work it is 845 nm. For lasing oscillation, the round trip phase must be an integral multiple of 2π. Therefore, the cavity length is adjusted by varying the thickness of the DVS-BCB such that the phase condition is fulfilled at 845 nm. The optical cavity properties are analysed using a 1D effective index model at 845 nm and are listed in table 3.2.

Table 3.2 Cavity parameters at a resonance wavelength of 845 nm, reproduced from [1].

Optical confinement factor	0.0173
Cold cavity Q	16200
Total loss (ps^{-1})	0.138
Top DBR transmission loss (ps^{-1})	0.053
Bottom DBR transmission loss (ps^{-1})	3×10^{-5}
Intra-cavity loss (ps^{-1})	0.085
Threshold QW gain (cm^{-1})	609
Photon lifetime (ps)	7.25

The intra-cavity loss is due to free-carrier absorption in the n-contact layer and the p-DBR. The variations of the real part of the refractive index and the intensity of the optical standing wave along the optical axis of the cavity are presented in Fig. 3.3. To the left of the bonding interface is the III-V "half-VCSEL" and to the right of the interface is the dielectric DBR on the Si substrate. As can be seen from Fig. 3.3, the active medium is placed at the anti-node of the optical field, in order to increase the interaction of the active material with the optical field. The oxide aperture is placed between a node and an anti-node for just enough index guiding.

The variation of the QW threshold gain and cavity resonance wavelength with the thickness of the bonding interface are shown in Fig. 3.4. It indicates that, over ~35 nm wavelength span (830–865 nm), the threshold gain is below 1000 cm^{-1}, which should allow for low threshold currents.

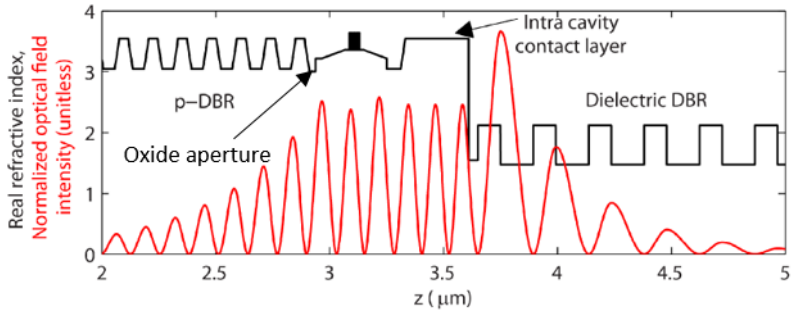

Fig. 3.3 Simulated standing-wave optical field intensity along the optical axis of the HC-VCSEL (red), together with the real refractive index profile (black), reproduced from [1].

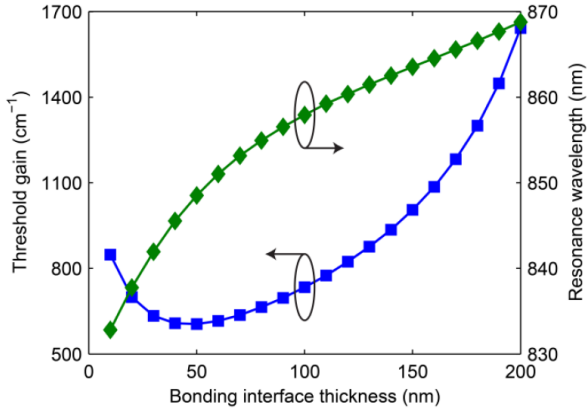

Fig. 3.4 Simulated dependence of resonance wavelength and threshold gain on bonding interface thickness, reproduced from [1].

3.4 Gen2: Hybrid-cavity Vertical Cavity Si-Integrated Laser (HC-VCSIL)

3.4.1 Laser structure

The schematic of the Gen2 hybrid-cavity VCSIL is shown in Fig. 3.5 (a). The structure again comprises of two distinct parts referred to as the top half-structure and the bottom half-structure.

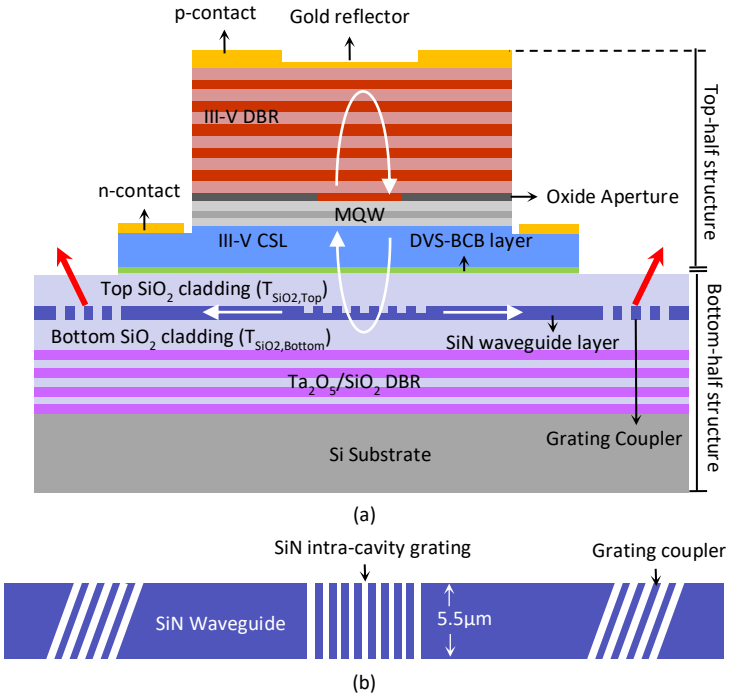

Fig. 3.5 (a) Schematic cross-section of the 855-nm-wavelength Gen2 HC-VCSIL with in-plane out-coupling. (b) Top view of the intra-cavity SiN grating with a waveguide and the grating coupler.

The top half-structure is the same GaAs-based half-VCSEL used in Gen1 VCSELs whereas the bottom half structure contains a weak diffraction grating etched in an intra-cavity SiN waveguide placed on top of the dielectric DBR used in the Gen1 VCSEL. The top and bottom SiO_2 cladding layers prevent the waveguide mode from leaking into the high index GaAs half-VCSEL and the high index dielectric DBR and Si substrate. A 50-nm-thick divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding layer is used to attach the top half-structure to the bottom-half structure, and a 200-nm-thick gold layer is placed on top of the p-doped DBR to avoid surface emission from the VCSIL and to reduce cavity loss. It also provides a more uniform lateral current injection into the QWs. As the arrows in Fig. 3.5 (a) illustrate, light is amplified vertically between the III-V top DBR and the intra-cavity grating/dielectric bottom DBR combination, and a fraction of this light energy is coupled out into a SiN waveguide. The intra-cavity grating is designed in such a way that the combination of the grating and the DBR reflects most of the light and couples a

small fraction of the light into the SiN waveguide (this is the designed dominant (useful) loss).

From our demonstrated Gen1 VCSEL devices, a VCSEL with resonance wavelength of 852 nm corresponding to a gain-to-resonance detuning of the -1 nm had superior performance at room temperature [1]. Therefore, the design of intra-cavity grating and hence the Gen2 VCSIL device to operate around that wavelength (855 nm) will be presented in the next section.

3.4.2 Intra-cavity grating design

The first challenge in this design is to prevent light guided by the SiN waveguide to leak away into the high index III-V material or bottom dielectric DBR and Si substrate. Therefore, the thicknesses of the top and bottom SiO_2 cladding layers, $T_{SiO2,Top}$ respective $T_{SiO2,Bottom}$ need to be sufficiently large to minimize this leakage loss. This leakage loss is estimated using commercially available software (FIMMWAVE, an optical mode solver from Photon Design).

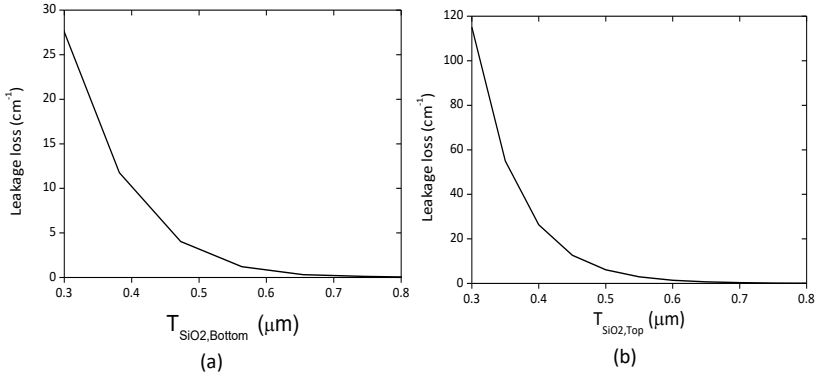

Fig. 3.6 Oxide cladded 5.5 μm × 300 nm SiN waveguide leakage loss as a function of (a) bottom oxide cladding layer thickness (855 nm wavelength, TE polarization), and (b) top oxide cladding layer thickness (855 nm wavelength, TE polarization).

The width of the SiN waveguide core is chosen in such a way that it is ~ 1 µm larger than the size of the fundamental transverse mode of the VCSIL to provide tolerance in misalignment of the VCSIL, which in turn is determined by the diameter of the oxide aperture. Therefore, for a VCSIL with oxide aperture diameter of 5 µm, the SiN waveguide core has the width set to 5.5 µm. An optimization of the oxide aperture will be presented in a next section. Fig. 3.6 (a) shows the leakage loss into the top half high index III-V material at 855 nm wavelength as a function of $T_{SiO2,Top}$ for the fundamental TE mode in a 300 nm

thick SiN waveguide core. A minimum thickness of 600 nm for $T_{SiO2,Top}$ is required to minimize the leakage loss. Moreover, the light guided by this waveguide should not leak into the bottom dielectric DBR and high index Si substrate either. Fig. 3.6 (b) shows the leakage loss into the bottom half of the structure at 855 nm wavelength as a function of $T_{SiO2,Bottom}$ for the fundamental TE mode. As can be seen from Fig. 3.6 (b), a minimum thickness of 600 nm for $T_{SiO2,Bottom}$ is required to minimize the leakage loss. In case the waveguide is tapered to a single mode SiN waveguide, $T_{SiO2,Bottom}$ needs to be > 800 nm to minimize leakage of the fundamental TE mode into the bottom dielectric DBR and high index Si substrate [4].

Next, numerical calculations for optimizing the intra-cavity grating design were performed using Lumerical, a commercial simulator based on the finite difference time-domain (FDTD) method. A 2D-simulation was performed on the bottom half structure of the Gen2 VCSIL shown in Fig. 3.7 (a). The bottom half structure of the VCSIL cavity contained the SiN (refractive index, n = 1.93) waveguide core with an integrated intra-cavity grating, the bottom SiO_2 cladding layer, and the 20 mirror pair Ta_2O_5/SiO_2 dielectric DBR. The quarter-wavelength-layers of Ta_2O_5 (n = 2.12) and SiO_2 (n = 1.45) have a thickness of 100 and 144 nm respectively. A Gaussian beam was launched from inside the top SiO_2 cladding layer (100 nm above the intra-cavity grating layer) perpendicular to the bottom half structure of the VCSIL cavity. Since the grating is placed inside the VCSIL cavity, the fraction of the light energy that is coupled to the SiN waveguide in a single cavity round trip must be made small, in order to maintain a low laser threshold gain. At the same time, the in-plane coupling should be the useful dominant cavity loss term in the laser in order to maximize the slope efficiency for the light coupled to the SiN waveguide. This means that other cavity losses from free-carrier absorption, oxide aperture scattering, and grating diffraction are to be minimized in the VCSIL design.

The main objective of the simulation was to design a weak coupling grating at 855 nm wavelength, for light polarized parallel to the grating lines (transverse electric, TE, mode). It should provide coupling of a small fraction of light into the SiN waveguide, and at the same time, it should introduce strong grating diffraction loss for light polarized perpendicular to the grating lines (transverse magnetic, TM, mode). This results in higher cavity loss for the TM mode, which can favorably be used to suppress the TM mode from lasing, i.e., set the TE polarization state for the light generated by the VCSIL.

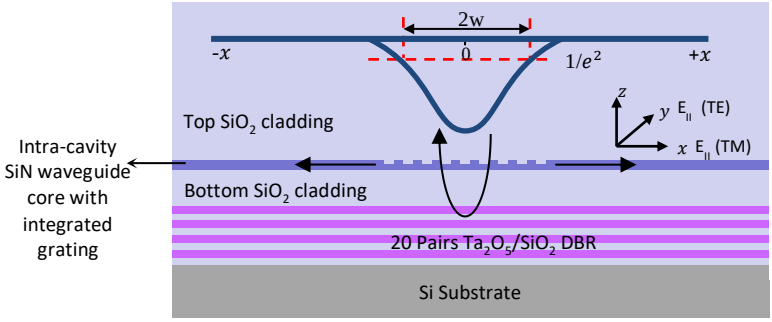

Fig. 3.7 Schematic cross-section of the 2-D FDTD simulation setup for the intra-cavity grating/dielectric DBR combination.

At first, the grating period, grating groove depth, and $T_{SiO2,Bottom}$ were simultaneously optimized using a particle swarm optimization algorithm [2]. The SiN waveguide core thickness was kept fixed at 300 nm, and a grating duty cycle of 50% was chosen to offer a simpler fabrication. A Gaussian beam with wavelength span of 10 nm, from λ_1 = 850 nm to λ_2 = 860 nm, and $1/e^2$ power diameter (2w) of 4.7 μm was used for the simulation. The lateral extent of the grating, i.e., the size of the grating region, was fixed to 10 grating periods, in order to match the diameter of the fundamental mode in the VCSIL. For the incident Gaussian beam, an average power reflection coefficient (R_{avg}) from grating/bottom dielectric DBR combination and power coupling coefficient (single-sided) into the SiN waveguide (T_{avg}) was defined by Equation (3.1). In the optimization algorithm, we assume that a minimum reflection coefficient, R_{min} of 0.995 was necessary to achieve a low threshold gain for the laser. When the conditions $R_{avg,TE\text{-}mode} > R_{min}$ and ($R_{avg,TE\text{-}mode}$ - $R_{avg,TM\text{-}mode}$) > 0 were fulfilled, $T_{avg,TE\text{-}mode}$ was calculated, and the single-sided coupling efficiency defined by the ratio $T_{avg,TE\text{-}mode}/(1 - R_{avg,TE\text{-}mode})$ was used as a figure of merit function for the optimization algorithm.

$$R_{avg} = \frac{\int_{\lambda_2}^{\lambda_1} R(\lambda)d\lambda}{\int_{\lambda_2}^{\lambda_1} d\lambda} \text{ and } T_{avg} = \frac{\int_{\lambda_2}^{\lambda_1} T(\lambda)d\lambda}{\int_{\lambda_2}^{\lambda_1} d\lambda} \quad (3.1)$$

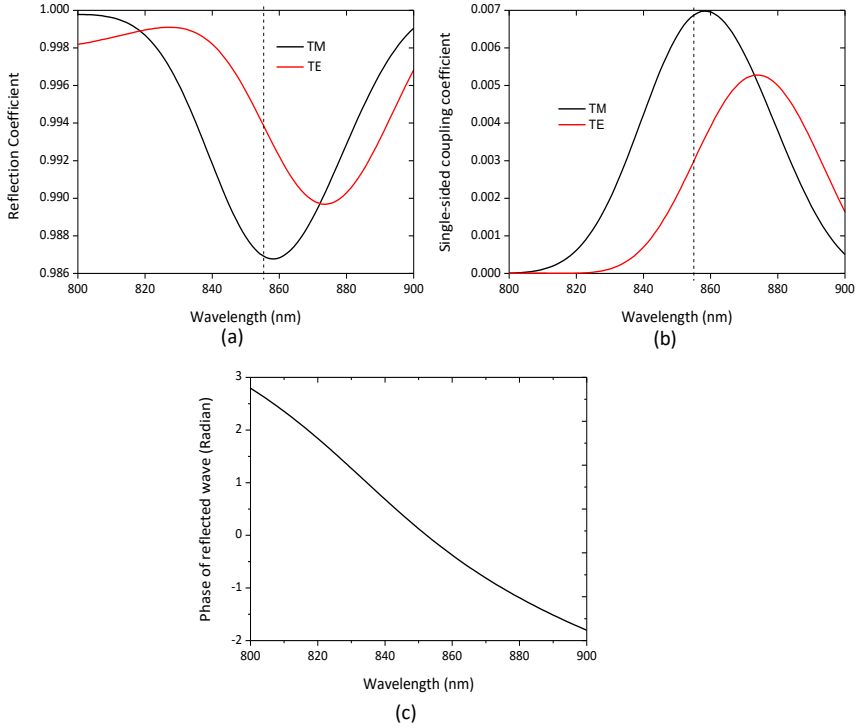

Fig. 3.8 (a) Reflection coefficient as a function of wavelength for TE and TM polarization. (b) Single-sided coupling coefficient as a function of wavelength for TE and TM polarization. (c) Phase of the reflected wave for TE polarization. Parameters of the simulations are 2w = 4.7 μm, grating period = 530 nm, SiN waveguide core thickness = 300 nm, $T_{SiO2,Bottom}$ thickness = 610 nm, grating groove depth = 30 nm, and grating duty cycle = 50%.

Simulation results for the optimized intra-cavity grating design are plotted in Fig. 3.8, where the grating period is 530 nm, the grating groove depth is 30 nm, and $T_{SiO2,Bottom}$ is 610 nm. Fig. 3.8 (a) shows the reflection coefficient spectrum. Fig. 3.8 (b) shows the single-sided coupling coefficient spectrum, for both the TE and TM polarized Gaussian beam and Fig. 3.8 (c) shows the phase of the reflected wave. As can be seen from Fig. 3.8 (b), at the VCSIL design wavelength of 855 nm, the grating operates away from the grating Bragg wavelength, and in particular for the TE-mode, the wavelength of the operation resides in the tail of the coupling coefficient spectrum. For the TE-mode, this provides coupling into the SiN waveguide, while maintaining a high reflection coefficient ($>R_{min}$) for lasing. For the TM-mode, the grating operates closer to the Bragg wavelength,

resulting in a higher coupling coefficient but the reflection coefficient is much lower than what is typically needed for lasing. Thus, the intra-cavity grating provides both the functionality of in-plane output coupling and pinning the polarization state of the light generated by the VCSIL at 855 nm wavelength. Next, we assess the fabrication tolerance on the intra-cavity waveguide with an integrated grating.

3.4.2.1 Effect of change in grating parameters on reflection and single-sided coupling coefficient spectrum

In 1st order approximation, a relative change in grating period results in an equal relative change of peak wavelength. As an effect, a 10 nm increase in grating period is found to result in a 15 nm red-shift of the reflection/coupling coefficient spectrum. But the grating period can be controlled down to 1 nm using advanced patterning techniques, so this should not be an issue. Moreover, the change in peak wavelength due to a change in grating duty cycle and SiN waveguide core thickness is the result of the change in the average effective index of the grating. A 20% change in grating duty cycle gives a minor 8 nm red-shift of the reflection/coupling coefficient spectrum, and a 10 nm increase in SiN waveguide core thickness results in a 3 nm red-shift in the reflection/coupling coefficient spectrum.

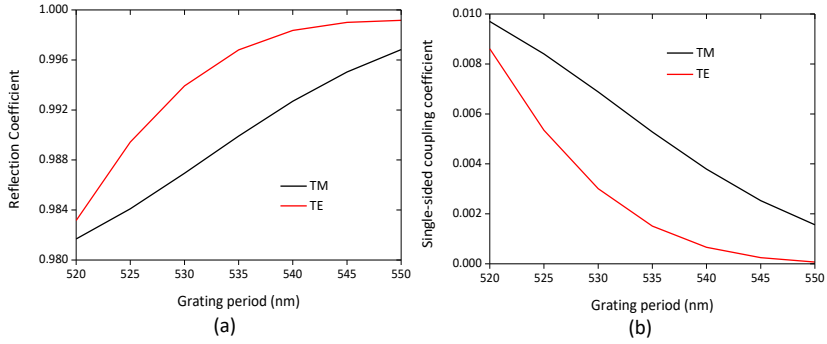

Fig. 3.9 (a) Reflection and (b) single-sided coupling coefficient as a function of intra-cavity grating period for TE and TM polarizations at a resonance wavelength of 855 nm. Parameters of the simulations are 2w = 4.7 µm, SiN waveguide core thickness = 300 nm, $T_{SiO2,Bottom}$ thickness = 610 nm, grating groove depth = 30 nm, and grating duty cycle = 50%.

Figure 3.9 shows the simulated reflection and single-sided coupling coefficient as a function of the grating period at a resonance wavelength of 855

nm for the two polarizations. As can be seen from Figure 3.9 (a) the intra-cavity grating is capable of pinning the polarization of the generated output to TE mode for a grating period ranging from 520 - 550 nm, while also providing coupling into the SiN waveguide, see Figure 3.9 (b).

3.4.2.2 Effect of bottom SiO_2 cladding thickness and VCSEL aperture size on reflection and single-sided coupling coefficient

A more critical parameter in the design is the bottom SiO_2 cladding thickness ($T_{SiO2,Bottom}$), as will be discussed below. The reflection/coupling coefficient spectrum is also affected by the width of the incident Gaussian beam. The next step is, therefore, to optimize the diameter of the oxide aperture in the VCSIL, which will approximately correspond to the $1/e^2$ power diameter of the incident Gaussian beam. The reflection/coupling coefficient spectrum for two VCSILs with oxide aperture diameters of 4 and 6 μm were compared as a function of $T_{SiO2,Bottom}$. The diameter of the fundamental transverse mode in these two VCSILs was estimated using an effective index analysis [3]. It was found that the 4 μm and 6 μm oxide aperture VCSILs correspond to a Gaussian beam with 4 and 5.4 μm $1/e^2$ power diameter respectively. Fig. 3.10 (a), (c) and (e) show simulation results for a Gaussian beam with a 4 μm $1/e^2$ power diameter (grating period = 539 nm, grating region width = 8 grating lines), and 3.10 (b), (d) and (f) show corresponding results for a Gaussian beam with a 5.4 μm $1/e^2$ power diameter (grating period = 525 nm, grating region width = 11 grating lines). Note that the double-sided coupling efficiency (=2*single-sided coupling efficiency) is plotted in Fig. 3.10 (e) and (f). As can be seen in Fig. 3.10 (a), (b), (c), and (d) the grating/bottom dielectric DBR combination reflects stronger for TE polarization than for TM polarization at 855 nm wavelength when $T_{SiO2,Bottom}$ is in the range between 580 and 660 nm, providing TE polarization selectivity in the VCSIL. By comparing Fig. 3.10 (a) and (b), we can conclude that a Gaussian beam with 4 μm $1/e^2$ power diameter has a somewhat lower reflection coefficient than with 6 μm diameter. Since a smaller oxide aperture diameter implies a wider angular spread of the optical field inside the VCSIL, it results in a penalty in the coupling efficiency for smaller oxide apertures, comparing Fig. 3.10 (e) and (f). Therefore, a VCSIL with large oxide aperture is preferred for optimal grating performance.

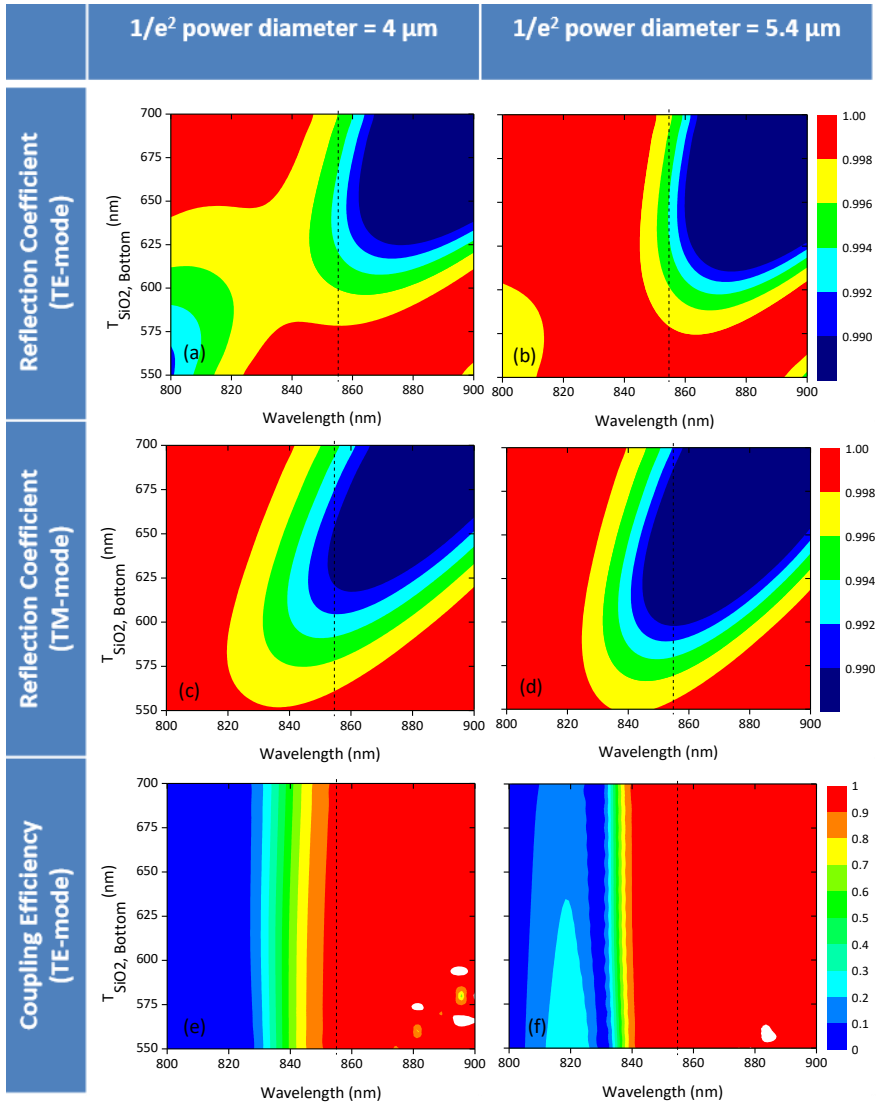

Fig 3.10 Reflection coefficient as a function of $T_{SiO2,Bottom}$ for (a) TE polarization, 2w = 4 µm and grating period = 542 nm (b) TE polarization for 2w = 5.4 µm and period = 530 nm (c) TM polarization, 2w = 4 μm and period = 542 nm. (d) TM polarization, 2w = 5.4 µm and period = 530 nm. (e) Double-sided coupling efficiency as a function of $T_{SiO2,Bottom}$ for TE polarization, 2w = 4 µm and period = 542 nm. (f) Double-sided coupling efficiency as a function of $T_{SiO2,Bottom}$ for TE polarization for 2w = 5.4 µm and period = 530 nm. Other parameters are fixed such as SiN waveguide core thickness = 300 nm, grating groove depth = 30 nm, and grating duty cycle = 50%.

3.4.2.3 Effect of misalignment on reflection and single-sided coupling coefficient

Finally, the dependence of the reflection coefficient and coupling efficiency on the possible lateral misalignment between the Gaussian beam (i.e., oxide aperture) and the grating region, in the direction perpendicular to the grating lines (x-axis in Fig. 3.7) is plotted in Fig. 3.11. At 855 nm wavelength, a misalignment of 1 μm leads to a 0.02% drop in reflection coefficient, and a misalignment of +1 μm gives a 6% drop in coupling efficiency for the right-hand-side waveguide.

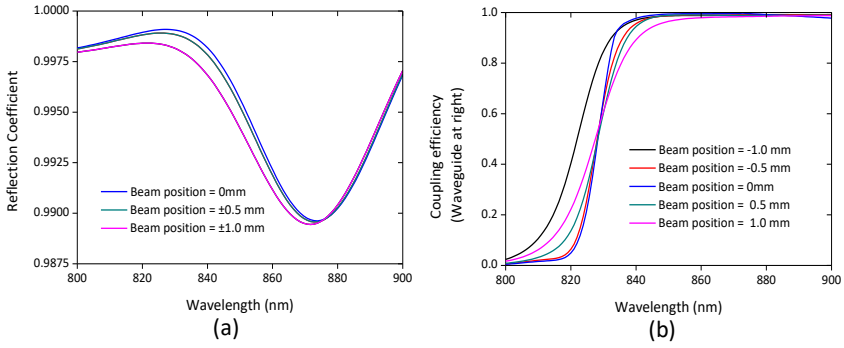

Fig. 3.11 (a) Reflection coefficient and (b) right-hand-side waveguide coupling efficiency, as a function of alignment between the Gaussian beam center relative to the grating region center, in the direction perpendicular to the grating lines. The grating region center is considered as the beam position = 0. Parameters of the simulations are 2w = 4.7 μm, grating period = 530 nm, SiN waveguide core thickness = 300 nm, grating groove depth = 30 nm, and grating duty cycle = 50%.

3.4.3 Vertical-Cavity Si-Integrated Laser design

In spite of all advantages of the transfer matrix formalism, this method remains limited to one-dimensional problems and plane waves and cannot give a deeper understanding of the optical processes inside of a complex three-dimensional structure, where some dimensions become comparable to the wavelength of the emitting light. Therefore to analyse the resonant optical field properties of the VCSIL cavity using a 1D wave transfer matrix method (TMM), the grating and bottom dielectric DBR combination is replaced by an artificial interface (blue dotted line in Fig. 3.12) having the spectral reflection coefficient, single-sided coupling coefficient and phase of the reflected wave obtained from the 2D FDTD simulations in Fig 3.8. From this 1D TMM model, the resonance wavelength and

optical field distribution along the optical z-axis above the grating are extracted, an example of which is shown in Fig. 3.12.

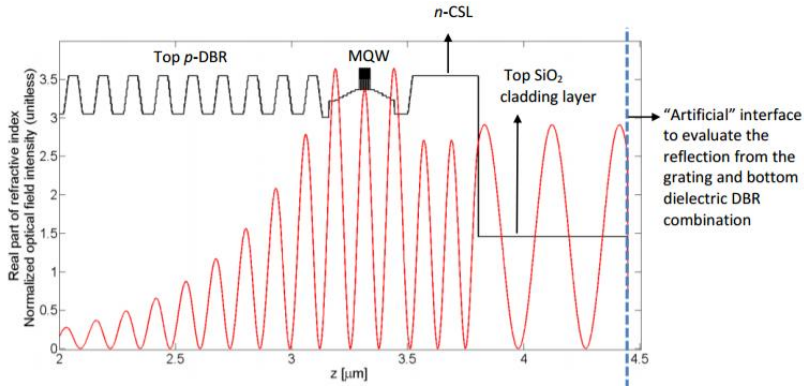

Fig. 3.12 Refractive index distribution (black line) and simulated resonant optical field intensity (red line) along the *z*-axis of a 855-nm-wavelength VCSIL.

The simulations also provide information on threshold gain and power incident on the artificial interface. From the latter, we can estimate the slope efficiency for the light coupled to the SiN waveguide, via the coupling coefficient obtained from the 2D FDTD simulations in Fig. 3.8. As found in Fig 3.6 (a), the thickness of the top SiO_2 cladding layer ($T_{SiO2,Top}$) needs to be around 600 nm or larger to minimize the SiN waveguide leakage loss. Also, since it is an intra-cavity layer, the thickness sets the VCSIL resonance wavelength. A $T_{SiO2,Top}$ thickness of 766 nm gives a resonance wavelength of 855 for a 5 μm oxide aperture diameter VCSIL. As observed in [5] a variation of 5 nm in the $T_{SiO2,Top}$ thickness shifts the resonance wavelength by approximately 0.65 nm, indicating a good fabrication tolerance. Since DVS-BCB has a refractive index similar to SiO_2, any change in the thickness of the DVS-BCB layer translates into a similar shift in resonance wavelength as for the SiO_2 layer. The threshold gain and single-sided slope efficiency at the resonance wavelength of 855 nm for a 5 μm oxide aperture diameter VCSIL are 821 cm^{-1} and 0.3 mW/mA respectively. When computing the slope efficiency, an internal quantum efficiency of 85% was assumed.

The calculated threshold gain and single-sided slope efficiency as a function of the grating period at a resonance wavelength of 855 nm are shown in Figure 3.13. While the VCSILs with the smallest grating period provide high single-sided slope efficiency, the threshold gain required for lasing is large. This shows that the selection of an optimal intra-cavity grating period sets a trade-off between the threshold gain and single-sided slope efficiency.

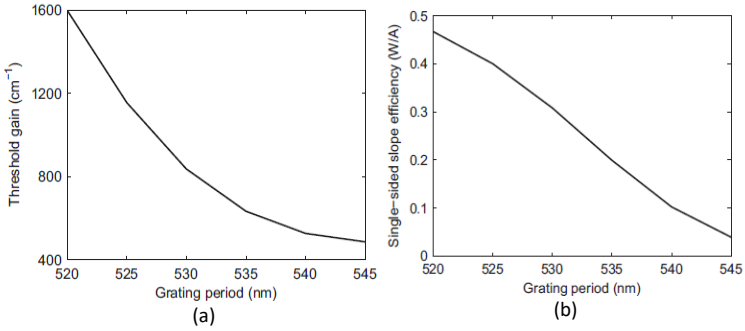

Fig. 3.13 (a) Simulated threshold gain and (b) single-sided slope efficiency as a function of the intra-cavity grating period at a resonance wavelength of 855 nm (TE polarization).

3.4.4 Grating coupler design

To be able to couple light in the SiN waveguide to an optical fiber, a grating coupler was designed (shown in Fig. 3.5(b)). In contrast to the intra-cavity grating, the grating coupler operates at the Bragg wavelength and has an etch depth of 300 nm, grating period of 683 nm and DC of 50%. The grating teeth are tilted by 20° to avoid the back reflection into the VCSEL.

A 3D simulation is performed to estimate the coupling efficiency and the angle of diffraction of the grating to couple the diffracted light in and out of the optical fiber. Fig 3.14 (a) shows the schematic cross-section view of the simulation setup in xz-plane whereas Fig 3.14 (b) shows the refractive index profile of the SiN grating with the waveguide in xy-plane. A waveguide mode with TE polarization is launched into the SiN waveguide. This mode is then diffracted by the grating coupler. A frequency monitor is placed above the grating to project the far-field distribution of the diffracted beam. A far-field projection of the beam diffracted by the grating coupler at 855 nm wavelength is plotted in Fig 3.14 (c). As can be seen from Fig. 3.14 (c), the diffracted beam is propagating at 40 degrees to the z-axis with a horizontal angle of 315 degrees. The theoretical coupling efficiency provided by such a grating coupler is -4.2 dB at 855 nm. The tilt of the grating teeth can be further optimized to get better coupling efficiency.

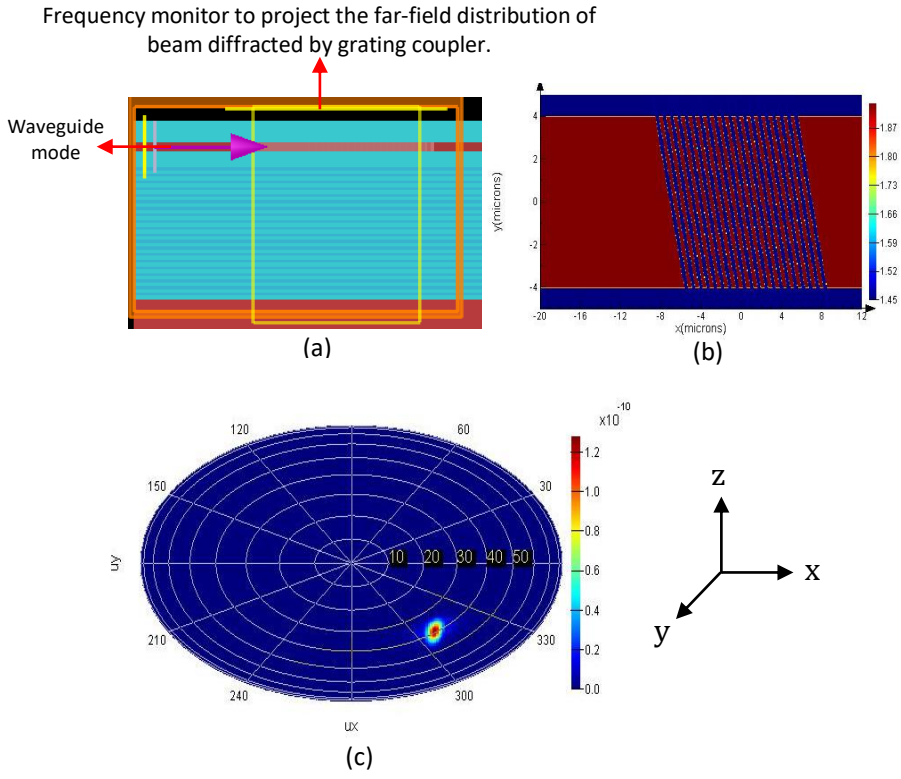

Fig. 3.14 (a) Cross-section view (xz-plane) of simulation setup (b) Index profile of SiN grating with waveguide (xy-plane) (grating teeth are tilted at an angle of 20 degree) (c) Far field projection of the beam diffracted by the grating coupler

3.5 Conclusion

In summary, the design of a hybrid cavity Gen1 VCSEL is presented where a GaAs half VCSEL is attached to a dielectric DBR on Si using DVS-BCB bonding. This design will benefit in the development of the heterogeneous integration technology. Further, a numerical investigation of a Gen2 VCSIL with an intra-cavity grating placed inside the cavity is presented. We show that a weak diffraction grating placed inside an oxide-confined 855 nm wavelength VCSIL cavity is able to provide a high in-plane coupling efficiency to a connected SiN waveguide while maintaining a low lasing threshold gain. The proposed design of an intra-cavity grating/dielectric DBR combination has following advantages:

- It allows the heterogeneous integration of GaAs-based vertical cavity light sources on a SiN waveguide circuit.
- It selects the polarization state of the light generated by the VCSIL.
- It can provide good transverse mode control.
- High-efficiency waveguide coupling can be obtained.
- As demonstrated in [4], the alignment is determined by lithography after the heterogeneous integration of the III-V material.

For a Gen2 VCSIL with smaller oxide aperture diameters, the grating coupling coefficient is reduced by the wider angular spread of the optical field inside the VCSIL. Therefore, an oxide aperture diameter >4 μm is required to give optimal performance. We also showed that the selection of the grating period sets a tradeoff between the threshold gain and single-sided slope efficiency. Such a VCSIL design with integrated SiN waveguide can offer a low cost, energy efficient, scalable solution for SiN photonic integrated circuits.

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4

Fabrication and characterization of photonic integrated circuits on SiN

4.1 Introduction

In the previous chapter, we discussed the design of a hybrid-cavity GaAs VCSEL integrated onto a SiN waveguide platform. We presented two different variants of the hybrid VCSEL referred to as Gen1 vertical cavity surface emitting laser (VCSEL) and Gen2 vertical cavity Si-integrated laser (VCSIL) devices, where the standing wave optical field extended over the III-V material and Si-integrated part. As shown in Fig4.1 (a), Gen 1 VCSELs were equivalent to a typical III-V VCSEL with the difference that the bottom III-V DBR is replaced by a 20 pair Ta_2O_5/SiO_2 DBR on Si. These devices were still surface emitting and thus acted as a stepping-stone in the development of the integration technique for the more complex Gen2 VCSILs. We purchased a customized DBR wafer with 20 pairs of Ta_2O_5/SiO_2 DBR layers deposited on Si from JDS Uniphase Corporation. As discussed previously, the GaAs half-VCSEL can be attached to these dielectric DBR wafers using a divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding to form the hybrid-cavity Gen1 VCSEL. Thus no post-processing on the Si wafer is required and the important process to be developed in this case is the heterogeneous integration technology, which will be briefly explained in the next chapter. Fig 4.1(b) represents the Gen2 VCSIL device which is an advanced

version of Gen1 VCSELs, where an intra-cavity SiN waveguide with a shallow etched grating is placed inside the cavity, to tap off the vertically amplified light into the SiN waveguide. In order to make use of the same dielectric DBRs for the Gen2 VCSIL, several new fabrication steps needed to be developed.

In this chapter, a complete description of the fabrication process required to define an intra-cavity waveguide and grating on top of the dielectric DBR is provided. All the fabrication steps required were carried out using conventional fabrication tools available in our clean room, including deposition, patterning, and etching. Since the performance of a photonic device is very sensitive to geometry, especially when the feature size of the structure is reduced to a few hundred nanometers, fabrication with very high accuracy and reproducibility is desired to minimize the discrepancy between designed and fabricated devices. Therefore, all the processes were optimized for optimal device performance.

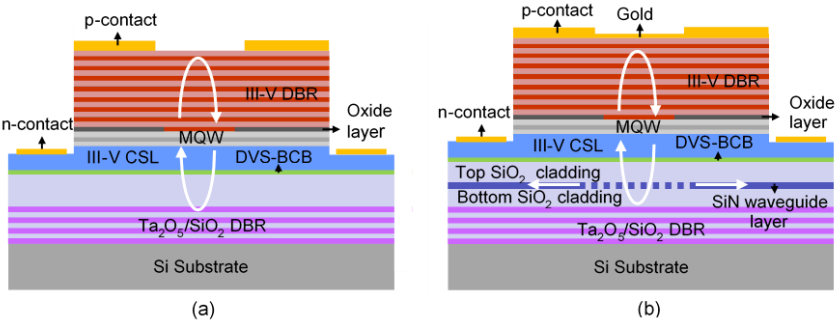

Fig. 4.1 Schematic cross-section of (a) Gen1 VCSEL and (b) Gen2 VCSIL device.

Finally, the vertical measurement technique for optical characterization of the defined waveguides and grating couplers is also explained.

4.2 Deposition

The first step towards the fabrication of the SiN intra-cavity waveguide and grating on the dielectric DBR is the deposition of a 610 nm thick bottom SiO_2 cladding layer and a 300 nm thick SiN waveguide layer (see Fig 4.1 (b)), using plasma enhanced chemical vapor deposition (PECVD). The PECVD deposition tool available in our cleanroom is “Advanced Vacuum Vision 310” equipped with different RF frequency sources which can operate at high frequency (H-f) mode of 13.56 MHz, low frequency (L-f) mode of 100−460 kHz and a mixed (high and low) frequency (M-f) mode. The temperature of the chamber plate can be varied

from 120−270 °C. The same deposition tool can be used to deposit both SiN and SiO_2 thin films. The deposition of standard PECVD SiO_2 is a well-optimized process with the refractive index close to 1.45 and negligible absorption in the VIS-NIR wavelength range, whereas the quality of the SiN film, its refractive index, and its absorption depends heavily on the chamber condition during deposition. A thin film of SiN can be deposited using a mixture of precursor gasses like SiH_4, NH_3, and N_2 with optimal ratio, at certain RF power and chamber pressure. A low loss PECVD SiN waveguide layer operating in the NIR wavelength range is highly desirable in this thesis. Various investigations have been carried out concerning the loss of thin SiN layers, as briefly explained in chapter 2 pp. 26 of Weiqiang Xie's PhD thesis [1]. SiN thin films deposited with two different frequency modes (L-f, and H-F) and two different temperatures of 120 and 270 °C were characterized using ellipsometry. The deposition rate of the SiN thin film was found to be 10-15 nm/min depending on the operating condition of the chamber. Fig 4.2 shows the real and imaginary part of the refractive index of SiN films for 4 different combinations of frequency and temperature. As can be seen from Fig 4.2(a) the real part of the refractive index is dependent on the temperature of the chamber. For instance, the SiN thin film deposited at high temperatures results in a higher index than the low-temperature-deposited SiN, thus indicating a reduction in the material density due to higher hydrogen content. From Fig 4.2(b) it can be seen that the RF frequency has a dramatic effect on the extinction coefficient with values for L-f SiN over two orders of magnitude lower than for H-f SiN, implying higher optical loss in H-f SiN films. The waveguides losses for all these SiN films were also examined to find the best material for photonic integrated circuits, detailed in chapter 2 pp. 48-50 of Weiqiang Xie's PhD thesis [1]. The waveguides with the same width were fabricated on different SiN films using the same process recipe (resist, patterning and etching). For a 2.0 μm-wide waveguide where the absorption loss is dominant over the scattering loss, it was found that H-f-SiN gives ~5.7 dB/cm higher loss at a wavelength of 900 nm compared to L-f SiN. A waveguide loss of 0.94 dB/cm and 1.88 dB/cm was achieved for 2.0 μm wide waveguides with 200 nm thickness, for L-f SiN waveguide deposited at 270°C and 120°C respectively at a wavelength of 900 nm (see chapter 2 pp. 54 of Weiqiang Xie's PhD thesis) [1]. Therefore, a L-f SiN deposited at 270°C is of particular interest in this thesis due to low material loss.

A 610 nm thick standard PECVD SiO_2 layer and 300 nm thick low-frequency (L-f) PECVD SiN layer was deposited at 270°C on a quarter of a 200 mm dielectric DBR wafer. The thickness of the deposited SiO_2 and SiN films were accurately monitored using ellipsometry. The next step is to pattern the intra-cavity grating, interconnecting waveguide and grating coupler on the deposited SiN waveguide layer using lithography.

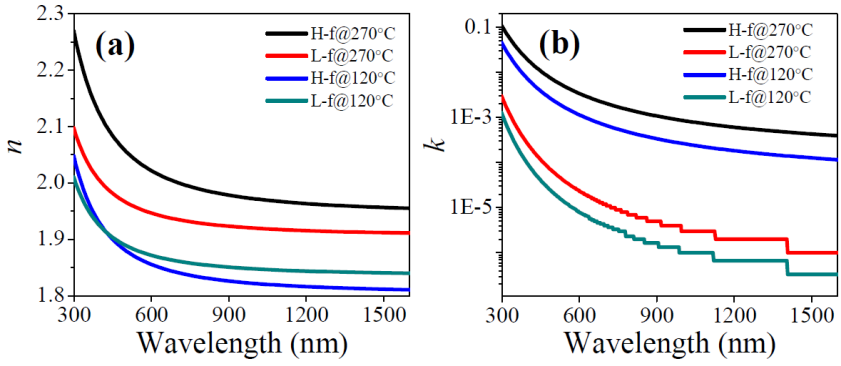

Fig. 4.2 Measured (a) refractive index n and (b) extinction coefficient k, of SiN films deposited under different conditions. Reproduced from [1]

4.3 Lithography

Lithography is a process of transferring information from design to a substrate. In order to do that, a form of radiation is delivered at specific locations on a material, which is designed to be sensitive to that radiation. Several techniques have been invented for patterning and among them, optical lithography is the most common technique utilized for mass fabrication in CMOS manufacturing. Deep-UV lithography is a well-established technique where a pre-defined mask is used in combination with 193 nm or 248 nm exposure wavelengths. [2] The advantages of such a technique are: large field size (many devices can be patterned on the mask at the same time), high throughput and the capability of handling complexity very well compared to other methods [2]. On the downside, optical lithography is diffraction limited by the exposure wavelength (λ_{exp}) and optics (i.e., the numerical aperture NA of the projection lens). The resolution is roughly proportional to λ_{exp}/NA.

In general, standard SiN chips are fabricated on 200 mm diameter Si wafers with a thickness of 700 µm, using a deep-UV lithography process. These wafers comprise a stack of 300 nm/220 nm/150 nm thick SiN on ~2-4 µm thick SiO_2, deposited by PECVD/LPCVD on top of the Si wafer. The PICs are defined with 193 nm optical lithography and etched by a fluorine-based inductively coupled plasma (ICP) reactive ion etch process to get the final structure. However, as discussed earlier, a customized dielectric DBR on Si, purchased from a commercial supplier is used in this thesis, which is quite different from a standard Si wafer. These dielectric DBR wafers were not acceptable for the front end of line of the CMOS fab due to potential contamination. Therefore, we cannot use the standard 193 nm optical lithography to define waveguide circuits on these

wafers. Instead, an e-beam lithography is used in this thesis to define the SiN waveguide structures on the deposited PECVD SiN waveguide layer.

4.3.1 E-beam lithography

Electron-beam lithography (EBL) is another common modality of lithography. It allows the direct writing of structures by exposing a sample coated with a thin layer of e-beam sensitive resist (in analogy with photoresist we use the word e-beam resist), with a focused electron beam such that the resist under exposure gets chemically modified. After the exposure, the sample is immersed in a developing solution where the exposed (non-exposed) areas will dissolve in case of positive (negative) e-beam resist. This process is called development (in analogy with the development of photographic films). Therefore, after a given amount of development time, the sample is dried leaving the designed pattern in the resist. There are two main EBL strategies: projection printing and direct writing. In projection printing, a large e-beam pattern is projected through a mask onto a resist-coated substrate. In direct writing, a small e-beam spot is moved with respect to the wafer to expose the wafer one pixel at a time. This eliminates the expensive and time-consuming production of masks [3-5], but also reveals the inherent drawback of direct writing, being the low throughput as a result of the serial way of writing structures. The patterning of intra-cavity grating, grating coupler, and waveguide described in chapter 3 relies on direct writing.

In our clean room, the electron beam lithography system available is a Raith-VOYAGER that can be used for the patterning and measurement of various samples, masks and wafers. The important system features include operation with acceleration voltages up to 50 KV, maximum write field size of 500 µm and automatic system setup (autofocus/autostigmator/automatic stage adjustment with mark recognition/automatic write-field alignment). The system can be used to pattern complex structures on masks of up to 7-inch diameter and wafers of up to 8-inch diameter, using direct-write procedures with ultra-high resolution in the nanometer range [6]. The resolution in electron beam lithography depends on the type of the resist used, the thickness of the resist, the type of substrate, the acceleration voltage (1 - 50 kV), and the operating conditions. Just like other lithographic processes, electron-beam lithography also has an optimum dose, which represents the dose at which the measured linewidth after development is equal to the designed linewidth, defined as an electron dose. An electron dose (usually expressed in $\mu C/cm^2$) is the charge per unit area required to achieve the desired chemical response in the resist. The required electron dose for exposure of structures mainly depends on the resist being used, its thickness, the developer, and the desired minimum structure size. Another important key factor in the patterning is the dwell time. The dwell time determines the writing time of the

beam at each defined position on the sample and relates with the electron dose as follows:

$$Electron\ Dose = \frac{Beam\ current \times Area\ dwell\ time}{Step\ size \times Line\ spacing} \quad (4.1)$$

The beam current can be measured directly from the instrument via the Beam Current module. The geometric parameters that affect the patterning of a structure are the step size, which is the distance between dots, and the line spacing, which is the distance between each line of dots. The minimum step size, also known as the pixel width, is hardware dependent and is proportional to the (18 bit) digital to analog converter (DAC) step resolution. The smallest step size can be calculated as:

$$Minimum\ step\ size = \frac{Writefield\ size}{2^{18}} \quad (4.2)$$

So, for example, for a 100 μm write field, the smallest step, or pixel width is 0.4 nm. Several complex processes that affect the reliability of the e-beam process are the delocalization of electrons due to forward and backscattering (proximity effects), collapse of the pattern due to swelling and capillary forces, fluctuations in the sizes of features (line edge roughness) and the field stitching. The explanation of each process involved in e-beam is out of the scope of this thesis. A brief explanation of these processes can be found in [3-5]. One of the problems that is of interest to us is field stitching, which is one of the limitations when writing a structure of several cm long. This problem is overcome in the voyager EBL system with a new continuous patterning mode compared to conventional EBL systems.

4.3.1.1 Conventional e-beam writing

In conventional e-beam writing mode, the stage is fixed and the beam is moving. The size of the write field is defined by the maximum deflection range of the electron beam. In the Voyager system, the size of the maximum write field is 500 μm. Any structure longer than the size of the writing field is fractured into shorter structures that fit into a single write field. Each boundary between write fields is therefore subject to some amount of stitching error. The operation principle of the conventional stitching technique is illustrated in Fig 4.3 (a) [7].

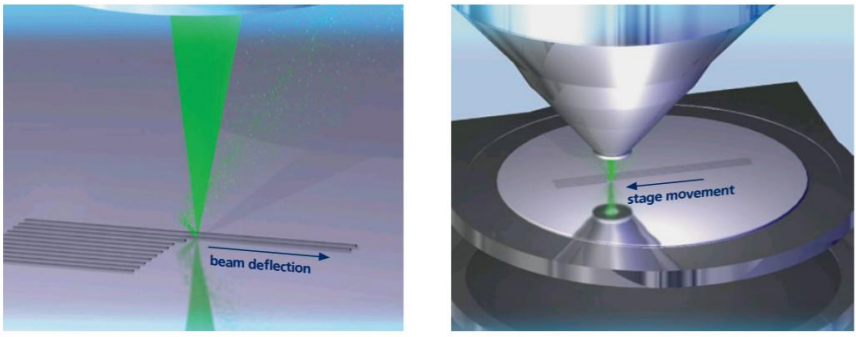

Fig. 4.3 (a) Illustration of conventional e-beam writing mode. The beam is deflected while the stage is stationary, resulting in a stitching error of several nm. (b) FBMS mode. The beam is fixed while the stage is moving. Reproduced from [7]

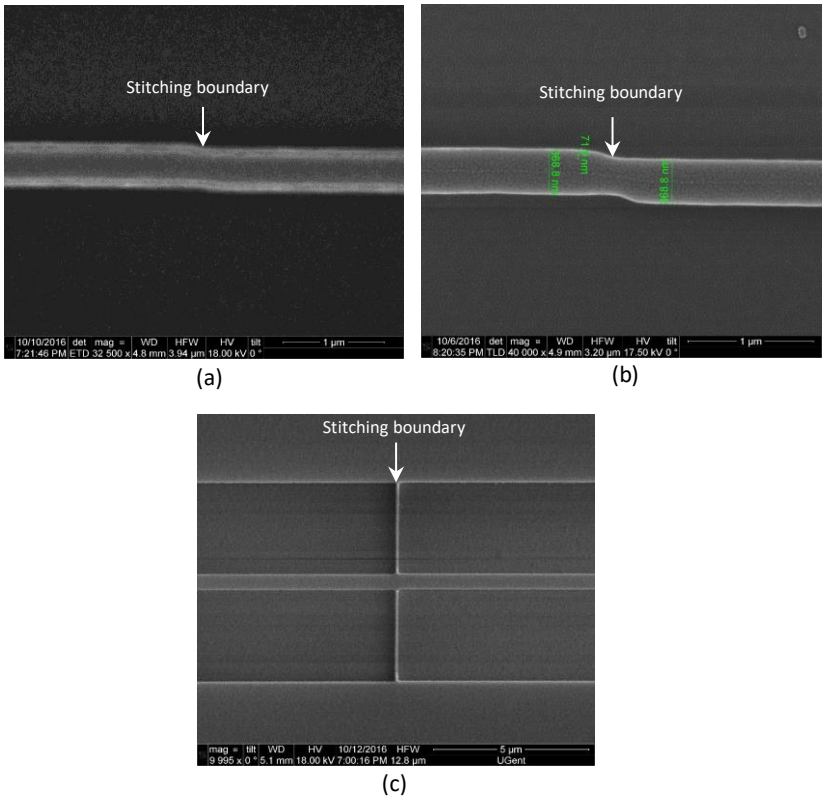

Fig. 4.4 SEM image of stitching boundary in three different samples.

When writing long waveguides (with lengths of the order of several cm), this can result in kinks in the waveguide. To check the occurrence of stitching errors while writing structures longer than the e-beam writing field, long SiN waveguides were written in conventional e-beam writing mode. The typical stitching errors are shown in Fig 4.4. As can be seen from fig 4.4, the stitching errors for 3 different samples written by e-beam with the same process are very different from each other. With the conventional e-beam writing mode, it was found that the stitching errors are not reproducible, varying from 30 nm - 70 nm and sometimes even result in a discontinuity in the waveguide. These stitching errors can influence the device performance significantly; e.g., significant increase in optical waveguide losses in elongated optical waveguides. Hence, it is important to limit the amount of stitching borders in order to avoid unwanted device deterioration as a result of stitching errors. Raith meets this challenge with a new continuous patterning mode. This "zero-stitching error" approach called "Fixed Beam Moving Stage" (FBMS) guarantees the fabrication of up to several cm long, thin, and smooth paths of arbitrary curvature, including tapered paths [7]. The FBMS writing mode is briefly explained in the next section.

4.3.1.2 FBMS writing

The FBMS technology allows exposing smooth and stitching-error free paths of arbitrary curvature of any length, even up to several cm long, by maintaining the beam at a fixed position and then continuously moving the stage (and thus the sample) with respect to the beam [6]. Fig 4.3 (b) illustrates the operating principle of the FBMS mode. Hence, FBMS is the ideal choice to fabricate optical devices like waveguides, where reproducibility of the fabrication process is very important. Two structures that can be written using FBMS writing mode are:

• **FBMS lines** - FBMS lines are paths with a width of zero. In "line mode", the beam is kept at a fixed position while the sample is moving laterally with constant speed. Like for single pixel lines, there is a strong correlation between beam current, speed, and the resulting line widths. The resulting dose is calculated by the following formula:

$$Line\ dose = \frac{beam\ current}{stage\ speed} \tag{4.3}$$

FBMS lines with less than 20 nm line width can be written in line mode.

• **FBMS areas** – FBMS areas are paths with a width larger than zero. In "area mode", an increase in linewidth up to several tens of microns is achieved by a repetitive and continuous lateral deflection of the beam in a circle generator pattern (see Fig. 4.5), which is defined such that the applied dose is constant over the designed line width. Moreover, its circular symmetry guarantees the same line

width regardless of the direction of the sample motion. In addition to the beam deflection, the sample is simultaneously moving along the designed path as in line mode. The area dose can be calculated by the following formula:

$$Area\ dose = \frac{beam\ current}{stage\ speed \times line\ width} \tag{4.4}$$

The speed of the stage for FBMS writing depends on the width and the step size, which is a user-defined value. The stage speed is automatically adjusted whenever another dose factor than 1.0 is applied, and when the width of the FBMS area element differs from the calculation width chosen in the patterning parameter calculator window. Thus the real stage speed during the patterning can differ from the specified stage speed.

The user should always enter a calculation width value as close as possible to the thinnest expected line in the GDSII pattern, in order to estimate accurately how fast the stage must move when writing the thinnest lines in the structure. The calculation width is simply a reference value, which relates width, stage speed, and dose. Stage speed will be automatically adjusted by the software depending on the patterning being carried out. There are three different kinds of beam deflection patterns related to the FBMS:

- Spot pattern for FBMS lines,
- Circle generator pattern for FBMS areas, and
- User-defined beam deflection

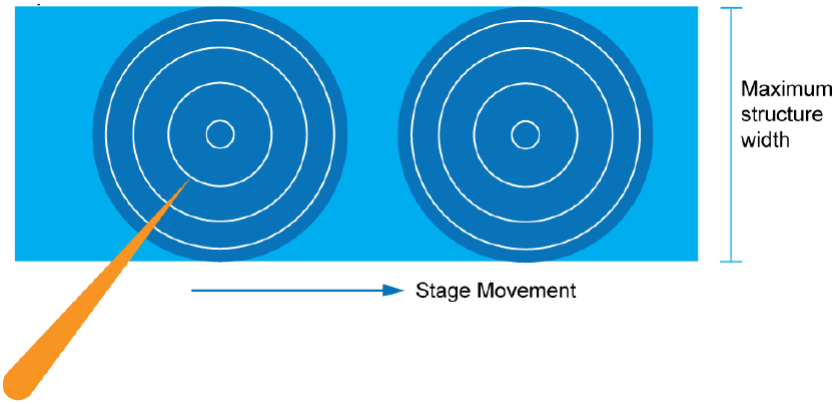

Fig. 4.5 Circle generator pattern for FBMS area.

In the spot pattern, the beam is simply kept at a fixed position in the center. The circle generator pattern is applied for FBMS area elements in order to achieve

uniform area dosing for any possible direction of stage movement for the given width of the element. A single filled circle cannot be used for this purpose since this would lead to a higher dose towards the center of the path. On the other hand, a single circle circumference is also not suitable, since this would lead to a higher dose towards the boundary. For this reason, a special circle symmetric pattern is calculated by the software, where the distance between inner circles is greater than the distance between outer circles. The pattern results in an average step size perpendicular to the stage movement, which can be defined in the enhanced parameters for FBMS. Using the FBMS mode in combination with the conventional stitching lithography enables the researcher with a whole new dimension in nano-device fabrication [4].

4.3.2 Patterning intra-cavity grating and waveguide on SiN

4.3.2.1 Process flow

As discussed in chapter 3, the intra-cavity grating has an etch depth of 30 nm whereas the interconnecting waveguides and grating couplers are etched 300 nm deep. Therefore, two different e-beam steps are required to achieve two different etch depths. Further, to pattern the second e-beam structure relative to first e-beam structure on SiN, gold alignment marks are required, which are written with an additional e-beam step. Thus, in total 3 e-beam steps are required to pattern the alignment marks, intra-cavity gratings, waveguides and grating couplers. The process of alignment in electron beam lithography is called overlay. There are different overlay techniques available in e-beam, either by manual detection of the alignment marks or by automatic recognition of alignment marks. The overlay accuracy is strongly dependent on the quality of the alignment marks and the mark detection techniques. With manual detection, an overlay accuracy of 100-200 nm can be achieved whereas by automatic recognition technique usually 10s of nm overlay accuracy is achievable. As discussed in chapter 3, the intra-cavity grating has good alignment tolerance (±1 µm) therefore, the overlay was done by manual detection of the alignment marks. Next, the selection of a positive or negative tone resist for writing these structures needs to be done. As can be seen from Fig 4.1 (b), a GaAs half VCSEL is attached to the processed dielectric DBR samples via adhesive DVS-BCB bonding. Hence, a uniform sample where the exposed areas are removed during development (positive tone resist) is of more interest, as the BCB can fill the etched gaps and the planarization of the surface is achieved, which helps in adhesive bonding. Depending on the type of resist used (in this case a positive resist), the GDSII mask with 3 different layers was designed using the mask design software IPKISS to perform 3 different EBL steps. Layer 1 consisted of the alignment marks for overlay and III-V post-processing. Layer 2

consisted of intra-cavity gratings with five different periods, varying from 525 - 545 nm, and three different DCs, varying from 45 - 55%. Layer 3 consisted of an interconnecting waveguide with width of 5.5 µm and trench of 3 µm and grating couplers at both ends of the waveguide with a period of 683 nm and 50% DC.

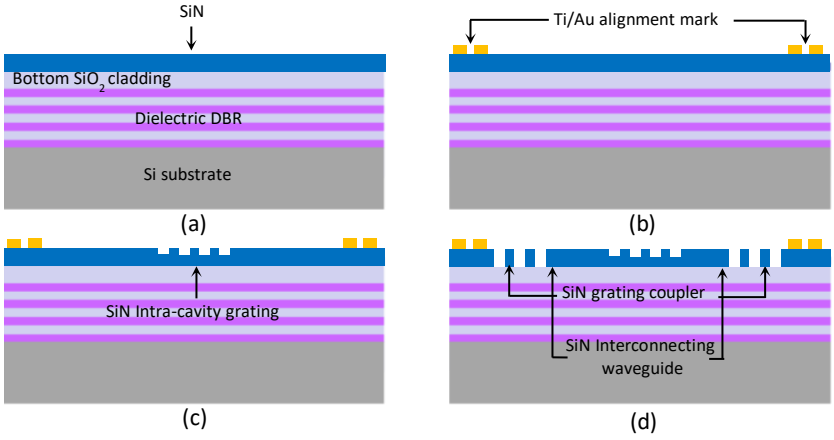

Fig. 4.6 Schematic for ebeam writing of SiN PIC: (a) SiN and SiO_2 cladding layer on dielectric DBR (b) Ti/Au alignment marks (c) SiN intra-cavity grating and (d) SiN grating coupler and interconnecting waveguides.

Fig. 4.6 shows the schematic for writing the SiN PIC structures using e-beam. Step1 is to define the Titanium/Gold (Ti/Au) (10nm/30nm) alignment marks with lift-off process, providing good contrast, which is written in conventional e-beam writing mode (Fig. 4.6 (b)). Step 2 is to define the intra-cavity grating with 30nm etch depth again written by conventional e-beam writing mode (Fig. 4.6 (c)) and finally step 3 is to define the interconnecting waveguide and the grating coupler with 300 nm etch depth written by the combination of conventional (grating couplers) and FBMS (interconnecting waveguide) e-beam writing mode (Fig. 4.6 (c)). Between each e-beam writing step the sample was cleaned thoroughly by removing e-beam resist in AR 600-71 in ultrasonic bath followed by 10 min O_2 plasma in a Tepla barrel etcher.

4.3.2.2 E-Beam resist AR-P 6200 (CSAR 62)

AR-P 6200 (CSAR 62) is a new positive tone electron beam resist designed by Allresist after intensive development work to have similar performance to ZEP520A (a popular positive tone e-beam resist) in resolution, speed, and etch resistance [8]. The acronym CSAR is deducted from the mechanism used: Chemical Semi Amplified Resist. There are a variety of developers offered by Allresist, i.e., AR 600-546, 600-548 and 600-549 with different pros and cons. A

comparison study between ZEP 520A in the corresponding developer ZED-N50 and CSAR 62 in developers AR 600-546 and 600- 549 showed that both CSAR and ZEP has excellent structural resolution and comparable broad process windows and CSAR 62 has even superior performance in terms of contrast and sensitivity when developed in AR 600-546. Thus CSAR-62 is an attractive cheaper alternative to ZEP. In conclusion, the CSAR 62 resist is characterized by the following features:

- high sensitivity which can be adjusted via the developer
- highest resolution (< 10 nm) and very high contrast
- highly process-stable, high plasma etching resistance
- easy fabrication of lift-off structures

Fig. 4.7 shows the thickness of the CSAR 62 resist at different spin speed. In this thesis the AR-P 6200.09 resist was spin coated on the SiN waveguide layer on the dielectric DBR at 2000 rpm. While writing the structures using e-beam on an insulating layer (SiN on dielectric DBR), there are no pathways for the electrons to dissipate and charge builds up and defocuses the electron beam. This can largely affect the pattern which will further degrade the device performance. Therefore, a water-soluble conductive polymer Electra 92 (AR-PC 5090) [9], which is compatible with CSAR 62 was also spin coated on top of the AR-P 6200.09 layer to reduce the effect of charging. It is also important to apply the conductive polymer on these samples to improve the contrast of the Ti/Au marks for overlay.

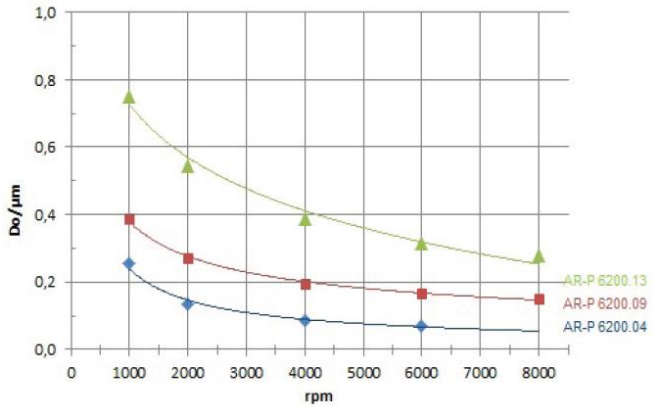

Fig. 4.7 CSAR 62 resist film thickness as a function of spin speed, Reproduced from [8]

Once the choice of e-beam resist is made, a preliminary test exposure, referred to as a dose test is performed on the sample. In this test, the pattern to be written is exposed at different electron doses and after development the optimum dose can be determined with a suitable inspection tool (such as a scanning electron microscope SEM, atomic force microscope AFM, optical microscope, etc.). The required electron dose for exposure of a structure depends on several factors such as the resist, its thickness, the developer, development time, and the desired structure size. After the dose test, it was found that an optimal electron dose of 140 $\mu C/cm^2$ is required to write the intra-cavity gratings and grating couplers using conventional EBL mode. As discussed above the long interconnecting SiN waveguides are written with FBMS mode. An optimal setting of the FBMS mode is also very important, which again can be determined by the dose test. An optimal electron dose and stage speed is required to write the structures with good sidewall roughness. An optimal electron dose of 100 $\mu C/cm^2$, a step size of 10 nm and stage speed of 0.138 mm/s was fixed to write the 3 um wide trenches of the waveguide.

4.4 Etching

After e-beam lithography and development, the pattern is transferred to the resist on top of the semiconductor substrate. To transfer this pattern into the dielectric layer, etching is used. There are two important aspects of etching. The first is the selectivity towards the mask. A good etch process will etch the material at a rapid rate as compared to the mask. The second is the directionality of the etch which is decided by the type of etching used. Etching can be accomplished in either a "wet" or a "dry" environment. Wet etching involves the use of liquid etchants to remove the material through chemical processes. A wet chemical etching can often provide good selectivity. However, wet etching is hard to control accurately and will not result in vertical sidewalls as anisotropic etching is difficult to achieve. The dry etching is done in a plasma reactor. Briefly, for a plasma etching process, a plasma generator creates etchant species (atoms, molecular radicals, and ions), and the material to be etched is removed by chemical reactions of those reactive radicals along with the generation of volatile by-products (chemical etching), and/or by direct physical sputtering due to ion bombardment on the material (physical etching). In general, physical etching is directional and shows less material dependence, while chemical etching is sensitive to material properties and usually nondirectional. All plasma conditions including RF power, pressure, and gas chemistry can affect the etching process and results. In this thesis, dry etching, more specifically reactive-ion etching (RIE), is used to etch the SiN layers. An Advanced Vacuum Vison 320 RIE tool equipped with 13.56 MHz RF excitation and a cooling system to maintain the sample plate temperature

at ~20 °C is used. An optimization of dry etching process parameters to etch SiN thin films is again briefly explained in chapter 2 of Weiqiang Xie's PhD thesis [1]. An optimal process with 210 W power, 20 mTorr pressure, and a gas mixture of CF_4, H_2, and SF_6 with ratio 80 sccm, 7 sccm, and 3 sccm respectively was used to provide vertical and smooth sidewalls. An etch rate of 90 nm/min for a L-f SiN layer was achieved with optimal etching parameters. Once etching is done the e-beam resist is stripped off in resist remover AR 600-71, and the sample is cleaned in an oxygen plasma for 10 min.

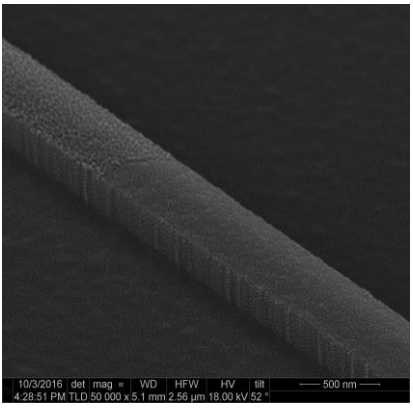

Fig. 4.8 Sidewall of the waveguide after dry etching and removal of the e-beam resist (A thin gold layer is deposited to reduce the charging during SEM imaging).

Fig 4.8 shows the SEM image of the sidewall of the SiN waveguide after dry etching. The sidewall roughness depends on the etching technique and irregularities introduced by e-beam writing. As the dry etch process used in the fabrication of waveguides has a proven record of providing SiN waveguide loss < 1dB/cm, (see chapter 2 of Weiqiang Xie's PhD) the source of the roughness is e-beam lithography. As can be seen from Fig 4.8, the roughness on the sidewall of the waveguide is periodic also indicating that the cause of the roughness is e-beam writing.

Further, for improvement in the sidewall roughness, resist reflow can be applied before the SiN etch step. By choosing a suitable temperature and time, this reflow process can greatly reduce imperfections in the resist patterns and harden the edge of the resist. Too low of a temperature will not cause the resist to reflow, while too high of a temperature will cause deformation in the resist. From the product datasheet of CSAR- 62 resist it can be found that a post bake of 130°C for 1 min on a hotplate can enhance the plasma etching resistance. Temperatures

above 130°C were investigated for the resist reflow, and the sidewall roughness was inspected with SEM imaging.

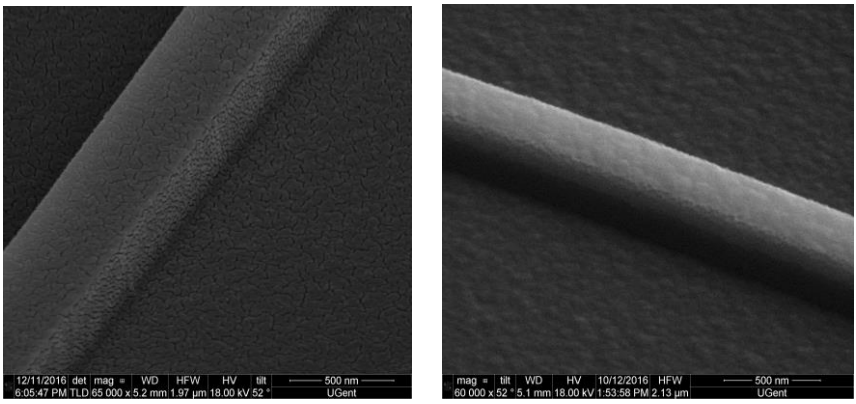

Fig. 4.9 Sidewall roughness of the waveguide after dry etching and removal of the e-beam resist at (a) a reflow temperature of 143°C for 2 min and (b) a reflow temperature of 150°C for 2 min (A thin gold layer is deposited on the top surface to reduce the charging during SEM imaging).

Fig 4.9 shows the SEM pictures of the waveguide sidewalls after resist reflow and etching for (a) a reflow temperature of 143°C for 2 min and (b) a reflow temperature of 150°C for 2 min. We can clearly see from Fig. 4.9(a) that the roughness on the sidewall of the waveguide is improved and almost vertical sidewalls can be achieved. However, in Fig. 4.9(b), the sidewall of the waveguide is rounded. This indicates that the reflow temperature of 150°C is too high, resulting in deformation of the resist. As a result, the resist at the edge of the waveguide is not thick enough for the RIE process. After a number of experiments, the appropriate resist reflowing temperature and time duration was set at 143°C for 2 min. Further, the etching directionality was inspected by cross-sectioning (CS) of the waveguide using focused ion beam (FIB). Fig 4.10 shows the FIB CS image of the waveguide after resist reflow at 143°C for 2 min on a hotplate and etching. As can be seen from Fig 4.10 vertical sidewalls were achieved using RIE.

Fig 4.11 shows the microscope image of a fully processed sample where the inset shows the Ti/Au alignment marks for overlay in e-beam surrounded by big alignment marks. The size of the alignment marks for overlay is 500 nm in width and 8 µm in length, therefore the surrounding big marks help in scanning the small marker. The next step is to deposit 780 nm thick top SiO_2 cladding layer using PECVD and to bond the III-V material on top of SiO_2, which is discussed in the

next chapter. To allow the bonding, SiN PICs were written in the center of the sample and enough margin was left around the edge for handling of the sample after bonding III-V material on top. To align the VCSELs relative to the intra-cavity grating underneath, the Ti/Au alignment marks were written 5 mm away from the SiN PICs.

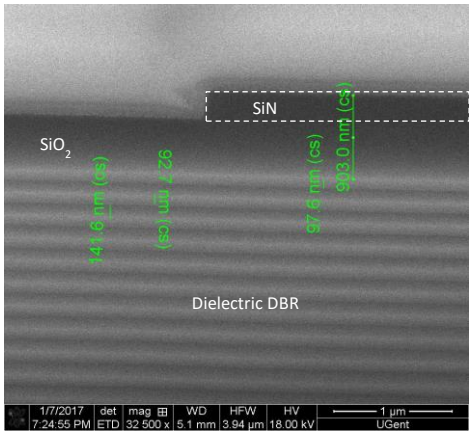

Fig. 4.10 FIB CS image of the waveguide after reflow at 143°C for 2 min.

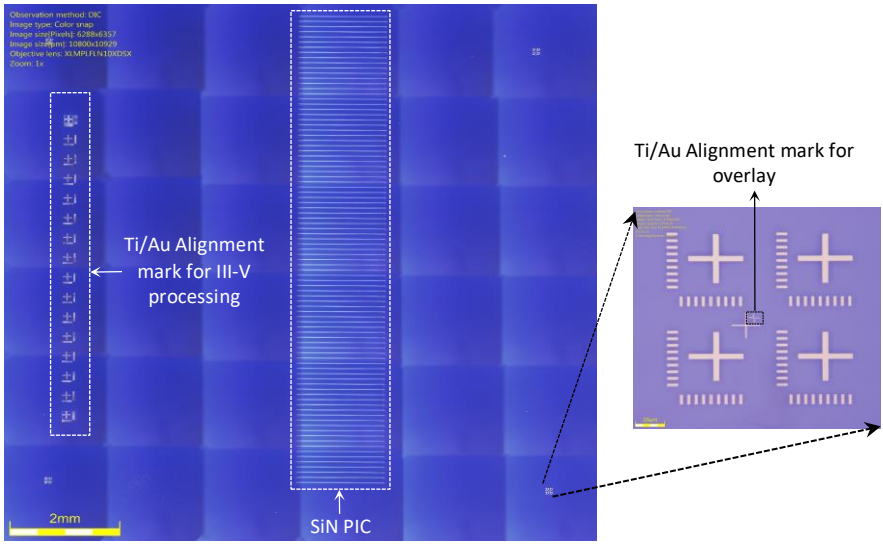

Fig. 4.11 Microscope image of a SiN PIC.

4.5 Optical characterization

It is also important to characterize the grating coupler and the waveguide losses. Waveguide losses are typically measured using a vertical coupling setup as shown in Fig. 4.12. The vertical coupling setup consist of a rotation stage to place the sample and to provide the angular rotation in horizontal direction. Optical fibers are placed above the sample under a certain angle. A grating coupler on the sample then allows to redirect the light from the fiber into the guided mode of the waveguide. A tunable Ti:sapphire laser is connected to an input fiber. The input fiber is connected to a polarization rotator (PR), which can be used to rotate the polarization and to optimize the transmission since the grating couplers are designed for a specific polarization. Next, the fiber is aligned with the input grating coupler on the sample by monitoring through a CMOS camera and the light is launched into the fundamental (TE) mode of the waveguide. The light is finally coupled out of the waveguide through another angled optical fiber and is sent to a power meter (PM) for quantitative measurement.

A SiN waveguide with length 1.6 mm and width 8 µm is written with e-beam FBMS mode. Two grating couplers with a period of 683 nm and DC of 50% are also written at both ends of the waveguide to couple the light in and out of the waveguide. The grating coupler teeth are tilted 20 degrees to avoid the back reflection to the VCSEL. The measurements are done using the vertical coupling set-up shown in Fig 4.12. The grating coupler loss is determined from the measured insertion loss of two such couplers connected to a 1.6 mm long waveguide. As discussed in Chapter 3, the grating coupler diffracts the beam at 40 degrees with respect to the z axis and 305 degree with respect to the horizontal axis. Therefore, the optical fiber is tilted with respect to the z-axis as shown in Fig. 4.12 and the horizontal angle was provided by rotating the sample (see Fig 4.12). Fig. 4.13 shows the sample with SiN waveguide rotated in horizontal direction. To couple the light into the SiN waveguide, a single mode fiber (SMJ-3A3A-780-5/125-3-2) with core size of 5 µm and cladding of 125 µm is used. For ease in alignment, a multimode fiber (MMJ-3A3A-IRVIS-62.5/125-3-2) with core size of 62.5 µm and cladding of 125 µm is used for outcoupling. The insertion loss of the grating coupler is measured for the combination of angles (in vertical and horizontal direction) close to the estimated value. A maximum peak transmission of -15.5 dB is achieved at a wavelength of 855 nm. To estimate the coupling loss to single mode and multimode fiber, the multimode fiber for out-coupling is then replaced by another single mode fiber. For such a configuration, a maximum peak transmission of -19.5 dB was achieved at a wavelength of 855 nm providing - 9.75 dB loss from the grating coupler for single mode fiber. This implies a loss of 5.75 dB for coupling to a multimode fiber.

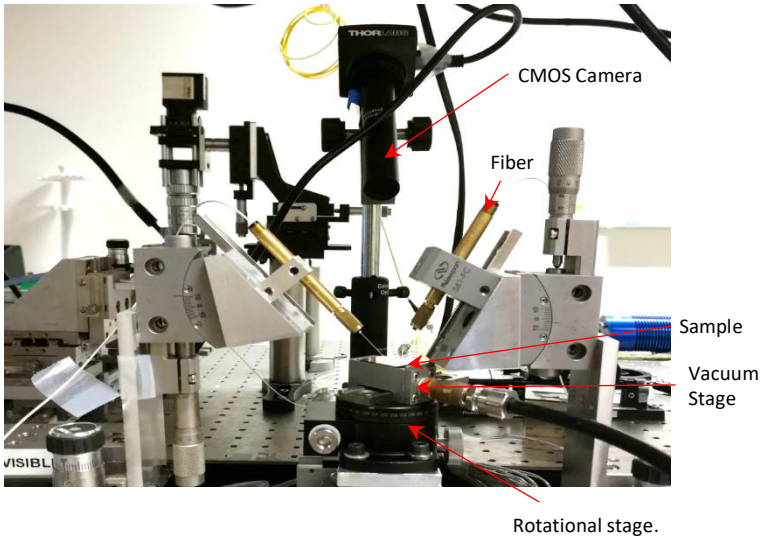

Fig. 4.12 Vertical setup to measure waveguide losses.

Fig. 4.13 Sample rotated at 305 degree and an optical fiber rotated at 36 degree to couple the light into the SiN waveguide.

4.6 Conclusion

In summary, we optimized the fabrication steps required to write the intra-cavity grating, interconnecting waveguide and grating coupler on a dielectric DBR. A L-f SiN film deposited at 270°C was found to have the lowest loss at 850 nm. The waveguides were written using FBMS writing mode to avoid stitching errors whereas intra-cavity grating and grating couplers were written using conventional

writing mode. An optimal electron dose of 140 μC/cm^2 was used to write the grating and 100 μC/cm^2 to write the waveguide.

The final e-beam procedure for high-resolution CSAR 62 resist is as follows:

1) Clean sample and bake at 150 °C for 3 min on hotplate
2) Spin coat AR-P 6200.09 (e-beam resist) at 2000 rpm for 60 sec, giving resist thickness of 200nm.
3) Bake at 150°C for 60 sec on hotplate.
4) Spin coat Electra-92 (conductive polymer) at 2000 rpm for 60 sec, giving a film thickness of 60 nm.
5) Bake at 90°C for 2 min on hotplate.
6) Expose the pattern with optimal electron dose (depending on structure) and writing mode.
7) Rinse the sample in DI water for 30 sec, to remove Electra-92.
8) Develop by immersing the sample in n-amino acid for ~90 sec
9) Immerse in stopper (IPA) for 30 sec
10) Rinse the sample in DI water for 30 sec.
11) Reflow the resist by baking it at 143°C for 2 min on a hotplate.

Finally, the SiN patterns were etched using RIE with the following optimal process parameters: 210 W power, 20 mTorr pressure, using a gas mixture of CF_4, H_2, and SF_6 with ratio 80 sccm, 7 sccm, and 3 sccm respectively.

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5

Heterogeneous Integration and Fabrication Technology

5.1 Introduction

In the previous chapter, we moved towards realizing an important building block i.e., the optical reflector on Si by integrating intra-cavity SiN waveguides, and gratings on a dielectric DBR mirror. The next step is to integrate the GaAs half VCSEL on these optical reflectors via adhesive bonding and thus fabricating an integrated Gen1 VCSEL/Gen2 VCSIL. A complete discussion of the different technologies utilized for the heterogeneous integration process is presented in this chapter. This includes techniques involved in adhesive bonding and fabrication techniques used to realize integrated Gen1 and Gen2 devices. The process of adhesive bonding was developed and performed in the clean room of UGent. Once the GaAs device layers were bonded on the Si substrates, the fabrication of Gen1 and Gen 2 lasers was performed at Chalmers University of Technology, Sweden.

5.2 Heterogeneous Integration

A widely used heterogeneous integration technology, adhesive bonding is used in this thesis to transfer the III-V epitaxial device layer onto Si substrate. The adhesive bonding technique consists three stages: (a) surface preparation of both the GaAs half VCSEL and Si photonics chip, (b) spin coating of a BCB layer on the Si chip to perform bonding, and (c) removal of the GaAs substrate post

bonding. The GaAs half VCSEL structure used in this thesis is homoepitaxially grown on a 3 inch GaAs wafer (750 µm thick) using metal organic chemical vapor phase deposition (MOCVD) by IQE Europe Ltd. The epitaxial layer stack of the GaAs half VCSEL is discussed in chapter 3, and a schematic is presented in Fig 5.1. As can be seen from Fig 5.1, etch stop layers and sacrificial layers are incorporated at both sides of the epitaxial layer stack. The two etch stop layers grown on top are to ensure a clean surface prior to bonding and the sacrificial layers at the bottom of the epitaxial layer stack enables GaAs substrate removal post bonding. The sacrificial layers we used in our device are $Al_xGa_{(1-x)}As$ and GaAs [1], which can be selectively etched with respect to each other using a selective dry or wet chemical etching process. In order to prepare a clean III-V surface prior to bonding, the chemical etchant used to remove the sacrificial layers should be able to provide a high-quality surface with high yield. Therefore, the etching properties of GaAs and $Al_xGa_{(1-x)}As$ layers in different wet etching solutions were investigated. Several tests were done to ensure homogeneous wet etching of sacrificial layers resulting in a clean and flat surface with high yield.

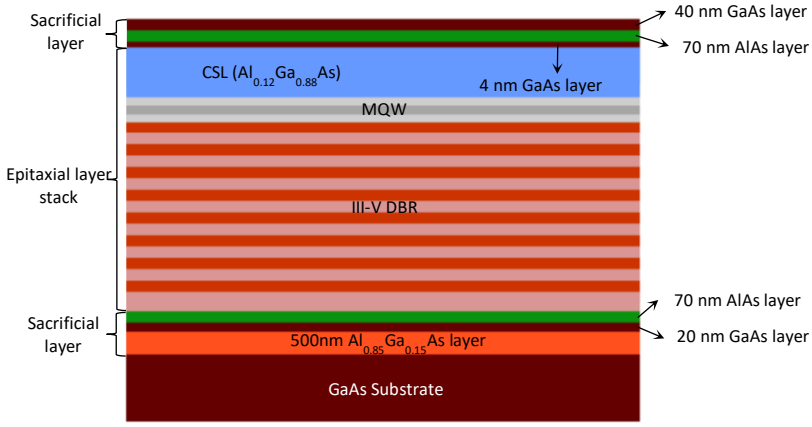


Fig. 5.1 Schematic cross section of the GaAs half VCSEL epitaxial layer stack

5.2.1 Selective wet etching of GaAs over $Al_xGa_{(1-x)}As$

Wet chemical etching procedures are widely applied in the preparation and conditioning of GaAs surfaces for the fabrication of semiconductor devices. Opposite to dry etching, wet chemical processing is impact-free and thus does not cause surface defect formation. Moreover, wet chemical processing is more simple and easy to control. The utility of a reproducible and selective etch of GaAs over $A1_xGa_{(1-x)}As$ and vice versa has become apparent in fabricating a wide range

of devices such as light-emitting diodes, semiconductor lasers, and integrated optical devices. Selective wet chemical etching of GaAs usually proceeds by oxidation, followed by dissolution of the oxide by a chemical reaction. Typically this is achieved by submerging the semiconductors in a liquid mixture consisting of two components: an oxidizing and a dissolving agent. Therefore, the oxidation and etching occur simultaneously, resulting in an etch depth dependent on the immersion time. Oxides formed on GaAs tend to be amphoteric and thus can be dissolved in either acidic or alkaline solution. Hence, several acidic and alkaline solutions are used as selective wet etchants for GaAs such as Citric acid-based etchants [2-7], Ammonium hydroxide-based etchants [7-11], and Succinic acid-based etchants [5,7]. Etch tests of GaAs over $Al_xGa_{(1-x)}As$ in every solution was not possible. Therefore two important etchants that are widely used were tested in this thesis and both of them were used in the heterogeneous integration process for a different purpose.

5.2.1.1 Citric Acid-based etching

The etching of GaAs in a citric acid($C_6H_8O_7$): hydrogen peroxide(H_2O_2) solution is a reaction rate limited process [2]. That is, the relationship between etch depth of GaAs with etching time is linear, and with temperature it is exponential. Furthermore, agitation (stirring) of the etchant does not affect the etch rate of GaAs, and the etched surface follows the crystal orientation. In the citric acid-based etchant solution, H_2O_2 is the oxidizer and the citric acid dissolves the oxide. The etch rate of GaAs depends on the volume ratio of the $C_6H_8O_7$:H_2O_2 (y:1) solution, providing a large variation in etch depth with a slight change in volume ratio. When the volume ratio (y) of the etching solution is too low the etch rate of GaAs is limited by the dissolution due to the deficiency of citric acid to remove the oxide. Further, with very high volume ratio (y) both the GaAs and $Al_xGa_{(1-x)}As$ layer has a high etch rate making the solution nonselective. A study shows that the etch rate of GaAs abruptly increases (with a value of ~ 200 nm/min) while the etch rate of $Al_xGa_{(1-x)}As$ ($x > 0.4$) is still very low when the volume ratio (y) is between 3 and 5. Once the top GaAs layer is etched, the $Al_xGa_{(1-x)}As$ layer gets exposed and the etch rate of $Al_xGa_{(1-x)}As$ decreases rapidly due to the formation of Al_xO_y. With an increase in Al composition, the etching selectivity between GaAs and $Al_xGa_{(1-x)}As$ layer increases but the etching surface starts to be of poor quality due to oxidation. In case the Al composition is very high (> 0.7), the oxidation of the $Al_xGa_{(1-x)}As$ layer is very severe regardless of the selective etchants used.

The $C_6H_8O_7$ (50%):H_2O_2(30%) (5:1) etching solution is prepared approximately 15 min before etching and is placed on a shaker, to mix it homogeneously and to allow the etchant to return to room temperature. The 40 nm thick sacrificial GaAs layer on top of the 70 nm thick AlAs etch stop layer is

removed selectively by immersing it into the $C_6H_8O_7$:H_2O_2 solution for 20 sec. While etching the GaAs layer, a color change on the surface of GaAs layer is observed. Once the GaAs layer is etched and the AlAs layer is exposed, the etching surface appears to be dark blue. In case of over-etch the color of the surface changes to a yellowish color indicating that the AlAs layer is over-exposed and the surface is getting oxidized. After etching the GaAs sacrificial layer, the exposed AlAs layer should be selectively removed immediately; otherwise, the surface will further oxidize when it comes in contact with air and a completely oxidized AlAs layer is very hard to remove.

5.2.1.2 Ammonia-based etching

The mechanism for selective etching of GaAs in ammonium hydroxide (NH_4OH)/hydrogen peroxide (H_2O_2) is the same as in the case of the citric acid-based solution. Here H_2O_2 again acts as an oxidizing agent and NH_4OH dissolves the oxidized surface. However, the etching and stability of the etched surface depend on the pH of the NH_4OH/H_2O_2 solution. In [8], etching of GaAs in a NH_4OH/H_2O_2 solution was investigated by adjusting the pH of the solution at different volume ratios. It was concluded that a solution with pH below 6 can be used to grow oxide on the surface (galvanically or anodically) while a solution with pH value greater than 6 can be used to etch the GaAs surface. Solutions with pH value between 6.0 - 7.1, can result in smoothly etched surfaces and for pH 7.0, the etching of GaAs with respect to $Al_xGa_{(1-x)}As$ was found to be selective. As the pH further increases to >7.2, dissolution of the oxidized layer limits the efficiency of etching of GaAs and results in surface roughness. In NH_4OH/H_2O_2 solution the etch rate decreases with time due to a deficiency of the etching solution to remove the oxidized layer and a continuous agitation in the etching solution is required to further increase the etch rate. Therefore, the etch rate of GaAs depends on the effective mechanical removal of the oxidized layer formed on the surface either by agitating the etchant or by wiping the surface with a polishing cloth [8], or by using a jet-thinning instrument for spray etching [9]. The latter technique of spray etching ensures a significant improvement in etched surface quality. Etching with a NH_4OH/H_2O_2 solution is often used as a processing step in the fabrication of GaAs-based devices to remove the native oxide layer from the GaAs surface. Moreover, treatment with aqueous ammonia solution renders the surface properties suitable for atomic layer deposition of a gate dielectric [12].

A NH_4OH:H_2O_2 (1:19) etching solution was prepared 15 min before the etching experiments [1]. An etch rate of ~3.5 μm/min was achieved for GaAs but the etching of the AlAs surface was very slow. The 40 nm thick GaAs layer was etched in 10-15 sec and a color change was again observed. A reddish surface indicated the removal of the GaAs layer leaving the AlAs layer exposed. A slight over etch again turned the top surface to a yellowish color indicating the oxidation

of AlAs. In case of over-etch, sometimes it was difficult to remove the AlAs layer. Therefore, by etching GaAs over AlAs in a $NH_4OH:H_2O_2$ (1:19) solution, reproducible results could not be achieved.

In summary, amongst the two selective etchants, the NH_4OH-based etch must be agitated vigorously throughout the etch so that the pH at the sample surface remains constant, while the citric acid-based etch is not affected by agitation. For final surface preparation, etching of GaAs over AlAs in citric acid is preferred over NH_4OH due to the better surface roughness and yield. However, NH_4OH etchants are still useful for processes such as GaAs substrate removal, where selective etching of GaAs with high etch rate is required.

5.2.2 Selective wet etching of $Al_xGa_{(1-x)}As$ over GaAs

The quality of the final GaAs surface after removal of an $Al_xGa_{(1-x)}As$ layer depends on the Al content in the layer, the extent of oxidation of the layer and the etchant used. In literature, several wet chemical etchants such as $HF:H_2O$ [13-16], $BHF:H_2O$ [3] and $HCl:H_2O$ [17] have been reported to provide excellent selective etching of $Al_xGa_{(1-x)}As$ over GaAs when $x > 0.6$. In this thesis, the quality of the final surface after etching of $Al_xGa_{(1-x)}As$ in HF and HCl-based etchants was investigated.

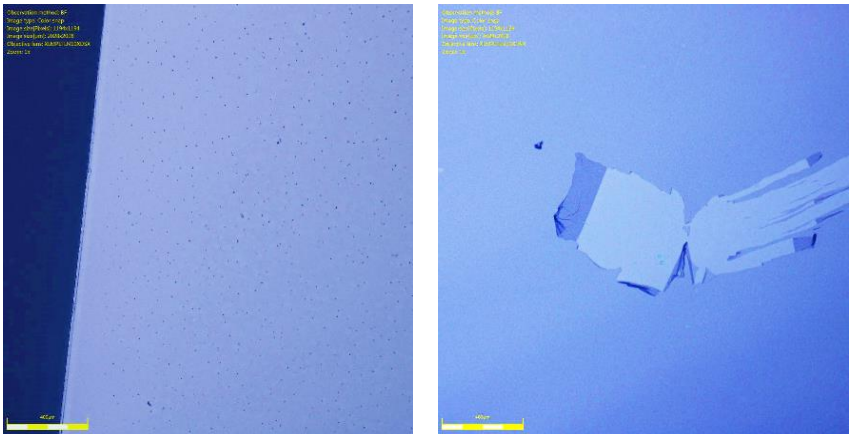
5.2.2.1 HF-based etching

The selective etching of $Al_xGa_{(1-x)}As$ over GaAs or $A_{lx}Ga_{(1-x)}As$ with low Al composition using hydrofluoric acid (HF) was proposed for a technique that is known today as epitaxial lift-off (ELO) [13-16], where the device film is separated from the GaAs substrate by etching. Etching of $Al_xGa_{(1-x)}As$ in HF is fully isotropic, where the released structure can possess arbitrary orientation. This method has been extensively explored to reduce the cost of III–V devices by reusing the substrates. An $Al_xGa_{(1-x)}As$ sacrificial layer inserted between the device film and the substrate can separate the device layer from a GaAs substrate. Subsequently, this same method has been applied by many researchers to successfully peel GaAs thin films from its parent substrate and transfer it onto desirable substrates for various applications [13-16]. An investigation revealed that the etch rate of $Al_xGa_{(1-x)}As$ in diluted HF with certain volume concentration increases with increase in Al composition [15]. Further, a higher concentration of HF shows a higher etch rate of $Al_xGa_{(1-x)}As$ with a fixed Al composition. It was concluded that HF in varying concentrations is an effective isotropic etchant for $Al_xGa_{(1-x)}As$ when the aluminium fraction is greater than $x > 0.5$ while exhibiting a rapid decrease in etch rate for Al fraction below $x < 0.4$ [15]. Also, a diluted HF with volume concentration 2 % showed a remarkable etch selectivity ($>10^6$) with GaAs, for Al fraction > 0.7.

Although etch selectivity of an AlAs over GaAs is very high (~10^6) and it has been used and investigated for ELO, there have been reports on the degradation of the final GaAs surface due to micro-particles formed from etching residues [13-16]. During the etching of AlAs in HF, a residue layer appears on the surface. Formation of residue upon etching in HF is also confirmed by the microscope images shown in Fig.5.2. The origin of these residues is explained in [13,14] by studying the chemical reaction during the etching of AlAs in HF. The chemical reaction during etching is shown below [13,14].

$$AlAs_{(s)} + 3HF_{(aq)} + 6H_2O \rightarrow AsH_{3_{(g)}} + [AlF_n(H_2O)_{6-n}]_s^{(3-n)+} + [(3-n)F^-]_{aq} + nH_2O \quad (5.1)$$

Where n=1,…,3. Among all the by-products formed during etching, AsH_3 is gaseous and can form bubbles and diffuse away from the interface to the atmosphere. Under certain conditions AlF_3 is formed, which is solid and hard to dissolve into the solution. The formation of AlF_3 can stop the etching. Besides these primary by-products, solid As_2O_3 can also be formed on the substrate depending on the oxygen concentration in the etchant.



(a) (b)

Fig. 5.2 Microscope image of the final GaAs surface after etching of GaAs in citric acid and AlAs in (a) 2% HF and (b) 10% HF

A stock HF solution with 2% and 10% concentration was prepared by diluting concentrated HF (40%). HF is a highly corrosive liquid and it should be handled with extreme care. The surface morphology of the GaAs layer after the removal of the final etch stop layer (AlAs) by exposure to HF was examined by optical microscopy and is shown in Fig 5.2. From Fig. 5.2, the formation of a residue

layer was confirmed. The size and the type of residue depended on the concentration of the HF used (see Fig 5.2). These residue layers have low solubility and stay on the surface but could be easily removed by a cotton tip. However, cotton tips are not clean room compatible and the process can reduce the yield of adhesive bonding. Therefore a spray bottle can be used to disperse DI water on the etched surface, to rinse off the residue layer. But some of the residue still stays at the surface, which can further reduce the device performance and yield of bonding. Therefore, a post-chemical treatment is required to get rid of these residues completely [17,18]. In a next section, such a chemical treatment, called digital etching, will be explained.

5.2.2.2 HCl-based etching

To overcome the above mentioned problem, another solution was also proposed by using a different sacrificial layer that can be selectively etched by a non-HF solution [14], leaving no insoluble etching by-products on the GaAs surface. For example, phosphide-based materials (InGaP, InAlP, InP and so on) have been widely applied as etch stop layers for the selective etching of arsenide-based materials (GaAs, InGaAs and so on), and vice versa. An InAlP layer in combination with GaAs has shown an excellent etch selectivity with high-quality surface without any residue when HCl is used as etchant [14]. Although it is an attractive solution, it does not help for the existing epi where AlAs and GaAs layers are already embedded as a sacrificial layer and the search of a viable solution to achieve a good quality surface continues.

Hydrochloric acid (HCl), which is a well-known acid to etch phosphide-based materials can also be used to etch $Al_xGa_{(1-x)}As$ [17,18]. Not much data is available on the etching of an $Al_xGa_{(1-x)}As$ layer with HCl. However, [18] states that $Al_xGa_{(1-x)}As$ with Al composition > 0.6 can be etched by HCl while it does not attack GaAs and only removes the oxide of GaAs. The roughness on GaAs induced by HF and HCl was examined in [14] by leaving blanket GaAs wafers in HCl or HF for 24 h. The atomic force microscopy (AFM) afterwards showed an RMS roughness of the 24h-HCl wafer of only 0.327 nm, much lower than the 1.666 nm RMS roughness after 24 h in HF. This result indicates that HF attacks GaAs severely and causes excess surface roughness.

To perform the etching experiment, HCl(36%):H_2O(30%) (1:1) etching solution was prepared which gives an exothermic reaction. Hence, to ensure that the solution is at room temperature, the solution was allowed to cool down for 30 minutes. The AlAs layer is etched by immersing the III-V sample in the etching solution for 1 min immediately after etching the top GaAs layer in citric acid.

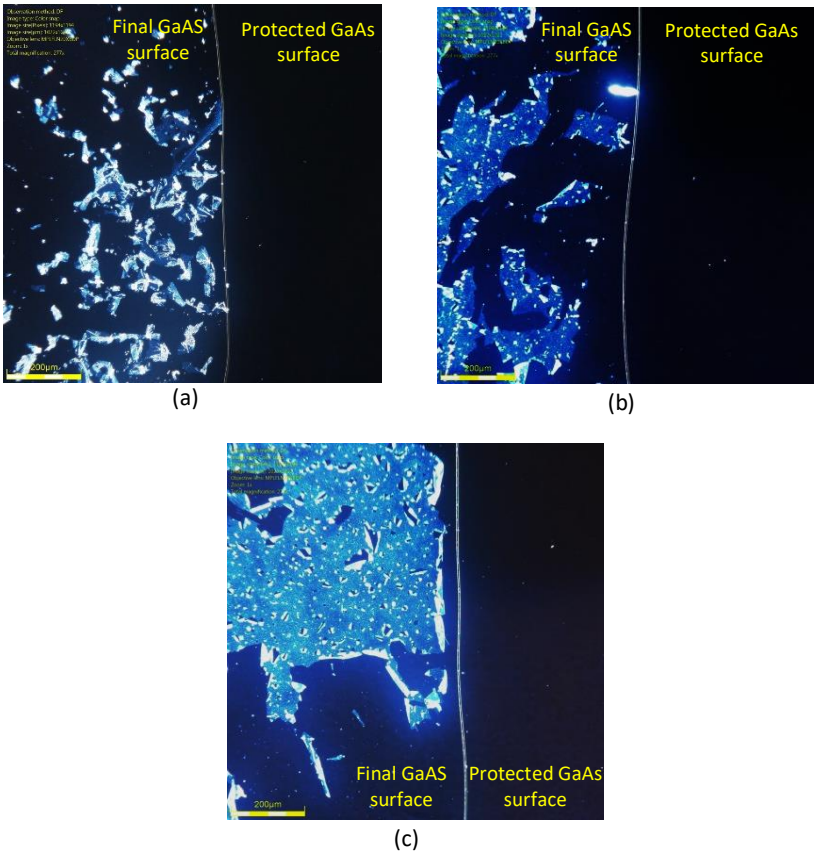


Fig. 5.3 Dark field microscopic image of the final GaAs surface after etching of GaAs in citric acid for (a) 20 sec (b) 40 sec and (c) 60 sec . The AlAs layer is etched in HCl:H_2O (1:1) for 1 min.

The surface morphology on the GaAs layer after the removal of the etch stop (AlAs) layer by exposure to HCl was examined by dark-field microscopy and is shown in Fig 5.3. From Fig 5.3, it is evident that the sample etched in HCl:H_2O again contained a thin, non-uniform layer of residual material that remains on the underlying smooth GaAs surface following the selective AlAs etch. These residue layers are again enriched by elemental arsenic or arsenic oxide and show a web-like morphology. This morphology persists even after additional exposure of the surface to HCl:H_2O. The size of the web-like structure varies depending on the exposure time of the GaAs layer to citric acid and is shown in Fig.5.3. The etching time of the GaAs layer in citric acid was 20sec, 40sec and 60sec for Fig 5.3 (a), (b) and (c) respectively whereas the AlAs layer is removed in 1 min in HCl:H_2O. The size dependence of the web-like structure can be seen as a result of the extent

of oxidation of AlAs layer by exposure to citric acid. As can be seen from Fig 5.3, over etching of GaAs in citric acid increased the size of the web-like morphology. For the particular case where the GaAs layer is etched in citric acid for 20 sec and AlAs in HCl:H_2O for 1 min, the web-like morphology could be completely rinsed off only by dispersing DI water with a spray bottle and no post chemical treatment was required. However, in case the over-etch is increased, the size of web-like structures increases and residue layer sticks to the GaAs layer and the removal of the residue becomes more difficult. Again, a post-chemical treatment such as digital etching is required to completely get rid of these residues.

In conclusion, the selective etching of $Al_xGa_{(1-x)}As$ layer in HF-based etchant, which is a highly corrosive acid requiring special handling and extra protection, is less attractive and attacks the final GaAs surface severely, resulting in surface roughness. Contrary to that, the use of HCl ensures better surface quality and is safer to use.

5.2.3 Digital wet etching

Normal III-V semiconductor wet etching occurs by combining two chemical reactions into a single chemical etching system. The digital etching technique differs from the normal etching method by separating the chemical reaction at the surface into two distinct processes. The first chemical reaction forms the surface film compound to a fixed depth due to the self-limiting nature of the first chemical reaction. The surface is then cleaned to prevent mixing of the first chemical with the second chemical in the next step. The second chemical reaction selectively removes the newly formed surface film compound but does not affect the unreacted GaAs region underneath. These two steps form an etching cycle and by repeating the etch cycles, etching can be achieved in a digital manner [17,18]. Therefore, in the wet chemical digital etching, the etch depth is dependent on the diffusion limited thickness of the surface film formed in the first step. An essential component in wet chemical digital etching is to develop a diffusion limited chemical reaction at the surface. H_2O_2 which is a well-known oxidizer forms a stable native oxide of GaAs by a self-limiting (diffusion- limited) process. It has been reported that an oxide thickness of 115 Å is formed after soaking a GaAs sample in H_2O_2 for 6 days at room temperature [19]. Thus H_2O_2 is used in a 1^{st} step to form a thin oxidized GaAs layer by this self-limiting process. In the 2^{nd} step, a HCl:H_2O (1:1) solution is used to etch away the oxide layer formed on the GaAs surface without affecting the unreacted GaAs material underneath. Therefore, the single etch cycle in the digital wet etch process used in this thesis consists of 1 min soaking the sample in H_2O_2 to oxidize the GaAs surface, rinsing the sample in DI water, blow drying with a N_2 gun, followed by 1 min soaking in HCl:H_2O (1:1) to remove the oxidized GaAs.

The digital etching was performed on the sample immediately after etching the AlAs sacrificial layer in HCl or HF. Fig 5.4 shows the dark field microscope image of the final GaAs surface after etching of GaAs in citric acid for 20 sec and AlAs in HCl:H_2O for 1 min. Fig 5.4 (a) shows the final surface without digital etching whereas Fig 5.4 (b) shows the final surface at the same location after digital etching. As can be seen from Fig 5.4 (b), the residues from AlAs etching were completely removed after repeating 3 cycles of digital etching and a smoother GaAs surface was achieved.

An AFM image of the final GaAs surfaces before and after treatment with three cycles of digital etching is also shown in Fig 5.5. From the AFM images, it is evident that the residue material remains on the underlying smooth GaAs surfaces following the selective AlAs etch in HCl:H_2O (1:1). For the sample shown in Fig. 5.4 (a), these residues account for the rougher surface, which had an rms roughness of 3.9 ± 0.16 nm. The residue had a height of 15-20 nm. As shown in Fig. 5.5 (b), the sample etched in HCl:H_2O (1:1) reflected an improvement in the surface quality as compared to the samples prepared without the digital etch and the surface had an rms roughness of 0.47 ± 0.18 nm.

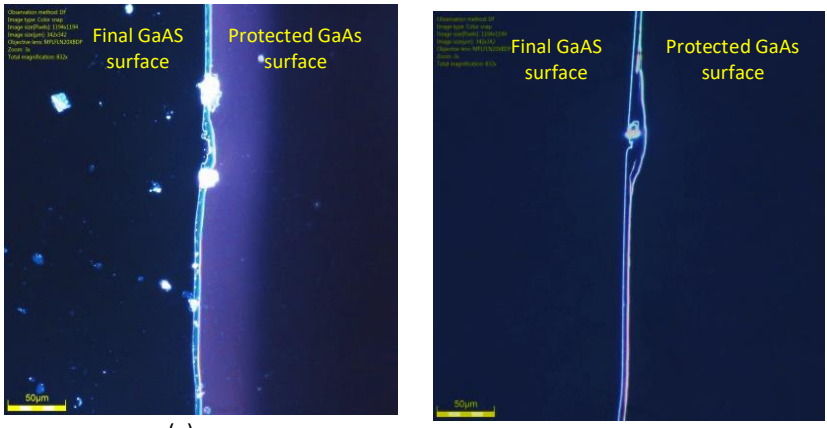


Fig. 5.4 Dark field microscope image of the final GaAs surface after etching of GaAs in citric acid for 20 sec and AlAs in HCl:H_2O (1:1) for 1 min (a) before treatment with the digital wet etch and (b) after treatment with the digital wet etch

To compare the surface quality of the etched GaAs surface with that of the dielectric DBR and an unetched GaAs surface, an AFM image of the surface of the dielectric DBR and the GaAs surface without any etch were also taken and are

shown in Fig 5.6. The surface had an rms roughness of 0.59 ± 0.06 nm, and 1.4 ± 0.26 nm for dielectric DBR and GaAs surface without any etch respectively.

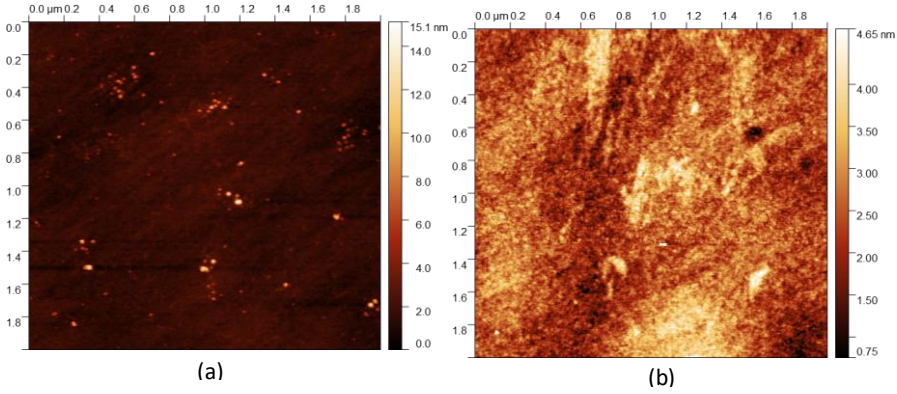


Fig 5.5 AFM image of the final GaAs surface after etching of GaAs in citric acid for 20 sec and AlAs in HCl:H_2O (1:1) for 1 min (a) before treatment with the digital wet etch and (b) after treatment with the digital wet etch.

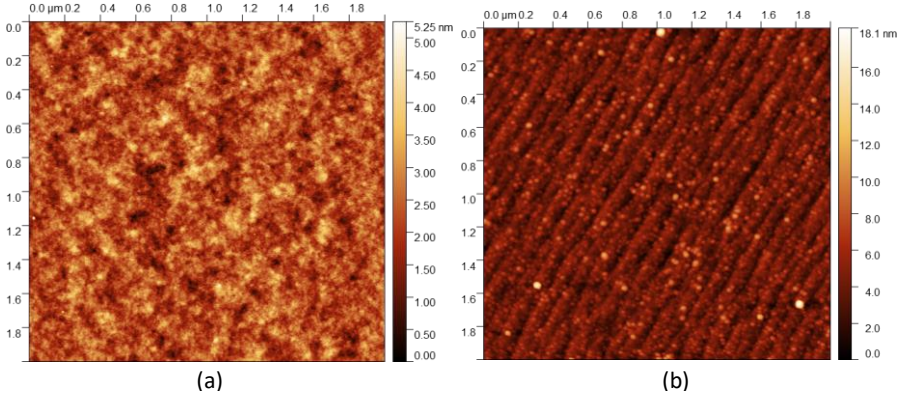


Fig 5.6 AFM image of (a) Ta_2O_5/SiO_2 DBR surface and (b) GaAs surface without any etch.

Apart from removing the residual layer, digital etching can also be used to etch thin GaAs layers in a controlled way. It has been shown that by etching GaAs material in a digital manner a precise, reproducible and controlled GaAs etch rate of approximately 1.6 nm/cycle can be achieved [17]. To avoid optical band-to-band absorption in the final devices, the 4 nm thin GaAs layer (see Fig 5.1) also needs to be removed using a digital wet etch process. Therefore during the 3

cycles of digital wet etching, the 4 nm GaAs layer on top of the CSL is also removed.

Thus in summary, among the presented etchants for selective etching, citric acid and HCl are preferred to etch GaAs and AlAs respectively. Finally, with 3 cycles of digital wet etching in H_2O_2 and HCl:H_2O, a smooth surface can be achieved with high yield. Therefore, digital wet etching proves to be an effective treatment for final surface preparation of GaAs for bonding. The use of HCl opposed to HF simplifies the process by reducing the number of chemical solutions involved in etching and by providing a safer environment. NH_4OH is still useful where coarse removal of GaAs is required.

5.3 Adhesive bonding

Bonding one material onto another is an important process in the microelectronics industry [20–23]. A comprehensive review of bonding techniques can be found in [24]. The adhesive bonding technique which employs an intermediate adhesive layer between two substrates offers several advantages over direct bonding, such as low bonding temperature (typically below 450°C depending on the polymer), good tolerance to particles and insensitivity to the surface topography of the bonding surfaces [24]. Therefore, less intensive cleaning procedures are required and higher yield can be obtained. The most important parameters in adhesive bonding are: the choice of the polymer used as the adhesive, the bonding pressure, bonding temperature, temperature ramp profile and chamber pressure. One of the most popular adhesives for wafer bonding is divinylsiloxane-bisbenzocyclobutene (DVS-BCB). It was developed in the late 1980's by Dow Chemical Company as a low dielectric constant (low-k) polymer intended to replace silica as a dielectric in on-chip interconnects [25]. Today, under the commercial name Cyclotene, it is a well-known material with a variety of applications in microelectronic packaging and interconnect applications. Chemically, DVS-BCB is a monomer molecule that polymerizes to create a low-k dielectric material with some advantageous properties. Important beneficial properties that make DVS-BCB a suitable candidate for adhesive bonding is its low dielectric constant, low moisture absorption, low curing temperature, a high degree of planarization, low level of ionic contaminants, high optical clarity, good thermal stability, excellent chemical resistance, and good compatibility with various metallization systems [25-28]. The drawback of DVS-BCB is its low thermal conductivity. Below we will elaborate on the adhesive bonding process used in this work.

5.3.1 Preparation of dielectric DBR on Si sample

The important process steps in the preparation of the DBR samples before bonding is to remove any contamination from cleaving or post-processing steps and to spin coat the DVS-BCB layer on the surface. Although the adhesive bonding is somewhat tolerant to particle contamination, it is essential to remove any residual particles on the bonding surface, since we want to achieve a bonding layer thickness of 40-50 nm. A careful preparation of the sample ensures high yield in the adhesive bonding procedure.

5.3.1.1 Gen1 DBR sample (Dielectric DBR on Si)

As mentioned before, the Gen1 devices are fabricated by bonding III-V half VCSELs onto a 20 pair dielectric DBR on Si. The dielectric DBR wafer was cleaved into 10 mm × 12 mm samples. Before cleaving, a thin layer of photoresist was spin coated to protect samples from small Si particles (by-products of the cleaving). After cleaving, the protective photoresist was removed using acetone, iso-propyl alcohol (IPA) and DI water. The remaining organic contamination was removed by a 10 min O_2-plasma etching in a Tepla barrel etcher [29]. The surface of the DBR was then cleaned using a Standard Clean 1 (SC-1) solution, comprising an aqueous ammonia solution (NH_4OH), hydrogen peroxide (H_2O_2) and deionized (DI) water in volume ratios of 1:1:5, respectively. The DBR sample was immersed in SC-1 at 70 °C, for 15 minutes, after which it was rinsed with DI water and dried. The SC-1 cleaning is very effective in removing organic residues and particles.

Next, the standard BCB solution (CYCLOTENE 3022-35 resins) was diluted with solvent (Mesitylene (MES)) to achieve an ultra-thin bonding layer thickness [30]. The dilution ratio depends on the sample (planar or non-planar surface) and the desired DVS-BCB bonding thickness. A stock solution of DVS-BCB was prepared by mixing 1 volume of Dow Chemical's Cyclotene 3022-35 solution and 8 volumes of Mesitylene. By using this solution, one can realize a bonding thickness of 40-50 nm on a planar sample in a reproducible way. The BCB:MES (1:8) solution was spin coated onto the DBR sample at a spin speed of 3000 rpm for 40 sec (see Fig 5.9 (b)). The spin-coated DBR sample is then baked at 150°C on a hotplate for 10 min, to let mesitylene evaporate, after which the substrate is slowly cooled down to 90°C in 20 min.

5.3.1.2 Gen2 DBR sample (SiN PIC on Gen1 DBR)

As discussed before, for the fabrication of Gen2 devices, the Gen1 DBR wafers with dielectric DBR on Si were modified by depositing and patterning the SiN intra-cavity waveguide and grating on top of it. More details about the processing

of the SiN PICs can be found in Chapter 4. In short, the SiN PICs were patterned on the Gen1 DBR by PECVD deposition of the SiO_2 cladding layer and SiN waveguide layer, and 3 steps of e-beam patterning and dry etching. After the SiN waveguide structures were patterned, a top SiO_2 cladding layer was deposited. The thickness of the top cladding layer depended on the resonance wavelength of the Gen2 VCSIL, as explained in Chapter 3. The size of the Gen2 DBR sample was 15 mm × 20 mm with a 1.6 mm × 10 mm SiN PIC pattern in the center. To allow the alignment of Gen2 VCSELs relative to the patterned SiN PIC the Ti/Au alignment marks were patterned 5 mm away from the SiN PIC. The cleaning of the Gen2 DBR sample is a bit different from the Gen1 DBR. Since the Gen2 DBR goes through various processing steps, an intensive cleaning before each step was done to ensure a clean surface for bonding. This cleaning included a short ultrasonic cleaning of the sample in an acetone bath, cleaning with acetone, IPA and DI water, and 10 min O_2 plasma. The SC-1 cleaning was avoided in this case due to the peeling of the Ti/Au alignment marks in SC1 solution.

A stock solution of DVS-BCB was prepared by mixing 1 volume of Dow Chemical's Cyclotene 3022-35 solution with 3 volumes of Mesitylene. The BCB:MES (1:3) solution was then spin coated onto the Gen2 DBR sample at a spin speed of 3000 rpm for 40 sec. Since the top SiO_2 cladding layer follows the topography of SiN PICs, the surface of the Gen2 DBR sample is non-planar. Therefore the DVS-BCB layer planarizes the sample by filling the topography with DVS-BCB (see Fig 5.10 (b)). With the solution mentioned above, a bonding thickness of 50-60 nm can be achieved on a non-planar sample. The spin-coated DBR sample is then baked at 150°C on a hotplate for 10 min to let mesitylene evaporate, after which the substrate is slowly cooled down to 90°C in 20 min.

5.3.2 Preparation of III-V sample

For realizing Gen1 VCSEL and Gen2 VCSIL devices, the same III-V wafer was utilized. Depending on the size of the target DBR sample, a small III-V die was cleaved. The size of the III-V die was 8 mm × 10 mm and 4 mm × 12 mm for the Gen1 and Gen2 DBR sample respectively. The protective photoresist on the III-V die is then removed using acetone, IPA, and DI water. A short 2 min O_2-plasma (600W) was used to remove the remaining organic contamination.

In comparison to Si, for III-V there are no equivalent chemical cleaning solutions which do not attack III-V. Also, ultrasonic cleaning is not advised in case of III-V, since III-V materials are very fragile. To overcome this problem, two sacrificial layers are grown on the top of our epitaxial layer stack, as described in section 5.2. As can be seen from Fig 5.1, a 40 nm thick GaAs layer was grown on top of 70 nm thick AlAs layer to act as a sacrificial layer. As described in section 5.2, these layers can be removed by selective wet etching prior to bonding.

The schematic of etching to remove the sacrificial layers is presented in Fig 5.7. Before etching the sacrificial layers, any native oxide on top of the GaAs surface is removed by dipping the III-V die in a HCl:H_2O (1:1) solution for 30 sec. The GaAs sacrificial layer is removed by Citric acid:H_2O_2 (5:1) in 20 sec (see Fig 5.7 (a)) and the AlAs is removed by a HCl:H_2O(1:1) solution in 1 min (see Fig 5.7 (b)). 3 cycles of digital wet etching was then performed on the etched surface by alternating the exposure of the GaAs surface to H_2O_2 and HCl:H_2O (1:1) for 1 min in separate steps (see Fig 5.7 (c)). While performing digital etching, the remaining 4 nm GaAs layer is also removed with a rate of 1.6 nm/cycle. The III-V sample is now ready to be bonded with the DBR sample (Fig 5.7 (d)). For better adhesion between III-V and the BCB, a 10 nm thin SiN layer was deposited on the III-V immediately after removal of the sacrificial layer and digital etching. The next step is to bond the III-V sample to the Gen1 and Gen2 DBR samples.

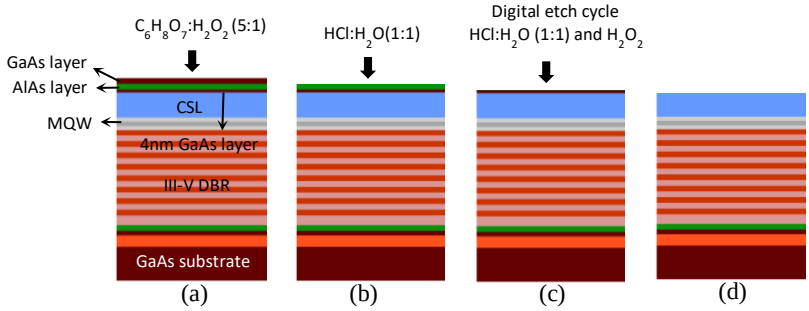


Fig. 5.7 Sacrificial layer etching prior to bonding: (a) 30 sec dip in HCl:H_2O (1:1) to remove the native oxide, (b) etching of the GaAs layer in $C_6H_8O_7$:H_2O_2 (5:1) solution for 20 sec, (c) etching of the AlAs layer in HCl:H_2O (5:1) solution for 1 min, (d) 3 cycles of digital etching in HCl:H_2O (1:1) and H_2O_2 solution.

5.3.3 Machine bonding

Machine bonding is employed to control the pressure applied on the sample, resulting in an improvement of thickness uniformity of the bonding layer. A Suss MicroTec ELAN CB6/8L wafer bonding machine is used in this work. Fig. 5.8 (a) shows the interior of the bonding machine, where a pressure head is used to apply force. Fig. 5.8 (b) shows the transport fixture where the sample can be mounted between 2 Pyrex glass plates. To transport the sample to the bonding machine, a carrier wafer made of Pyrex glass (1200 µm thick, 100 mm diameter) is mounted on the transport fixture. The DBR sample is then placed on the carrier wafer and the clean III-V die is flipped on the DBR with the epitaxial device layer facing the dielectric DBR (Fig 5.9 and 5.10). After that, another carrier wafer is placed on top of the III-V and the stack is then clamped between these two carrier

wafers by the transport fixture. The whole transport fixture is then loaded into the processing chamber of the wafer bonding tool. Fig. 5.9 and 5.10 shows the schematic of the bonding process for Gen1 VCSELs and Gen2 VCSILs respectively.

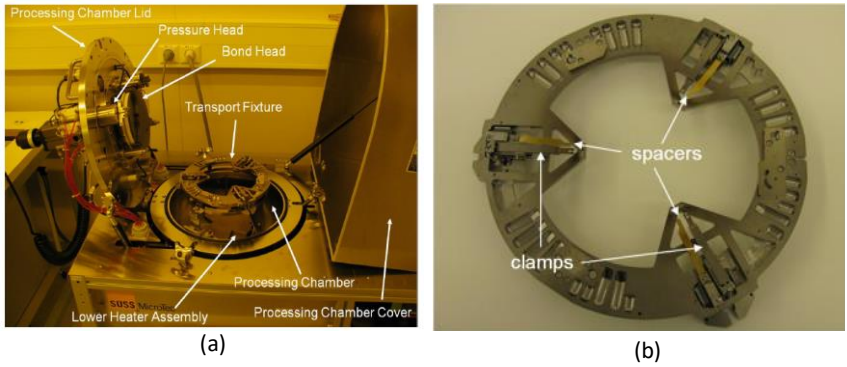


Fig 5.8 (a)The basic components of the Süss Microtec ELAN CB6L wafer bonder. (b) transport fixture for handling 100 mm diameter wafers

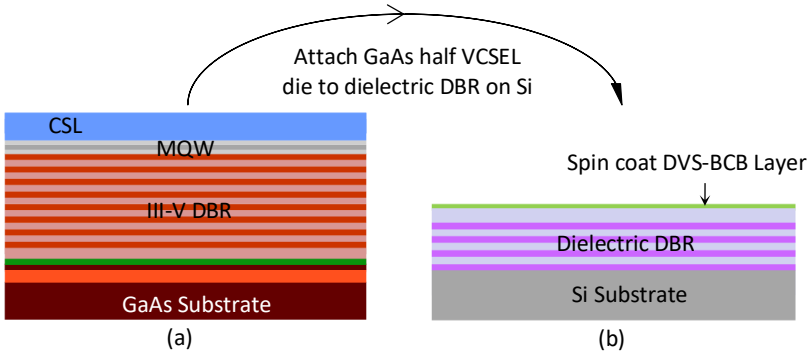


Fig. 5.9 Schematic of bonding III-V on Gen1 DBR sample: (a) III-V epitaxial layer after removing the sacrificial layer (b) Gen 1 DBR sample with spin-coated DVS-BCB.

After loading the fixture into the bonding chamber, the chamber lid is closed properly. The chamber is then pumped-down (target pressure 10^{-3} mbar) and heated to 150°C with a ramp of 15 °C/min for 10 min, while applying pressure on the III-V/SOI stack. The actual bonding pressure (the applied force per area of the III-V die) is kept in the range of 200 to 400 kPa. After maintaining the pressure on the dies for 10 min at 150 °C, the temperature is increased up to 280 °C, with a ramp of 1.5 °C/min. Upon reaching 280 °C, the dies are kept at this temperature

for 60 min in a nitrogen atmosphere to cure the DVS-BCB layer. After curing, the bonded samples are cooled down (at 6-10 °C/min) and unloaded from the processing chamber. The next step is to remove the thick GaAs substrate.

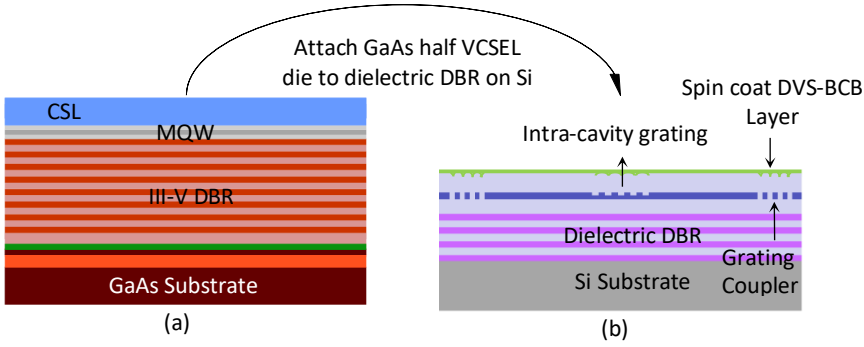


Fig. 5.10 Schematic of bonding III-V on Gen2 DBR sample: (a) III-V epitaxial layer after removing the sacrificial layer (b) Gen 2 DBR sample with spin-coated DVS-BCB.

5.3.4 Substrate removal

After bonding, the 750 µm thick GaAs substrate needs to be removed completely by selective etching. Before removing the GaAs substrate, a wax (CrystalBond 509) [31] is applied around the die to protect the edges of the III-V during the etching process. CrystalBond 509 can be dissolved in acetone. Its melting point is at 121°C and its softening point is at 71°C. The CrystalBond 509 wax exhibits strong adhesion and high chemical resistance which makes it suitable for sidewall protection during the substrate removal process. The CrystalBond 509 was melted by heating it to 140 °C in a glass petri dish. With the help of a sharp cotton tip, the melted wax was carefully applied at the edges of the bonded III-V (See Fig 5.12 (a)). In case the wax spreads on top of the bonded III-V die, it can be wiped by a clean cotton tip dipped into Acetone. The schematic of the substrate removal process is shown in Fig 5.11. The major part of the GaAs substrate can be removed either by a mechanical grinding (~500 µm) or by a fast non-selective wet etching (~700 µm) (Fig 5.11 (a)). After that, the remaining GaAs substrate is removed selectively where the etching stops once the $Al_{0.85}Ga_{0.15}As$ etch stop layer is reached (Fig 5.11(b)). The etching solution used in this step is NH_4OH: H_2O_2 (1:19). The 500 nm thick $Al_{0.85}Ga_{0.15}As$ layer is removed selectively in HCl:H_2O_2 (1:1) in 5 min and the etching stops when the GaAs layer is reached. The 20 nm thick GaAs layer is removed in $C_6H_8O_7$:H_2O_2 (5:1) in 10 sec. The final 70 nm thick AlAs layer is then removed in HCl:H_2O in 1 min followed by 3 cycles of digital wet etching. The microscope images of the surface of III-V during different

etch steps are shown in Fig 5.12. Below we elaborate on the mechanical substrate removal and full wet substrate removal process.

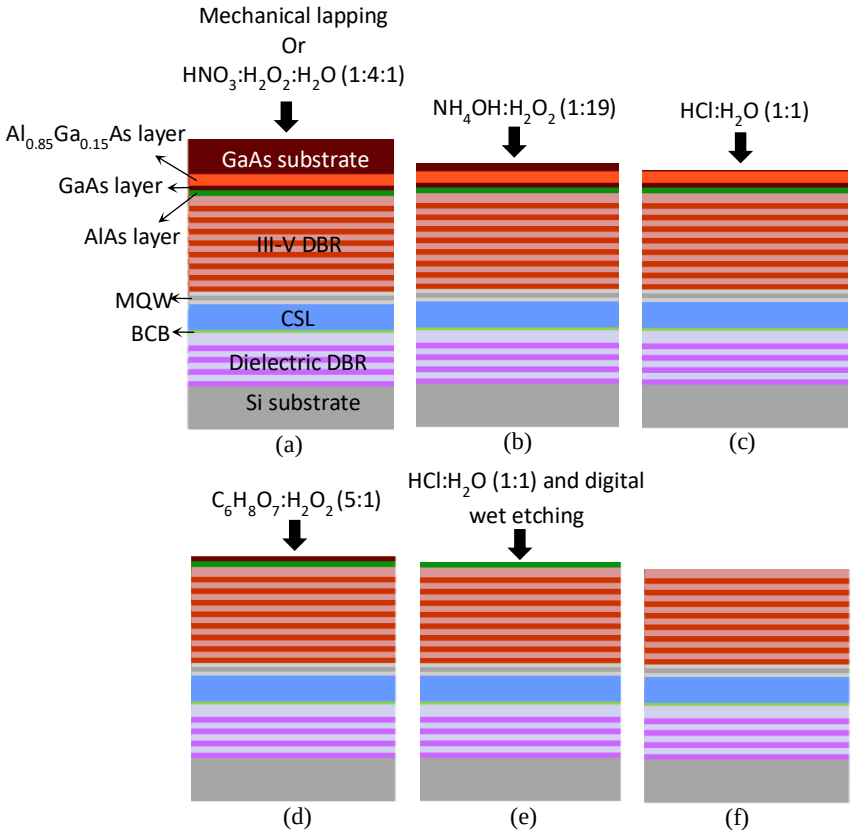


Fig 5.11 Schematic process flow for the removal of the GaAs substrate: (a) mechanical grinding or non-selective etching in HNO_3:H_2O_2:H_2O, (b) etch the remainder of the GaAs substrate in NH_4OH:H_2O, (c) etching of $Al_{0.85}Ga_{0.15}As$ in HCl:H_2O, (d) etching of GaAs in $C_6H_8O_7$:H_2O_2:H_2O, (e) etching of AlAs in HCl:H_2O and digital wet etching, and (f) final bonded sample.

5.3.4.1 Mechanical substrate removal process

To shorten the process time, most of the substrate can be removed mechanically in a process called lapping or mechanical grinding and the rest of the substrate is then removed by selective wet etching. For the mechanical substrate removal process, the sample is temporarily glued to a smaller glass plate using a wax, which melts at ~70 °C. Care should be taken to get a uniform contact between the

sample and the glass plate when gluing the sample as usage of an excess amount of glue can result in a thickness variation. The glass plate with the sample glued on is then mounted on a glass grinding plate. A controlled downward force on the sample can be applied by a pressure head and an abrasive slurry containing a very fine powder, i.e., Aluminium oxide powder (12.5 μm diameter) mixed with water is used. The slurry is fed continuously onto the grinding plate for homogenous abrasion. It is recommended to not lap the substrate to less than ~200 μm thickness in order to not crack the sample. The cracks are mostly caused by any small particles trapped between the bonding interfaces, non-optimum force and the rotation speed of the grinder (too high force and too fast rotation speed). After removing the majority of the GaAs substrate by mechanical grinding, the rest of the sacrificial layers are etched by carrying out the etch steps of Fig 5.11 (b)-(f).

It is also possible to skip this process step altogether and just perform wet etching if a high yield is more important than short process time. However, the wet etchant used for complete substrate removal needs to be selective and have a high etch rate. A process of complete wet etching to remove the GaAs substrate is presented in the next section.

5.3.4.2 Complete wet etch substrate removal process

There is also a possibility to perform complete wet etching of the GaAs substrate by choosing two wet etchants. The 1st etchant needs to have a high etch rate to reduce the substrate removal time and the 2nd etchant needs to be selective and can be introduced at the end to remove the GaAs substrate selectively. Even though the etching of the GaAs substrate in an ammonia-based solution is fast (~3.5 μm/min) and selective, it cannot be used in the 1st step of a complete wet etching process for substrate removal as etching in ammonia is not linear over time and the etching becomes very slow with time. Therefore a non-selective etching was chosen to remove the GaAs substrate. A Nitric acid-based etchant can be used for fast removal of the GaAs substrate until 40-50 μm of GaAs substrate is left. It is reported that the etch rate of GaAs in HNO_3: H_2O_2:H_2O (1:*x*:1) solution depends on *x* (H_2O_2 concentration) used in the solution [32]. The etch rate of the GaAs substrate increases first and then decreases with the amount of H_2O_2 increasing. When the ratio of HNO_3:H_2O_2:H_2O is 1:6:1, the etch rate reaches its maximum, which is ~8.024 μm/min. When the ratio of HNO_3:H_2O_2:H_2O is 1:4:1, the etch rate is ~5 μm/min and the smoothest morphology with a roughness of about 4.57 nm was observed. We choose HNO_3:H_2O_2:H_2O with ratio 1:4:1 due to the high etch rate and smoother etching surface. The advantages of Nitric acid-based etchants are that it is easy, repeatable, and gives no contamination. The only disadvantage of Nitric acid-based etchants is that the etching of the GaAs substrate starts from one edge of the sample and it finishes at another edge, giving ~20-30 μm of non-uniformity between one edge to another edge of the sample.

The origin of this non-uniformity is not well understood. However, this is not a serious problem as the Ammonia based solution has very high selectivity and we can etch the rest of the GaAs substrate in it until the etch stop is reached. Hence we need to etch the substrate in HNO_3:H_2O_2:H_2O (1:4:1) solution for ~140 minutes and that should leave ~50 µm of substrate.

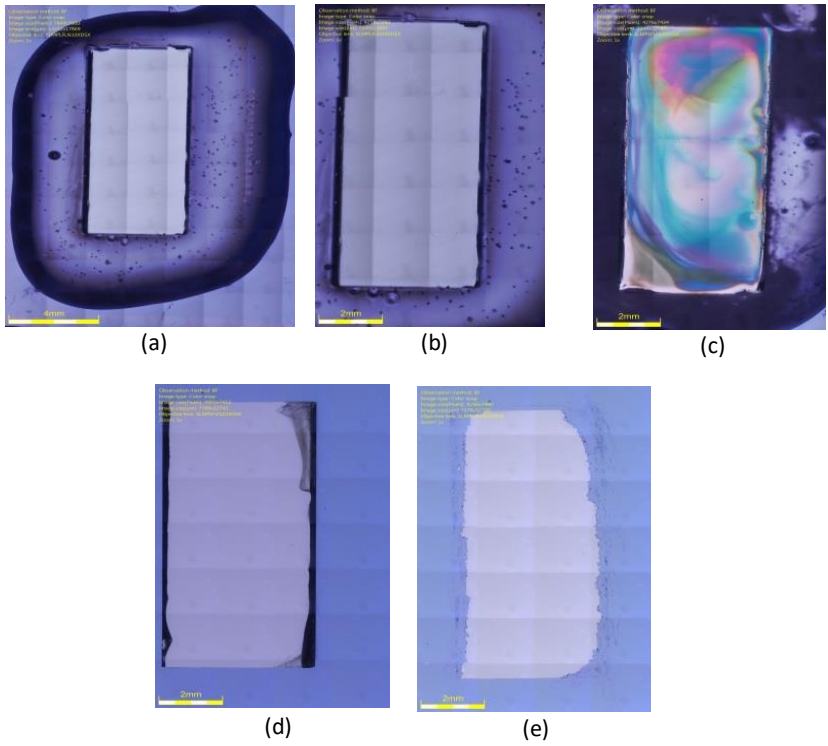
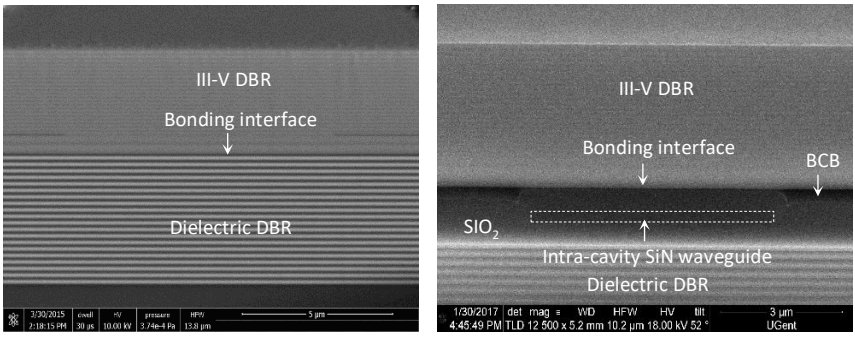


Fig. 5.12 Microscope image of the surface after (a) applying the CrystalBond 509 wax around edge of the bonded III-V die; (b) mechanical grinding or non-selective etching in HNO_3:H_2O_2:H_2O; (c) etching the rest of the GaAs substrate in a selective etching solution (NH_4OH:H_2O); (d) etching the rest of the sacrificial layers followed by digital wet etching; (e) final bonded surface after scratching the ears using a scalpel.

While doing the fast etching of the GaAs substrate in a Nitric acid based etchant, monitoring of the thickness of the substrate left is required towards the end, 30 minutes before the expected end time. As the non-uniformity induced by the wet substrate removal and the thickness of the substrate that we want to leave is similar, this step is crucial because the Nitric acid-based etch is not selective. After the etching of the substrate in Nitric acid is finished, the sample needs to be cleaned in DI water thoroughly for at least 1 minute in order to prevent mixing of

etchants in the next step. After cleaning the sample in DI water, the remaining GaAs substrate is removed by selective wet etching in $NH_4OH:H_2O_2$ (1:1) solution. To maintain the etch rate the etching solution was continuously agitated throughout the etching process. Once the $Al_{0.85}Ga_{0.15}As$ layer is exposed in ammonia solution, the etching stops due to the oxidation of the $Al_{0.85}Ga_{0.15}As$ layer. Since the nitric acid etch gives nonuniformity in the substrate removal, a rainbow pattern can be seen on the surface (Fig 5.12 (c)). The rest of the sacrificial layers are then etched by repeating the etch steps in Fig 5.11 (c)-(f). As can be seen from Fig 5.12 (d), the bulk GaAs stays at the edge of the bonded III-V forming ears during the substrate removal. These ears can affect the optical lithography in subsequent steps during VCSEL fabrication. Therefore, they are removed with a scalpel (Fig 5.12 (e)). Before scratching the GaAs ears, a thick photoresist was spin coated on the sample to avoid the contamination of the bonded III-V layer with particles from scratching. Fig 5.13 shows the SEM image of the FIB cross section of a Gen1 and Gen2 bonded sample.



(a) (b)

Fig. 5.13 SEM images of a FIB cross-section of (a) a bonded Gen1 VCSEL sample and (b) a bonded Gen2 VCSIL sample

5.4 VCSEL fabrication

After the bonding of the GaAs-based "half-VCSEL" structure to the dielectric DBR on Si using DVS-BCB and removal of the GaAs substrate, VCSELs were fabricated using a range of standard VCSEL processing steps, including photolithography, thin film deposition, metallization, etching, and wet oxidation [33,34]. These processes were carried out at Chalmers University of Technology, as part of the PhD work of E. P. Haglund [34].

5.4.1 Gen1: VCSEL fabrication

The fabrication process for hybrid-cavity Gen1 VCSELs is illustrated in Fig. 5.14 and the different steps in VCSEL fabrication are explained as below:

5.4.1.1 p-contact metallization

The bonded sample is cleaned in acetone, IPA, and DI water and 2 min O_2 plasma, followed by a 30sec dip in HCl:H_2O (1:1). As a first step, the alignment marks and top p-contact rings were patterned using optical lithography. The metal contacts (Ti/Pt/Au) (10 nm/10 nm/175 nm) were deposited by electron-beam evaporation. A lift-off procedure is performed after the metallization by dipping the sample in acetone, after which the sample is rinsed and dried.

5.4.1.2 Island definition

In order to isolate the individual VCSEL devices, rectangular islands of bonded III-V were defined by making trenches in the III-V using optical lithography. The epitaxial III-V was etched using ICP-RIE with $SiCl_4$ and Ar chemistry. These trenches allowed residual gas trapped in the bonding layer to escape during subsequent high-temperature process steps (oxidation and annealing).

5.4.1.3 Mesa definition

A 300 nm thick blanket SiN layer was deposited by sputtering on the entire chip to act as a hard mask for etching the mesa. Circular mesas with diameters of 22, 24, 26, and 28 μm were defined by photolithography and the pattern was first transferred to the SiN hard mask by a dry etch of the SiN using an NF_3 chemistry, followed by etching the III-V mesas using ICP-RIE with $SiCl_4$ and Ar chemistry. While etching the mesa, an *in-situ* laser interferometer endpoint detection system was used to accurately stop within the thin (~280 nm) intra-cavity $Al_{0.12}Ga_{0.88}As$ n-contact layer just below the active region and to expose the $Al_{0.98}Ga_{0.02}As$ layer for oxidation.

5.4.1.4 Wet oxidation

Selective wet oxidation of high aluminium-content $Al_xGa_{(1-x)}As$ is used to form the VCSEL oxide aperture. The surface of the mesas and the contact layer were protected during oxidation by a 100 nm thick SiN layer deposited by plasma-enhanced chemical vapor deposition. The SiN layer was removed at the mesa sidewalls using photolithography and ICP-RIE etching with NF_3 chemistry to expose the $Al_{0.98}Ga_{0.02}As$ layer for oxidation. The wet oxidation is performed by exposing the high aluminium-content $Al_{0.98}Ga_{0.02}As$ layer to water vapour at elevated temperature [35]. The sample was transferred to an oxidation furnace

held at 420°C. Using a N_2-bubbler the water vapour from a water beaker held at 95°C is transported to the oxidation furnace, achieving a typical oxidation rate of ~0.3 μm/min for $Al_{0.98}Ga_{0.02}As$. The progress of the wet oxidation is monitored *in-situ* using IR illumination under a microscope with a CCD camera. Since the oxidation rate is very sensitive to the temperature, even a small temperature gradient across the sample is enough for the oxide aperture diameter to become non-uniform [35]. To improve the uniformity, the sample was rotated 180° after half of the oxidation. Depending on the mesa diameters, oxide aperture diameters from 4 to 10 μm were obtained.

5.4.1.5 n-contact metallization

After wet oxidation, the SiN layer is again removed in ICP-RIE using NF3 chemistry. An optical lithography step was performed to define the n-contact pattern. The sample was then dipped in $HCl:H_2O_2$ (1:1) for 30 sec to remove any native oxide on AlGaAs. A thin film of metal (Ni/Ge/Au) (20 nm/52 nm/100 nm) was deposited using electron beam evaporation, see Figs. 4.2 (d). Germanium is included in the composition of the n-metal contact because the intra-cavity n-contact layer is not sufficiently doped to allow for ohmic contacting without additional doping. In the subsequent rapid thermal annealing at 430°C in an N_2 atmosphere for 30 sec, Ge alloys with the contact layer, thereby heavily doping it and generating ohmic contacts.

5.4.1.6 Passivation

After the n-type metallization, the passivation is performed. This is realized by spin coating a thick protective layer of DVS-BCB on the sample. This layer later provides an electric insulation between the p-contact on the top and the n-electrodes located below. For this purpose, a photosensitive DVS-BCB 4026-46 resin is spin-coated on the sample.

5.4.1.7 Bondpads

The photosensitive DVS-BCB enables opening up of the DVS-BCB by photolithography. After defining the bondpads on the DVS-BCB layer in a GSG configuration through photolithography, the last process step is to deposit Ti/Au bondpads through sputtering and lift-off to allow for probing and evaluation of the devices.

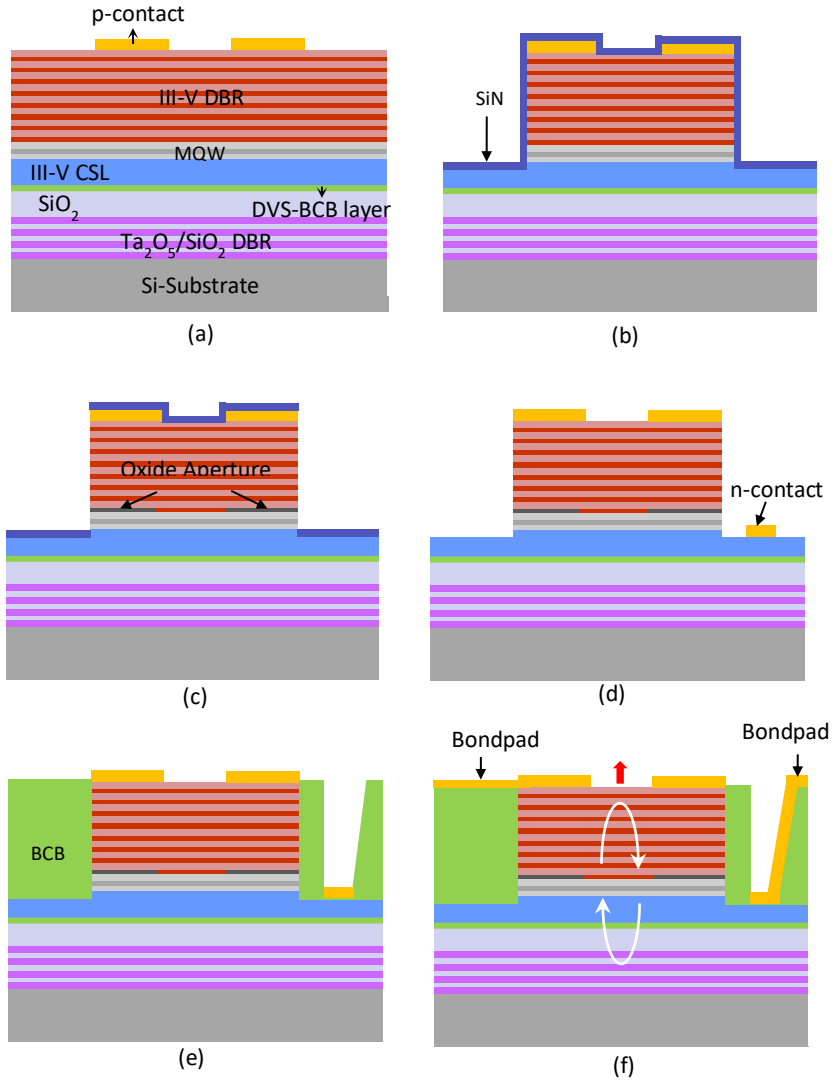
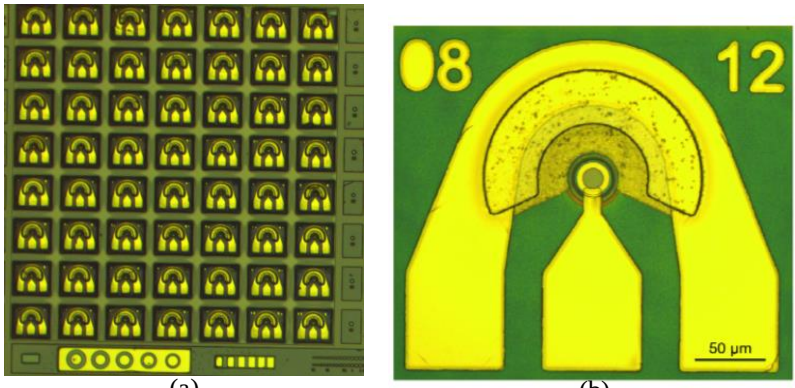


Fig. 5.14 The process steps for hybrid-cavity GEN1 VCSEL fabrication includes: (a) p-contact deposition, (b) mesa etching followed by deposition of SiN, (c) oxide aperture formation after opening of SiN on mesa side walls, (d) n-contact deposition, (e) planarization with DVS-BCB, and (f) deposition of bondpads.



(a) (b)

Fig. 5.15 Optical micrographs of (a) an array of fully processed VCSELs and (b) a single VCSEL.

The top GaAs p-contact layer has a thickness of λ/2, thereby producing an anti-phase reflection at the surface to facilitate post process tuning of the photon lifetime. Therefore, after initial characterization of the VCSEL, the top GaAs surface of the VCSEL can be etched by low power Ar ion milling to investigate the dependence of VCSEL performance on the top DBR reflectivity [36]. The optical micrograph image of an array of fully processed Gen1 VCSELs and a single Gen1 VCSEL is shown in Fig. 5.15

5.4.2 Gen2: VCSIL fabrication

The fabrication process for Si-integrated hybrid-cavity Gen2 VCSILs has a similar fabrication process as Gen1 VCSELs and is illustrated in Fig. 5.16. The only difference is in defining the top contact and the III-V mesas: direct laser writing is used instead of the optical lithography in this case. This improved the alignment of the VCSIL relative to the intra-cavity grating underneath. Any remaining $Al_xGa_{(1-x)}As$ material on top of the waveguides was also removed outside the device structure to reduce the power leakage from the waveguide to the higher refractive index $Al_xGa_{(1-x)}As$ material. As can be seen from Fig 5.16(e), the device fabricated at this step still act as surface emitting device and allowed us to characterize the surface emitting output of the VCSEL. The surface-emission was then suppressed by depositing 100 nm thick gold by electron beam evaporation on top of the III-V mesas (Fig 5.16(f)). The optical micrograph of an array of fully processed Gen2 VCSILs and a single Gen2 VCSIL is shown in Fig. 5.17.

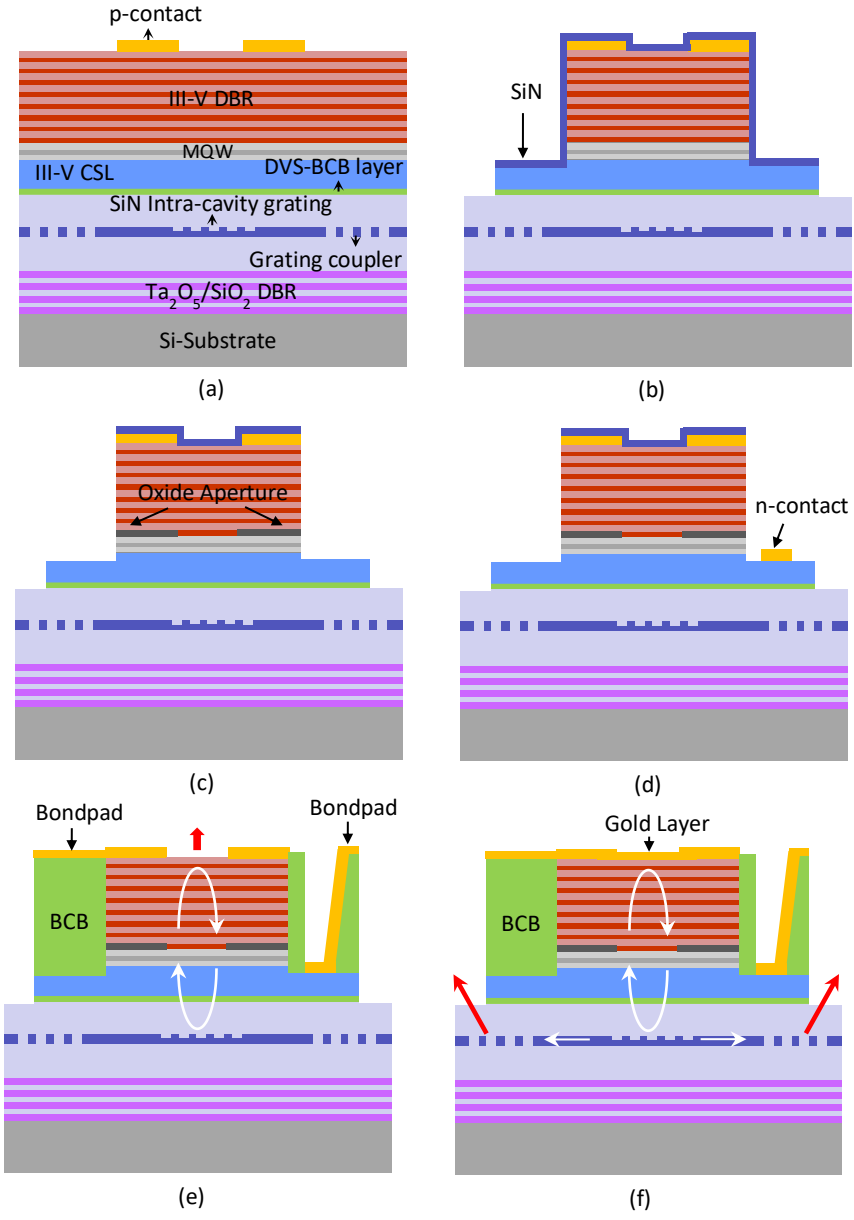
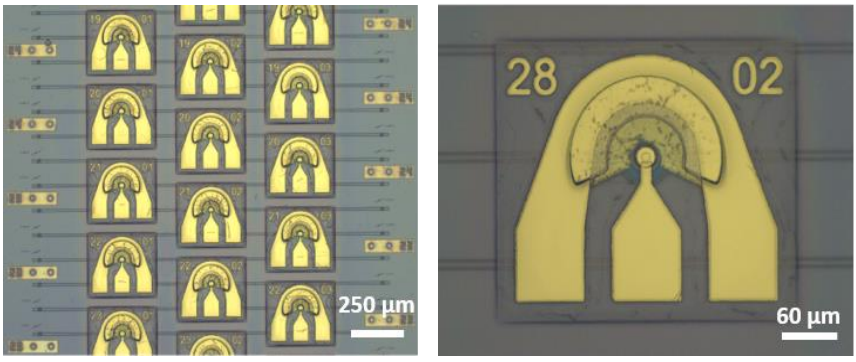


Fig. 5.16 The process steps for hybrid-cavity Gen2 VCSIL fabrication include: (a) p-contact deposition, (b) mesa etching followed by deposition of SiN, (c) oxide aperture formation after opening of SiN on the mesa sidewalls, (d) n-contact deposition, (e) planarization with DVS-BCB, and deposition of bondpads and (f) deposition of a gold reflector



(a) (b)

Fig. 5.17 Optical micrographs of (a) an array of fully processed Gen2 VCSILs and (b) a single Gen2 VCSIL.

5.5 Conclusion

In summary, several etchants were investigated for selective etching of GaAs over AlAs and vice versa. An optimal wet chemical selective etching process was developed to achieve a reproducible high-quality surface. This ensured high yield in the adhesive bonding process. After bonding, the process to fabricate Gen1 VCSELs and Gen2 VCSILs is also presented.

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6

Characterization of Si-Integrated Hybrid cavity VCSELs

6.1 Introduction

In the previous chapters, we discussed the design and technologies to realize Si-integrated VCSELs. In this chapter, the optical characteristics of these integrated VCSELs will be presented. Static measurements will be presented for Gen1 VCSELs and Gen2 VCSILs. The impact of the DVS-BCB thickness on the static and dynamic performance of Gen1 VCSELs will also be presented. These measurements were carried out at the Chalmers University of Technology, as part of the PhD work of E. Haglund. Finally, in the last section of this chapter, a conclusion will be provided.

6.2 Gen1 HC-VCSEL

As discussed before, the Gen1 HC-VCSEL consists of a GaAs half VCSEL attached to a dielectric DBR on Si, resulting in a surface emitting laser. The static light-current-voltage (LIV) characteristics of these devices are measured using a low noise current source and a large area Si photodetector. A Peltier element and a thermistor are attached to the VCSEL submount to enable measurements at elevated temperature.

6.2.1 Static performance

The first batch of lasers were fabricated after etching the GaAs and AlAs sacrificial layers on the III-V layer stack in citric acid and 2% HF respectively. Since there was no digital etching performed at this stage, a very thin layer of GaAs (~4nm) is still left inside the cavity. The LIV characteristics under continuous wave operation of VCSELs with oxide aperture diameters of 7 µm, measured at 25°C, can be seen in Fig 6.1. As can be seen from Fig 6.1, this device showed almost no lasing behavior and the output power of the VCSEL is very low due to optical band-to-band absorption in the thin GaAs layer and scattering/absorption by residues left inside the laser cavity after sacrificial layer removal.

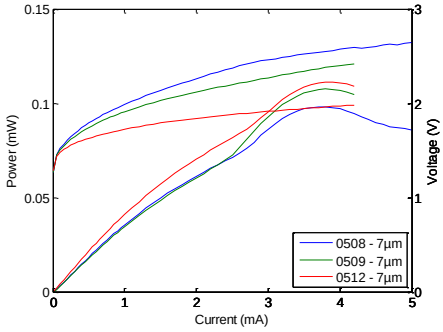

Fig. 6.1 Measured light-current-voltage characteristics for hybrid-cavity VCSELs with oxide aperture diameter of 7 µm.

In the next batch of devices, 3 cycles of digital etching were performed. As discussed in chapter 5, the digital etch ensured removal of residues from the sacrificial layer removal as well as it etches away the 4 nm thin GaAs layer in a very controlled way. The LIV characteristics of such VCSELs under continuous operation with oxide aperture diameters ranging from 3-9 µm, measured at 25°C, can be seen in Fig 6.2. The impact of this digital etching step is clearly seen by a significant improvement in the output power of the VCSEL. The VCSELs with the smallest and largest oxide aperture exhibit threshold currents of 0.3 and 1.2 mA, respectively. The maximum output power is 1.6 mW at 6.0 mA bias current for the 9 µm VCSEL, mainly limited by thermal effects.

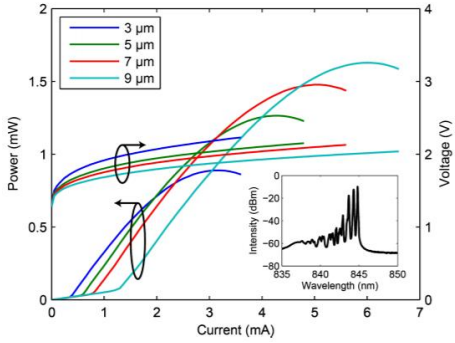

Fig. 6.2 Measured light-current-voltage characteristics for hybrid-cavity VCSELs with oxide aperture diameters of 3–9 µm. Inset: spectrum for a 7 µm aperture VCSEL operated at 3.0 mA. Reproduced from [1]

The slope efficiency is 0.5 W/A for all aperture sizes. The differential resistance ranges from 50 Ω for a 9 µm aperture VCSEL to 120 Ω for a 3 µm aperture VCSEL which is lower than the typical values for oxide-confined VCSELs [2] with same aperture size due to the intra-cavity contact. The emission spectrum for a 7 µm aperture device operated at 3.0 mA is included as an inset to Fig. 6.2, showing multiple transverse modes lasing around 844 nm.

6.2.2 Impact of BCB bonding thickness on VCSEL performance

As discussed in Chapter 3, the cavity resonance wavelength of a heterogeneously integrated VCSEL can be adjusted by the DVS-BCB layer thickness used for adhesive bonding. In a VCSEL cavity, as temperature increases both the cavity resonance and the laser gain peak shift to longer wavelength with a rate of 0.06–0.09 nm/K and 0.32nm/K respectively [3]. A degradation in laser performance is expected when the cavity resonance wavelength is not properly aligned with the gain peak wavelength. Therefore, we can adjust the DVS-BCB thickness to align the cavity resonance and the laser gain peak wavelength in such a way that, either a low threshold/high output power can be obtained at a particular temperature or a relatively invariant threshold properties over a wide range of operating temperatures can be produced. Below we will elaborate on the impact of the DVS-BCB thickness on the static and dynamic performance of Gen1 VCSELs.

6.2.2.1 Static performance

To study the impact of the bonding thickness on the VCSEL performance, 4 batches of HC-VCSELs denoted as A–D with an interface thickness of 35, 65, 125, and 180 nm and cavity resonance wavelengths of 843, 853, 861, and 867 nm,

corresponding to a gain-to-resonance detuning of approximately +9, −1, −9, and −15 nm, respectively are prepared. The diameter of the oxide aperture is 10 µm. The resonance wavelengths are extracted from optical emission spectra of HC-VCSELs biased below the threshold at 25 °C. The output power and voltage-versus-current measured at ambient temperatures ranging from 15 to 100 °C, in steps of 5°C, are shown in Fig. 6.3, while the corresponding static performance characteristics are summarized in Table 6.1.

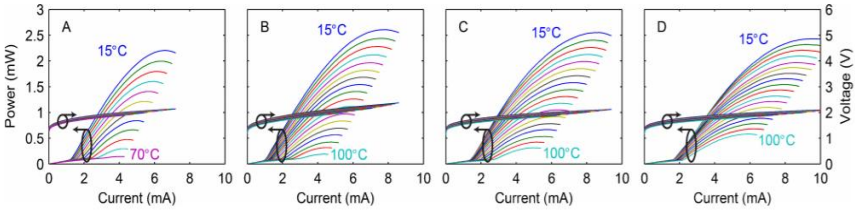

Fig. 6.3 Output power and voltage versus current for HC-VCSELs A–D measured at ambient temperatures ranging from 15 to 100 °C in steps of 5 °C, reproduced from [4].

As can be seen from Fig 6.3, the HC-VCSEL B, providing the smallest gain-to-resonance detuning (-1 nm) at 25°C has a minimum threshold current (1.1 mA). At higher ambient temperatures, HC-VCSELs C and D have lower threshold currents since the detuning is reduced with temperature as a result of the ~4 times faster redshift of the gain peak with respect to the cavity resonance [3]. The threshold currents for different VCSELs as a function of ambient temperature is extracted from Fig. 6.3 and is plotted in Fig. 6.4(a). The temperatures for minimum threshold current were identified by fitting a second order polynomial to the dependence of threshold current on temperature, as seen in Fig. 6.4(b).

At the temperature for minimum threshold current, the wavelengths of the cavity resonance and the gain peak are aligned. At 25°C this occurs at 852 nm. While the threshold current of HC-VCSEL D is higher than that of HC-VCSEL B at 25°C, it is lower at high temperatures and shows a weaker dependence on temperature.

The achievable output power depends on the threshold current, the slope efficiency and the thermal roll-over current. All HC-VCSELs have similar slope efficiency (~0.5 W/A at 25 °C), with a slight variation due to uncertainty in the thickness of the top layer of the p-DBR. At high temperature, reduction in slope efficiency is observed as a result of increased internal optical loss (free carrier absorption) and reduced internal quantum efficiency [5].

Table 6.1. Static performance parameters, reproduced from [4].

Parameter	Temp. (°C)	HC-VCSEL			
		A	**B**	**C**	**D**
Resonance wavelength (nm)	25	843	853	861	867
Peak gain-to-resonance detuning (nm)	25	+9	−1	−9	−15
Temperature at min. threshold current (°C)		6	27	36	54
Threshold current (mA)	25	1.42	1.07	1.42	1.85
	55	2.18	1.36	1.52	1.64
	85	n/a	2.10	2.08	1.87
	100	n/a	3.00	2.77	2.24
Maximum optical output power (mW)	25	1.8	2.3	2.3	2.2
	55	0.66	1.4	1.4	1.5
	85	n/a	0.56	0.67	0.89
	100	n/a	0.19	0.31	0.58
Thermal roll-over current (mA)	25	6.2	7.4	8.2	9.0
	55	4.8	6.2	7.1	7.9
	85	n/a	5.0	5.7	6.6
	100	n/a	4.3	5.0	5.9
Slope efficiency (W/A)	25	0.54	0.55	0.54	0.50
	55	0.30	0.42	0.41	0.39
	85	n/a	0.25	0.26	0.28
	100	n/a	0.09	0.16	0.22
Differential resistance at 4 mA (Ω)	25	61	81	55	51
	55	62	79	54	50
	85	n/a	79	55	50
	100	n/a	81	55	51
Differential resistance at thermal roll-over (Ω)	25	48	61	33	28
	55	60	67	41	34
	85	n/a	76	48	42
	100	n/a	81	53	45

The thermal roll-over current is largely determined by the thermal impedance and the dependence of threshold current on temperature.

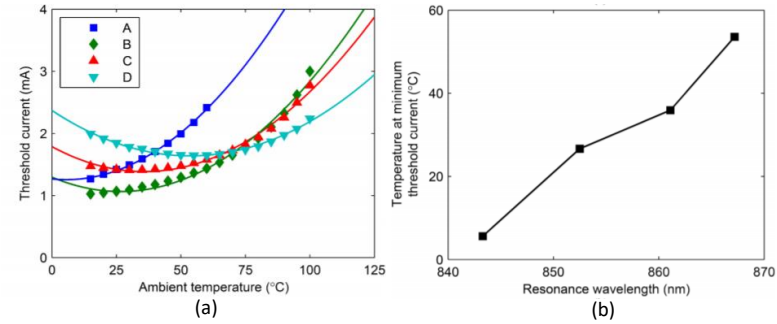

Fig. 6.4 (a) Threshold current versus ambient temperature and (b) estimated temperature at minimum threshold current versus resonance wavelength, reproduced from [4].

The thermal impedance was deduced by tracking the red shift of the fundamental mode as a function of stage temperature and dissipated power. The fundamental mode redshifts with temperature by 0.059 nm/K, while it redshifts with dissipated power by 0.42 nm/mW (Fig. 6.5). This gives a thermal impedance of 7 K/mW for all HC-VCSELs, regardless of the thickness of the bonding interface. This indicates that the thermal impedance is to a large extent determined by heat transport through the dielectric DBR. With the thermal impedance being ~4 times larger than for ordinary GaAs-based oxide-confined VCSELs [5], the thermal roll-over currents are relatively low, which limits the maximum output power. Therefore, while HC-VCSEL B and C produce the highest output power at 25 °C (2.3 mW), HC-VCSEL D shows improved high temperature and high current performance since the gain peak aligns with the resonance wavelength at higher internal temperature. The maximum output power at 100 °C is 0.6 mW. The rapid increase of threshold current with temperature for HC-VCSEL A limits the maximum operating temperature to 70 °C.

The differential resistances are comparable (50–60 Ω), with negligible dependence on temperature, since the bonding interface thickness should have no impact on the electrical characteristics. The somewhat higher resistance of HC-VCSEL B (80 Ω) is believed to be due to residues from the removal of the substrate, which led to a higher p-contact resistance. The performance of HC-VCSEL B is still superior in terms of maximum output power at temperatures up to 25°C. Optical emission spectra, measured at a bias current of 2 mA, are shown in Fig. 6.6.

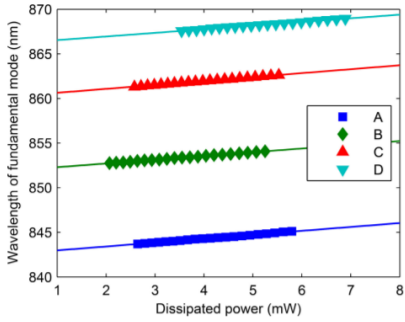

Fig. 6.5 (a) Wavelength of the fundamental mode versus dissipated power at 25 °C for HC-VCSELs A–D with fits to extract the thermal impedance, reproduced from [4].

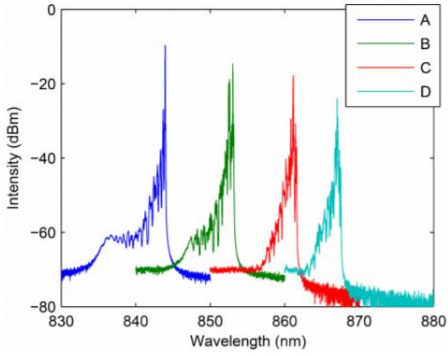

Fig. 6.6 Emission spectra at 25 °C for HC-VCSELs A–D biased at 2 mA, reproduced from [4].

6.2.2.2 Dynamic performance

6.2.2.2.1 Small signal modulation response

A first indicator of high-speed performance is to measure the small signal frequency response (*S*21) of the VCSEL using a network analyzer. From this measurement, f_{3dB}, f_r, γ, and f_p and their respective dependencies on bias current can be extracted through curve-fitting equation 2.14 to the measured data and conclusions can be made about which parameters are limiting the dynamic performance. It is in principle possible to attain both phase and magnitude of the modulation response if the system is calibrated accordingly. However, only magnitude information of the detector frequency response is typically available in the product calibration sheet and even though phase response information in

principle can be extracted from this data [6], we measure only the magnitude of the frequency response (|*S*21|) as it requires less calibration and still provides much information (|*S*21(*f*)| = |*H*(*f*)| from equation 2.14).

Fig. 6.7 shows a schematic of the setup used to measure the modulation response. The bias current is combined with the sinusoidal small signal modulation signal from port 1 of the 20GHz vector network analyzer (VNA-Agilent N5230A) through a high frequency bias-T and fed to the VCSEL by a high-speed RF probe (Picoprobe 40A-GSG-100-P from GGB Industries). The design of the VCSEL bondpad is such that it is matched with the 100 μm pitch of the ground-signal-ground configured probe. A Peltier element and a thermistor are attached to the VCSEL submount to enable measurements at elevated temperatures. The modulated light is coupled to a short (1m long) 50 μm multimode fiber (OM4) via an AR coated lens system that matches the numerical aperture of the VCSEL with that of the fiber. This coupling system results in >60% coupling efficiency and minimizes optical feedback to the laser. The fiber is connected to the 28 GHz (Picometrix DG-32xr-FC) photodetector which in turn is connected to port 2 of the network analyzer. If the fiber-coupled output power is high, a variable optical attenuator (VOA) is included to keep the photodetector from saturating. A calibration is made to remove any influence from attenuation in the cables and the bias-T prior to the measurement. The measured data is corrected for the response of the RF probe and detector (with data obtained from the calibration sheets provided with the respective equipment) before the transfer function (equation 2.14) is fitted to the response. From the fit, the *K*- and *D*-factors can be extracted.

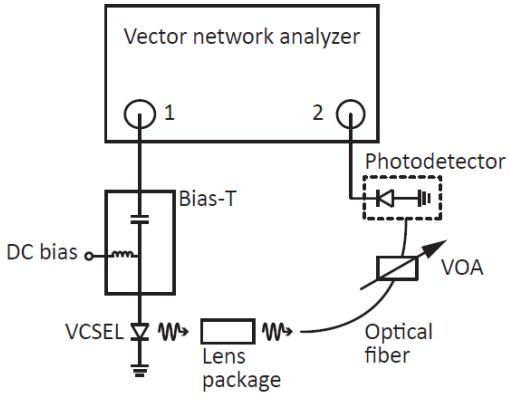

Fig. 6.7. Measurement setup for the small signal modulation response.

The modulation response for HC-VCSELs A–D at 25 and 85 °C, compensated for the frequency response of the probe and the photodetector, are shown in Fig. 6.8. The dynamic performance characteristics of all HC-VCSELs at three ambient temperatures (25°C, 55°C, and 85°C) are summarized in Table 6.2.

Table 6.2. Dynamic performance parameters, reproduced from [4].

Parameter	Temp. (°C)	HC-VCSEL			
		A	B	C	D
Maximum 3 dB bandwidth (GHz)	25	8.2	10.0	9.7	9.5
	55	4.3	8.1	8.1	8.1
	85	n/a	5.2	5.6	6.4
Bias current at max. 3 dB bandwidth (mA)	25	5.2	7.1	7.9	9.0
	55	4.4	5.8	6.9	7.1
	85	n/a	4.9	5.0	6.2
D-factor (GHz/mA$^{1/2}$)	25	4.8	4.2	3.3	3.0
	55	2.8	4.2	3.3	2.9
	85	n/a	3.1	2.6	2.7

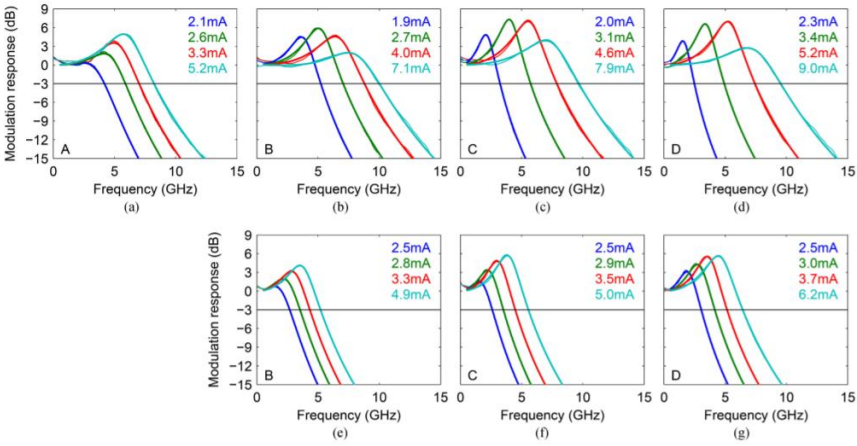

Fig. 6.8. Small-signal modulation response at 25 °C (a)-(d) and 85 °C (e)-(g) for HC-VCSELs A-D at indicated bias currents. The maximum 3 dB modulation bandwidth is reached at the highest bias currents indicated. Reproduced from [4].

All HC-VCSELs show a strongly resonant modulation response caused by the relatively low photon density established in the cavity at thermal roll-over. A more damped response is desired to reduce overshoot and jitter during large signal modulation and data transmission [7]. Although the modulation bandwidth is largely limited by the capacitance over the single oxide layer (with a parasitic pole frequency of 6–8 GHz), there are clear differences in the maximum modulation bandwidth related to the differences in bonding interface thickness and gain-to-resonance detuning. The maximum modulation bandwidth depends on how fast the resonance frequency increases with bias current (quantified by the D-factor) and the highest photon density that can be achieved [8].

The D-factors were extracted from the measured dependence of the resonance frequency on the square root of current above threshold (Equation 2.16), as shown in Fig. 6.9(a) at 25 °C. The D-factors are plotted in Fig. 6.9(b). Clearly, the D-factor is reduced with increasing resonance wavelength. This is caused by the differential gain being lower on the long-wavelength side of the gain peak. At higher temperatures (Table 6.2), the D-factors are further reduced due to a reduction of differential gain with temperature and a more pronounced reduction of internal quantum efficiency at the highest temperature.

The maximum photon density is reached at the thermal rollover current. Therefore, higher photon densities can be established in HC-VCSELs with low threshold current and weak dependence of threshold current on temperature.

As a consequence of these dependencies, HC-VCSEL B has the highest 3 dB modulation bandwidth at 25 °C (10.0 GHz) while HC-VCSEL D has the highest bandwidth at 85 °C (6.4 GHz). HC-VCSEL D also shows the smallest dependence of bandwidth on temperature.

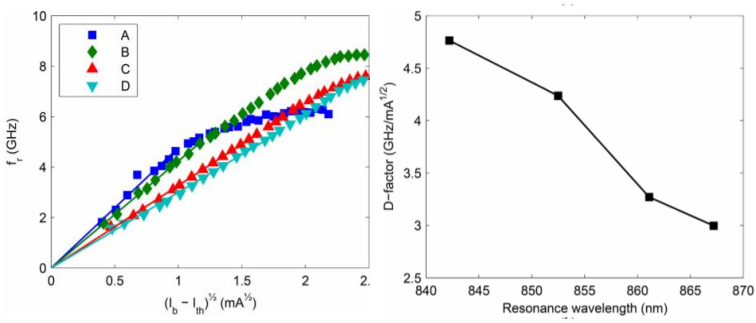

Fig. 6.9 Resonance frequency versus square root of current above the threshold at 25 °C with fits to extract the D-factors, which are shown versus resonance wavelength in (b). Reproduced from [4].

6.2.2.2.2 Large signal data transmission

By setting a VCSEL in either it's on- or off-state, the simplest modulation format of ones and zeros can be represented. This binary modulation format is called on-off keying (OOK).

The schematic of the setup used to measure large signal data transmission is shown in Fig. 6.10. To perform large signal data transmission experiments, an OOK signal consisting of a pseudo-random bit sequence (PRBS) signal with word length 2^7-1 is generated by a bit pattern generator (SHF 12103A) and is fed to the VCSEL through a bias-T and a GSG probe after amplification. The light from the HC-VCSEL is coupled into a 1 m long OM4 multimode fiber using the AR coated lens package. The fiber is then connected to a 30 GHz limiting photoreceiver (VI Systems R40- 850) through a VOA. The electrical signal from the photoreceiver is connected to either an error analyzer (SHF 11100B) (Path A in Fig 6.10) synchronized with the pattern generator to count the number of errors in the received signal or a 70 GHz equivalent time sampling oscilloscope (Agilent Infiniium DCA-J 86100C) (Path B in Fig 6.10) to record eye diagrams (an overlay of the signal waveform). By relating the number of errors to the total number of bits the bit error ratio (BER) can be calculated. For very low BERs the time needed to accumulate errors is very long. For reasonable measurements times, it is, therefore, necessary to use statistical methods. It is required that N_{bits} are detected without any error to ensure a BER below p with a statistical confidence c, where N_{bits} is given by [9]

$$N_{bits} = -\frac{\ln(1-c)}{p} \tag{6.1}$$

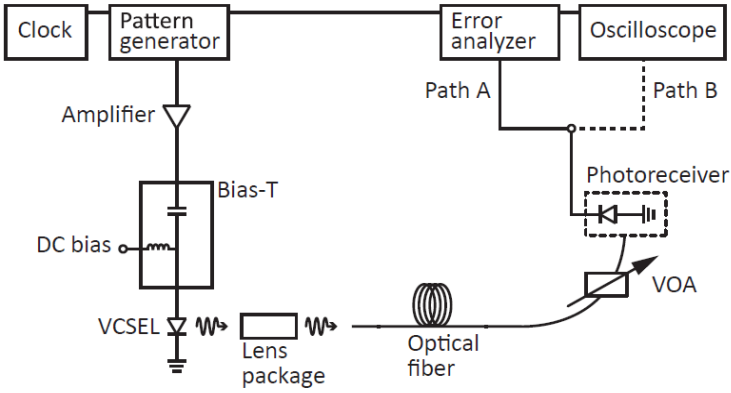

Fig. 6.10. Large signal data transmission setup. Path A is used to measure BERs, while path B is used to record eye diagrams.

A HC-VCSEL with similar resonance wavelength (859 nm) as HC-VCSEL C, but with a smaller oxide aperture diameter (5 µm), was chosen for back-to-back data transmission experiments. The smaller aperture device has a slightly more damped modulation response and a higher photon density at low bias currents. The small signal 3 dB modulation bandwidth for this device is 12.1 and 8.9 GHz at 25 and 85 °C, respectively. With a bias current of 4.5 mA, a modulation voltage of 350 mV_{pp}, and the HC-VCSEL held at 25 °C, error-free transmission (BER < 10^{-12}) was achieved at data rates up to 25 Gbit/s with an extinction ratio (ER) of 5.6 dB (Fig. 6.11). At 85 °C, a bias current of 3.5 mA and modulation voltage of 180 mV_{pp} enabled error-free transmission at data rates up to 10 Gbit/s (ER = 5.9 dB).

The lower bias current and modulation voltage used at 85 °C were required to maintain high modulation efficiency and avoid the operation below threshold at the off-state. The same biasing and modulation conditions were also used with the HC-VCSEL held at 25 °C and modulated at 10 Gbit/s for comparison, resulting in a reduction of the ER to 3.9 dB due to the lower threshold current. At 10 Gbit/s, there is no power penalty when increasing the temperature from 25 to 85 °C due to the higher ER at 85 °C, but the power budget is 2.3 dB larger at 25 °C. However, increasing the data rate from 10 to 25 Gbit/s at 25 °C results in a 4 dB power penalty.

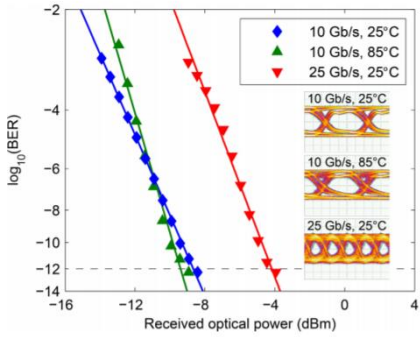

Fig. 6.11. Measured BER versus received optical power for a 5-µm oxide aperture diameter HC-VCSEL with similar resonance wavelength as HC-VCSEL C at data rates up to 25 Gbit/s at 25 °C and 10 Gbit/s at 85 °C. Insets: Corresponding optical eye diagrams (scales: 100 mV/div and 20 ps/div). Reproduced from [4].

6.3 Gen2 HC-VCSIL

As discussed before, a Gen2 HC-VCSIL is a modified version of the Gen1 VCSEL with a shallow etched grating incorporated inside the cavity to tap off the output to the SiN waveguide. As discussed above, a VCSEL with a resonance wavelength of 852 nm corresponding to a gain-to-resonance detuning of -1 nm has superior performance at room temperature. Therefore, Gen2 VCSIL devices to operate around that wavelength were fabricated. As the GaAs half VCSEL used in this case is designed for surface emission, a 100 nm thick gold layer needs to be deposited on top of the p-DBR to suppress the surface emission. Moreover, the surface emission of the device prior to gold deposition works to our advantage as it enables the evaluation of the polarization state and the transverse mode characteristics of the device.

6.3.1 Static performance

6.3.1.1 Surface emitting characteristics

To evaluate the properties of the Gen2 HC-VCSIL cavity, the surface emission was studied prior to the deposition of the surface gold layer. Fig 6.12 (a) shows the polarization-resolved light-current-voltage (LIV) characteristics at 25ºC of a device with an intra-cavity grating period of 545 nm and 50% DC, measured from the surface using a free-space polarizer and a large area Si photodetector. The measurement result shows that the cavity only supports lasing in the TE polarization, which is consistent with the simulations.

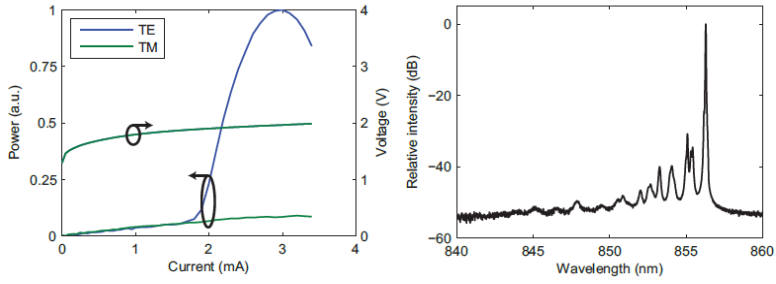

Fig. 6.12. (a) Polarization-resolved surface-emitted light-current-voltage characteristics for a 5 μm oxide-aperture diameter VCSIL with 545 nm intra-cavity grating period and 50% DC (prior to gold deposition on the surface). (b) Surface emitssion spectrum for the same device operated at 2.5 mA.

The surface-emitted spectrum for the same device at a bias current of 2.5 mA is shown in Fig 6.12 (b). The spectrum shows near-single-mode operation with a side-mode suppression ratio (SMSR) of 30.8 dB and a peak wavelength of 856.3 nm. This indicates that the cavity is mode selective enough to achieve near single transverse mode emission. At this stage, without the gold layer on top of the surface to suppress surface emission, the waveguide-coupled power was weak due to the dominant cavity loss from the top surface emission. Below we will elaborate on the waveguide-coupled characteristics of Gen2 HC-VCSILs.

6.3.1.2 Waveguide-coupled characteristics

With the gold layer on top of the p-DBR surface, the waveguide-coupled output from the VCSIL is coupled into a bare OM4 multi-mode fiber by a TE grating coupler (GC) with peak coupling efficiency near 855 nm. As discussed in Chapter 4, the grating coupler used in this measurement has a loss of -5.75 dB when coupling to a multimode mode fiber. To be able to estimate the actual optical power coupled into the SiN waveguide from fiber-coupled measurements, the measured optical power through the grating coupler was compensated for the grating coupler loss. The single-sided on-chip continuous wave LIV characteristics of VCSILs with five intra-cavity grating periods ranging from 525 to 545 nm and 55% DC were then measured at 25^{o}C using a fiber-coupled power meter, as shown in Fig. 6.13(a). The variation of threshold current with intra-cavity grating period is expected to follow the variation of the threshold gain predicted by the simulation result shown in Fig 3.13 (Chapter 3). However, as can be seen from Fig. 6.13 (a) the influence of the intra-cavity grating period on threshold current is not as strong as numerically estimated. This indicates that there are unexpected dominant losses in the cavity due to surface roughness, material loss, etc. From Fig. 6.13(a), we see that the slope efficiency trend is in agreement with the simulation result shown in Fig 3.14 in terms of the reduction of the slope efficiency with an increased intra-cavity grating period. There is a clear difference in the maximum output power that is coupled into the SiN waveguides as a function of the intra-cavity grating period. A VCSIL with the smallest grating period of 525 nm exhibits a threshold current of 1.13 mA providing a maximum single-sided waveguide-coupled output power of 73 μW at 2.6 mA bias current. The single-sided slope efficiency and the differential resistance for this device are 0.085 W/A and 78 Ω, respectively.

Compared to the simulated single-sided slope efficiency, the experimental slope efficiency is somewhat lower, which could be due to the unexpected dominant cavity losses. The on-chip spectrum for a VCSIL with intra-cavity grating period of 525 nm, at a bias current of 2.5 mA is shown in Fig. 6.13 (b). The SMSR is 28.9 dB, while the peak wavelength is at 856.6 nm. As can be seen from the spectra in Fig. 6.12 (b) and Fig 6.13 (b), the demonstrated VCSIL has

better transverse mode control than ordinary oxide-confined VCSELs with the same aperture size, both before and after deposition of gold on the surface aperture. This can be attributed to the fact that the higher order transverse modes contain spatial frequency components with larger off-normal angles than the fundamental mode and the spatial frequency components with large off-normal angle couple more efficiently to the waveguide, thereby leading to an increase in the threshold gain. Since the gain is clamped at the threshold gain of the fundamental mode, a good transverse mode control is obtained from the grating.

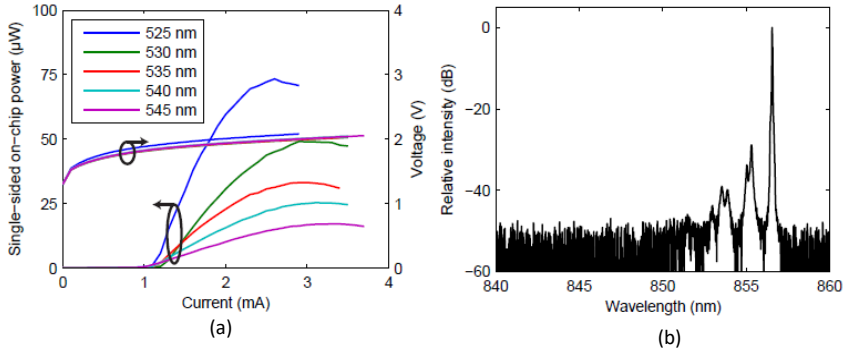

Fig. 6.13 (a) Waveguide-coupled light-current-voltage characteristics for 5 μm oxide-aperture diameter VCSILs with intra-cavity grating periods ranging from 525 - 545 nm (after gold deposition on the surface). (b) Spectrum for the 525 nm device operated at 2.5 mA.

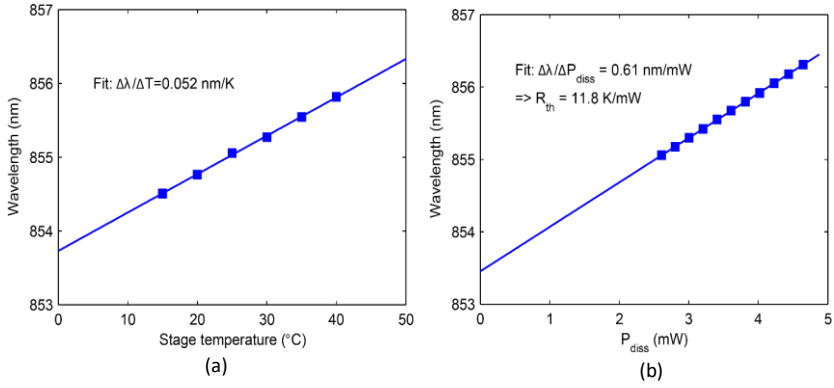

Fig. 6.14 (a) Wavelength of the fundamental mode versus dissipated power at 25 °C for HC-VCSILs with oxide aperture of 5 μm with fits to extract the thermal impedance.

The thermal impedance is deduced by tracking the red shift of the fundamental mode as a function of stage temperature and dissipated power. The fundamental mode redshifts with temperature by 0.052 nm/K, while it redshifts with dissipated power by 0.61 nm/mW (Fig. 6.14). At 25ºC the thermal impedance is 11.8 K/mW, which is similar to the 10.7 K/mW of a Gen1 VCSEL with the same aperture diameter. The thermal impedance is ~4 times higher than for an ordinary GaAs-based oxide-confined VCSELs [5] and explains the early onset of thermal rollover in both these cases.

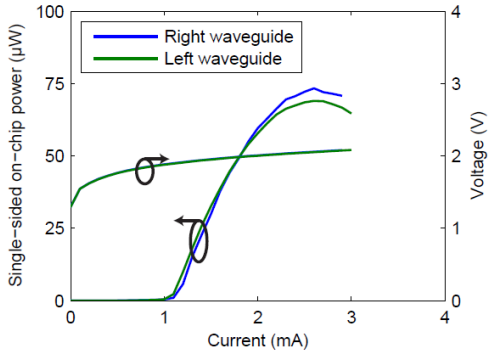

Fig. 6.15 Measured light-current-voltage characteristics where the power has been measured from both grating couplers for a VCSIL with 525 nm intra-cavity grating period and 55% DC.

Finally, the coupling symmetry was studied. As can be seen in Fig. 6.15, an equal amount of power is tapped off into both connected waveguides in opposite directions. This indicates that the VCSIL aperture is well aligned with the intra-cavity grating.

6.4 Conclusion

In summary, we demonstrated a heterogeneously integrated continuous-wave electrically-pumped Gen1 VCSEL and Gen2 VCSIL. A substantial improvement in performance is observed when the 4 nm thin GaAs layer present in the laser cavity was removed by digital etching.

Gen1 HC-VCSELs with a 10-μm oxide-aperture diameter have an output power (modulation bandwidth) of 2.3 mW (10.0 GHz) at 25 °C and 0.9 mW (6.4 GHz) at 85 °C for different interface thicknesses and gain-to-resonance detuning. The HC-VCSEL with the largest detuning of −15 nm (thickest bonding interface) also shows weak temperature dependencies of the threshold current and the modulation bandwidth over the temperature range 25–85 °C. It was found that the

thermal impedance is independent of the thickness of the bonding interface, therefore being largely determined by the thermal conductivity of the dielectric DBR. Finally, an error-free data transmission back-to-back at bit rates up to 25 and 10 Gbit/s at 25 and 85 °C, respectively, is demonstrated using a 5-µm oxide-aperture diameter Gen1 HC-VCSEL with moderately large gain-to-resonance detuning.

The intra-cavity grating used inside the Gen2 HC-VCSIL cavity provides the advantage of setting the polarization of the output coupled into the SiN waveguide together with transverse mode control. A Gen2 HC-VCSIL with a 5 µm oxide aperture diameter has a threshold current of 1.13 mA and produces a maximum single-sided waveguide-coupled output power on the order of 73 µW at 856 nm. The slope efficiency and the thermal impedance of the corresponding device are 0.085 W/A and 11.8 K/mW, respectively.

The performance of both the Gen1 HC-VCSEL and Gen2 HC-VCSIL was to a large extent limited by the high thermal impedance due to the dielectric DBR. Further, the performance of the Gen2 VCSIL was inferior to the Gen1 VCSEL due to unexpected additional cavity losses, attributed to surface roughness at the bonding interface and excess material absorption.

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7

Conclusions and Future Perspectives

7.1 Conclusions

As elaborated throughout this work a hybrid integration approach is promising to facilitate a SiN photonic integration platform with an energy efficient laser source, a VCSEL. During the course of this work, we have made a number of important contributions towards the design and development of such hybrid cavity VCSELs. The important contributions and achievements of this work are summarized below:

- As a first step towards the realization of a heterogeneously integrated VCSEL, we proposed a Gen1 HC-VCSEL**,** where a GaAs half VCSEL was attached to a Si-integrated dielectric DBR via adhesive bonding. We provided theoretical and technical background for the demonstration of these VCSELs. Although these VCSELs were surface emitting, it helped in the development of the integration process and to study the impact of the high thermal impedance dielectric DBR on the integrated VCSEL performance. A successfully demonstrated Gen1 HC-VCSEL showed that, with a 10-µm oxide-aperture diameter, we can reach an output power (modulation bandwidth) of 2.3 mW (10.0 GHz) at 25 °C and 0.9 mW (6.4 GHz) at 85 °C. We also studied the impact of the bonding interface thickness of such HC-VCSELs on important static and dynamic performance parameters. We showed that the VCSEL with resonance to

gain peak detuning of −15 nm (thickest bonding interface) has a weak temperature dependency of the threshold current and the modulation bandwidth over the temperature range 25–85 °C. We also found the thermal impedance to be independent of the thickness of the bonding interface, therefore being largely determined by the thermal conductivity of the dielectric DBR. Finally, we demonstrated error-free data transmission back-to-back at bit rates up to 25 and 10 Gbit/s at 25 and 85 °C, respectively, using a 5-µm oxide-aperture diameter HC-VCSEL with moderately large gain-to-resonance detuning.

- We further proposed a modified laser design by implementing a weak diffraction grating in the hybrid cavity to tap off power to an in-plane SiN waveguide. This intra-cavity grating also provided the advantage of setting the polarization of the output coupled into the SiN waveguide with transverse mode control. Theoretical and technical background for the realization of such lasers were also presented. We could successfully demonstrate a heterogeneously integrated continuous-wave electrically-pumped vertical cavity Si-integrated laser (VCSIL) with laser output coupled into a SiN waveguide. A VCSIL with a 5 µm oxide aperture diameter had a threshold current of 1.13 mA and produced a maximum single-sided waveguide coupled output power of ~ 73 µW at 856 nm. The slope efficiency and the thermal impedance of the corresponding device were 0.085 W/A and 11.8 K/mW, respectively.

7.2 Current and future perspectives

The performance of the current VCSELs can probably be significantly improved by considering the following points:

- Gen1 VCSEL: The Performance of our Gen1 HC-VCSELs was to a large extent limited by high thermal impedance due to the dielectric DBR. Therefore, the thermal properties need to be improved to be able to catch up with state-of-the-art discrete VCSELs. This can be achieved by replacing the dielectric DBR with a DBR with high index contrast, such as a-Si/SiO_2 DBR, thereby reducing the number of DBR pairs required and by integrating a metallic heat spreader.
- Gen2 VCSIL: The initial results of Gen2 VCSILs are promising. However, they are inferior to Gen1 HC-VCSELs. To demonstrate an improved performance with in-plane emission, we need to investigate and solve the origin of the unexpected cavity losses. The origin of these losses are currently not well understood.

In future, a transfer printing integration approach can be used to integrate VCSELs on a SiN waveguide platform. It is anticipated that the transfer print technology will replace die-to-wafer or wafer-to-wafer bonding technology for III-V light source integration for relatively large volume applications. Also, to integrate multi-wavelength VCSEL arrays on the SiN waveguide platform, the most viable solution is to change the cavity length of the VCSEL. This can be achieved by varying the top oxide thickness of the device by etching the oxide on top of the grating. However, the topography introduced this way does not allow for wafer bonding anymore. As can be seen from Fig. 7.1, with the help of transfer printing, we can achieve multi-wavelength VCSEL arrays by changing the length of the cavity by different amounts on the same chip.

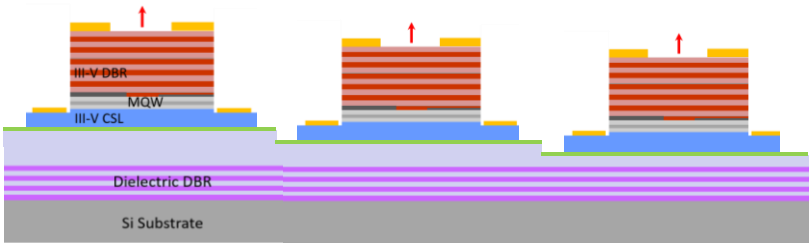

Fig. 7.1 (a) Schematic cross-section of a transfer printed VCSEL on the same chip.

A single mode, polarization stable, waveguide coupled VCSEL would benefit various on-chip optical interconnect and sensing applications. Further, an integrated multi-wavelength array of waveguide-coupled VCSELs would also enable the realization of PIC-based WDM transmitters for optical interconnects and multi-wavelength sources for biophotonic applications.