Wafer-Scale Fabrication Technology for Silicon Photonic Integrated Circuits

Fabricagetechnologieën op waferschaal voor fotonische geïntegreerde circuits in silicium

Shankar Kumar Selvaraja

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ஏந்நன்றி கொன்றார்க்கும் உய்வுண்டாம்; உய்வில்லை
செய்ந்நன்றி கொன்ற மகற்கு.

\- திருக்குறள் (423)

The virtue-killer may be saved
Not benefit-killer who is damned.

\- Thirukkural (423)

Table of Contents

List of Acronyms

A

AFM	Atomic Force Microscope
AWG	Arrayed Waveguide Grating
APM	Ammonium Peroxide Mixture

B

BARC	Bottom Anti-Reflective Coating
BHF	Buffered hydrofluoric acid ($NH_4F : HF$-6:1)
BOx	Burried Oxide

C

C	Carbon
CD	Critial Dimension
CVD	Chemical Vapour Deposition
CMOS	Complementary Metal Oxide Semiconductor
CAMFR	CAvity Modelling FRamework
CMP	Chemical Mechanical Polishing

D

DBR	Distributed Bragg Reflector
DC	Directional Coupler
DoF	Depth of Focus
DUV	Deep-ultraviolet

E

EL	Exposure Latitude

F

FC	Fiber Coupler
FIB	Focused Ion Beam
FTIR	Fourier Transformed Infrared Spectroscopy
FSR	Free Spectral Range

H

H	Hydrogen
HBr	Hydrogen Bromide
HDP	High Density Plasma
He	Helium
HF	Hydrofluoric acid

I

ICP	Inductively Coupled Plasma

L

LPCVD	Low Pressure Chemical Vapour Deposition

M

ME	Main Etch
MMI	MultiMode Interference coupler
MZI	Mach-Zehnder Interferometer

N

NA	Numberical Aperture

O

O/O_2	Oxygen
OE	Over Etch
OPC	Optical Proximity Correction
OPE	Optical Proximity Effect
OPE	Overlapping Process Window

P

PCG	Planar Concave Grating
PECVD	Plasma Enhanced or Assisted Chemical Vapour Deposition
PhC	Photonic crystal
PhW	Photonic wire
PW	Process Window

R

RFC	Raised Fiber Coupler
RIE	Reactive Ion Etching
RF	Radio Frequency

S

SAD	Selected Area Diffraction
SARF	Sub Resolution Assist Feature
SE	Spectroscopic Ellipsometry
SEM	Scanning Electron Microscopy
SF_6	Sulfur hexafluoride
Si	Silicon
SiN	Silicon Nitride
SiO_2	Silicon dioxide
SLED	Superluminescent Light Emitting Diode
SOI	Silicon-On-Insulator
SPM	Sulfuric acid hydrogen Peroxide Mixture

T

TEM	Transmission Electron Microscope
TEOS	TetraEthylOrthoSilicate
TMAH	TetraMethylAmmonium Hydroxide

W

WDM	Wavelength Division Multiplexing
WG	Waveguide
WiW	With in Wafer
WtW	Wafer to Wafer

X

XRD	X-Ray Diffraction

Nederlandse samenvatting

Communicatie is een integraal deel van ons leven geworden. Fotonica speelt een ontzagwekkende rol in dit proces. De introductie van optische vezel communicatie heeft de capaciteit voor informatieoverdracht naar nieuwe hoogten gebracht. De trend richting fotonica heeft ook de informatieoverdracht op verschillende lengteschalen verbeterd. In supercomputers bijvoorbeeld is de verwerkingssnelheid nu beperkt door de bandbreedte van de interconnecties. Door gebruik te maken van optische interconnecties kan deze flessenhals vermeden worden en de snelheid verder worden opgedreven. Een gelijkaardig voorbeeld kan gevonden worden bij lange afstand communicatie waar het gebruik van een volledig optische signaalverwerking de snelheid van informatieoverdracht verhoogd.

Technologie gebaseerd op Silicium-op-isolator (SOI) materiaal wordt beschouwd als de sleutel om geïntegreerde fotonische circuits te realiseren. De drie voornaamste voordelen van silicium zijn 1) een superieure materiaalkwaliteit (transparant voor infrarode golflengten), 2) een hoge brekingsindex en 3) een gekend en veelgebruikt materiaal bij de CMOS fabricagetechnologie van de micro-elektronica. Door gebruik te maken van de CMOS fabricagetechnologie op de schaal van een wafer[1], kunnen de fotonisch ge integreerde chips gemaakt worden met een hoog rendement en lage kost. Deze combinatie van materiaal en fabricagetechnologie maakt van siliciumfotonica het platform bij uitstek voor het maken fotonisch geintegreerde circuits en voor de integratie van elektronica met fotonica.

Er blijven echter nog altijd een aantal kernuitdagingen om het ideale siliciumfonotica platform te realiseren voor een brede waaier aan toepassingen. Voor fotonisch geïntegreerde circuits, kunnen de kernuitdagingen gegroepeerd worden in twee categorieën: componenten en fabricage. Fotonische componenten zoals lichtbronnen, versterkers, modulatoren, golfgeleiders, filters, splitters en detectoren zijn essentieel om een op zichzelf staande fotonische geïntegreerde chip te verwezenlijken. Jammer genoeg laat de indirecte energiekloof van silicium niet toe om efficiënte lichtbronnen, versterkers en detectoren te realiseren. Door gebruik te maken van een heterogene integratie met III-V materiaal kan dit probleem overwonnen worden. De passieve componenten zoals golfgeleiders en filters behoeven een fabricageproces met een hoge resolutie. Fabricage met hoge resolutie laat toe om componenten te maken met lage verliezen en het biedt tevens de controle die

[1] In de computerindustrie worden chips gefabriceerd op een cirkelvormige plak silicium, die omwille van het vorm wafers genoemd worden. Soms wordt de diameter van de plak vermeld, vb. 200 mm wafers.

nodig is om de component reproduceerbaar te maken.

Dit werk

Het doel van dit werk is tweeledig: in de eerste plaats het ontwikkelen van een fabricagetechnologie met hoge resolutie voor silicium fotonische circuits gebruik makende van geavanceerde 200mm CMOS fabricage toestellen; in de tweede plaats het ontwikkelen van een alternatief materiaalsysteem in plaats van kristallijn silicium voor fotonisch en electronisch-fotonisch geïntegreerde circuits.

Patroonvorming met hoge resolutie

Met behulp van een state-of-the-art 200mm proeflijn te *imec* hebben we een geavanceerd fabricageproces ontwikkeld om de 2 belangrijkste uitdagingen voor de fabricage van silicium fotonische componenten aan te pakken: het bereiken van laag propagatieverlies en hoge uniformiteit. Deze twee uitdagingen werden aangepakt door een rigoureuze procesontwikkeling. Het maken van patronen gebeurde met behulp van 193nm stap-en-scan optische lithografie en een droog-ets proces. Door deze processen te optimaliseren, kon de ruwheid van de zijwanden laag gehouden worden en daardoor ook de verliezen in de golfgeleiders. Dankzij dit proces kon een propagatieverlies bereikt worden van maar 1.36 dB/cm voor een fotonische draad-golfgeleider (450×220 nm^2). Door gebruik te maken van een hybride circuit kon het verlies verder gereduceerd worden tot 0.23 dB/cm.

Uniformiteit van de fotonische componenten is de sleutel om complexe circuits te maken en te commercialiseren. Aangezien fotonische siliciumcomponenten heel gevoelig zijn voor kleine variaties in de dimensies, werd het fabricageproces geoptimaliseerd om sub-nanometer uniformiteit te hebben. Voor componenten die golflengteselectief zijn[2] en in elkaars buurt stonden, vonden we een uniformiteit van 20 pm. In het geval ze over een afstand van 200 mm van elkaar stonden was de uniformiteit nog steeds $\approx$1 nm. Aanvullend op deze demonstraties, hebben we ook het effect bestudeerd van afstand en densiteit van apparaten op de uniformiteit en absolute golflengte respons. We hebben ontdekt dat als componenten dichter staan dan 15 μm bij andere componenten ze de absolute dimensie en hierdoor de absolute golflengte respons kunnen beïnvloeden.

Alternatieve materiaaltechnologie

SOI wafertechnologie gebaseerd op kristallijn silicium is de dominante materiaaltechnologie voor siliciumfotonica. In dit werk hebben we ook alternatief materiaal bestudeerd: amorf en polykristallijn silicium voor fotonische en elektronisch-fotonische geïntegreerde circuits. Dit materiaal laat een flexibeler design toe van materiaaleigenschappen zoals de brekingsindex, de conductiviteit en de bandkloof. Door gebruik te maken van door plasma versterkte chemische damp depositie

[2]Een voorbeeld zijn filters die een golflengte heel nauwkeurig moeten filteren.

(PECVD) en lage druk chemische damp depositie (LPCVD), hebben we respectievelijk amorf en polykristallijn silicium verkregen met lage verliezen. Vooral amorf silicium, gemaakt met PECVD, is interessant omdat het kan aangebracht worden bij lage temperaturen (<450C) en dit maakt het bruikbaar voor de integratie van elektronica met fotonica. We hebben in amorf silicium een propagatieverlies aangetoond van 3.45 dB/cm voor fotonische draadgolfgeleiders die slechts een mode geleiden. Dit lage verlies werd bekomen door het reduceren van defecten door middel van waterstofpassivering tijdens of na de depositie. We hebben aangetoond dat de golflengterespons van de componenten getrimd kan worden, door het controleren van de hoeveelheid waterstof door thermische behandeling. Dit laat toe om na de fabricage op een gecontroleerde manier de non-uniformiteit van componenten, gecreëerd tijdens het maken van de patronen, te trimmen.

Het aanbrengen van lagen, laat toe om een fotonisch circuit te maken met meerdere lagen. De densitiet van circuits kan verhoogd worden door het vertikaal integreren van fotonische circuits. Door gebruik te maken van de voordelen van de depositie van lagen, hebben we een fotonisch circuit gemaakt van twee lagen, waarbij de optische koppeling gebeurde via een roosterkoppelaar. Met een simpel optisch design, bekwamen we een koppelingsefficiëntie van 11 %. Numerieke simulaties geven aan dat dit nog verder verbeterd kan worden door een optimalisatie van het ontwerp.

English summary

Communication has become an integral part of life. Photonics plays a formidable role in this process. Introduction of optical fiber communication has shifted the information transfer capacity to new levels. The shift towards photonics has also improved the information transfer over different length scales. For instance, in high performance computing the processing speed is limited by the bandwidth of the electronics, meanwhile using an optical interconnect would increase the speed without any constraints. Similarly, in long distance communication the use of all-optical signal processing increases the data transfer rate.

Silicon-on-Insulator (SOI) material technology is considered as the key for photonic integrated circuits. The three main advantages of silicon are 1) superior material quality, i.e., transparent to infrared wavelengths, 2) high refractive index and 3) a well-known material to microelectronics CMOS fabrication technology. Moreover, by using the wafer scale CMOS processing technology the photonic integrated chips can be delivered with high yield and low cost. This combination of material and fabrication technology makes silicon photonics an enabling platform for photonic integrated circuits and likewise, for electronics-photonics integration.

However, there are still key challenges persist in realizing an ideal silicon photonics platform for a wide range of applications. For photonic integrated circuits, the key challenges can be grouped in two categories: circuit components and device fabrication. Photonic components such as light sources, amplifiers, modulators, waveguides, filters, splitters and detectors are essential to realise a self-contained photonic integrated chip. The advantages of silicon mentioned above is hampered by the indirect band-gap, which forbids light emitters, amplifiers and detectors. Using heterogeneous integration III-V material can be used to overcome this issue. The passive devices, namely, waveguides and filters require a high resolution fabrication process. This high resolution fabrication allows low-loss devices and provides precise control over the device for reproducibility. Even though the CMOS fabrication process is compatible with photonics the requirements for a photonic circuit are very different from those of CMOS circuits.

This work

The goal of this work can be divided into two, firstly, to develop a high resolution fabrication technology for silicon photonic circuit using advanced 200 mm CMOS fabrication tools. And secondly to develop an alternative material system

to crystalline SOI for photonic and electronic-photonic integrated circuits.

High resolution device patterning

We have developed an advanced fabrication process using start-of-the-art 200 mm pilot line at *imec* to address the challenges in fabrication of silicon photonic devices: propagation loss and device uniformity. These two challenges were addressed through rigorous process development of the patterning process. The patterning was done by using 193 nm step-and-scan optical lithography and a dry etch processes. By optimising these processes the sidewall roughness was kept low to achieve low-loss waveguides. Using such a process we have demonstrated process propagation loss as low as 1.36 dB/cm for a photonic wire (450×220 nm^2). Furthermore, this loss was reduced to 0.23 dB/cm by using hybrid waveguide circuit. To our knowledge, these loss numbers are the lowest reported so far for compact waveguides fabricated using wafer scale technology.

Uniformity of photonic devices is the key for building complex circuits and also for commercialisation. Since silicon photonic devices are very sensitive to small dimension variation the fabrication process was optimised to achieved sub-nanometer device uniformity. For wavelength selective devices, which were closely placed we found a uniformity of 20 pm. Likewise, for devices over a 200 mm it was $\approx$1 nm. In addition to these demonstrations, we have studied the effect of distance and density of devices on the uniformity and absolute wavelength response. And found that devices as close as 15 μm apart could affect the absolute dimension of the device and therefore, the absolute wavelength response.

Alternative material technology

Crystalline silicon based SOI wafer technology is the dominant material technology in silicon photonics. In this work, we have developed an alternative material: amorphous and polycrystalline silicon for photonic and electronic-photonic integrated circuits. This material allows design of flexible material properties, such as the refractive index, conductivity and band gap. By using plasma enhanced chemical vapour deposition (PECVD) and low pressure chemical vapour deposition (LPCVD) we have developed low-loss amorphous and polycrystalline silicon, respectively. PECVD-based amorphous silicon is particularly interesting as it can be deposited at low temperatures ($<$450C), which allows back-end compatible electronic-photonic integration. We have demonstrated propagation loss of 3.45 dB/cm for single-mode photonic wire waveguides in amorphous silicon. This low loss is achieved by reducing the defects in the film through hydrogen passivation, either during or after deposition. By controlling the amount of hydrogen through thermal treatment, we have shown that the wavelength response of the devices can be trimmed. This allows controlled post-fabrication trimming of device non-uniformity created during the patterning process.

Layer deposition allows multi-layer photonic circuits. The circuit density can be increased through vertical integration of photonic circuits. Taking advantage of

the layer deposition, we have built double layer photonic integrated circuit optically coupled through a grating optical via. With a simple optical via design we have shown a via coupling efficiency of 11 $\%$, nevertheless numerical simulation show that this can be further improved through optimisation.

1 Introduction

1.1 Motivation

Information processing and transfer are key for social and economic development of human society. Historically, the use of electric wire based communication facilitated the first evolution in data transfer rate [1]. The capacity of communication using copper cables continuously increased until the introduction of optical fiber communication systems. This has shifted the information carrying capacity of communication systems to new levels [1] and has tremendously improved the data carrying capacity of long distance links. The use of low-loss (<0.1 dB/Km) and low dispersion optical fibers make optical fiber communications the most suitable technology for long distance communication. Later, the application of wavelength division multiplexing (WDM), facilitated by the use of broadband erbium doped fiber amplifiers, has increased the capacity of the optical fiber further by using multiple wavelengths, each separately modulated, on the same fiber.

On the other hand, optical communication systems tend to be more expensive than electrical systems and the choice for one or the other is based on the overall figure of merit of the system. Historically a cross-over point has been seen for a distance-bandwidth product of 10 Mb/s·Km. Interpolating this to short distance communication links in computer chips, this metric implies a shift from electrical interconnect to optical interconnect for processor speeds above 10 GHz.

The tremendous bandwidth offered by these high speed communication sys-

[1] The speed of information transfer is measured in bits per second.

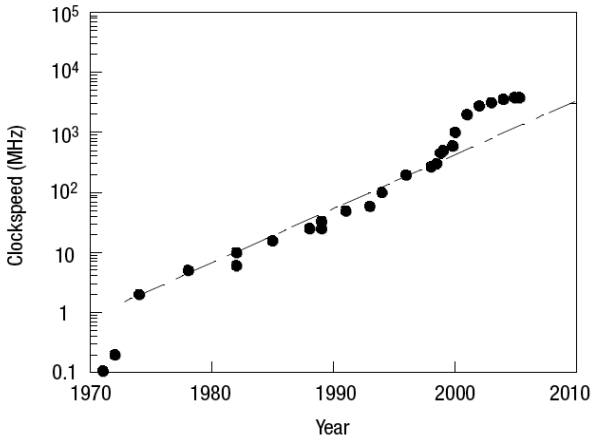


Figure 1.1: Microprocessor clock speed versus time [3].

tems can not be efficiently employed however if the data can not be processed in an efficient way. Fortunately, micro-electronics data processors evolved concurrently with the increase in available data rate. Integration of individual electronic components onto a single chip, an integrated circuit (IC), enabled scaling of the processing speed of the electronic circuits. Monolithic integration of electronic circuits using high volume manufacturing technology has been the key for realizing high speed and high performance computation. The speed of computation is measured in terms of the processor clock frequency, which has exponentially increased over the years. This increase in speed is a direct consequence of down scaling of the basic electronic components, the transistors. The phenomenon of this scaling is often referred to as Moore's Law, stating that the number of transistors on a chip doubles every 18 months [2].

This increase of clock speed has continued over the past thirty years but recently this trend was no longer followed (Fig. 1.1) [3] . The increase of speed realized by the scaling of the circuits seems to be reaching a limit, originating from the electrical interconnects between the transistors, resulting in a speed ceiling of a few GHz. The two major limitations are power consumption and electromagnetic interference. Both are directly related to scaling. As the transistors become smaller their leakage current increases and this waste of power eventually is dissipated as heat. Secondly, the electrical interconnects in the circuits which connect the individual transistors experience limitations due to resistance-capacitance delays. This is often called the interconnect bottle-neck and now limits the maximum operating speed of a chip.

It is now believed optics may partly solve this problem. This will require the development of densily integrated electro-photonic circuits. The prospects of this

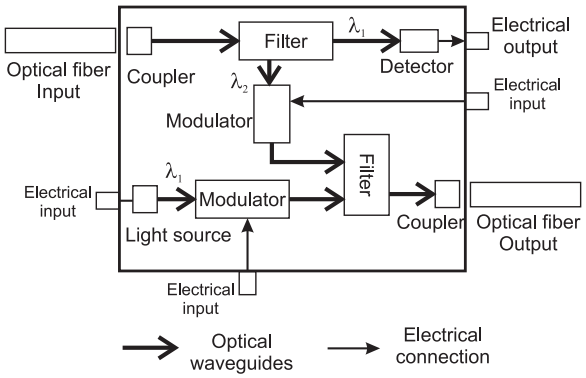


Figure 1.2: Schematic of a photonic integrated circuit.

integration are immense. As the optical fiber systems provide the highest speed for data communication, there is no reason why such a system cannot work in an integrated form. The essential components, such as the laser, modulators and detectors all can have a large bandwidth. However, the optical devices being used currently in classical communication systems are large, discrete and expensive. In order to use these components in an integrated form, they should be engineered to various specifications, such as material, size, bandwidth, power and process compatibility. Integration of photonic and electronic circuits will also enable communication networks with higher complexity and unique functionality. Similar to electronic integrated circuits, photonic integrated circuits should exhibit lower cost, higher reliability, and increased functionality compared to discrete components.

In summary, the bandwidth-distance limitation of electronic interconnects has led to a bottleneck in data transfer and processing rate. By using integrated photonic interconnects this bottleneck can be bridged. This also enables both integrated electronic circuits and photonic circuits to extend their capability beyond efficient communication and computation technologies.

1.2 Photonic integrated circuit technology

The main idea of a photonic integrated circuit is to monolithically integrate all required devices on a single chip, in a single material platform. These components include:

Light Source Effcient and low-power single wavelength lasers

Couplers The link between the photonic integrated circuit and the external world.

A coupler should be able to couple light efficiently between a light source or an optical fiber and the photonic integrated circuit.

Waveguides Transport of light between two designated points within in a chip with low attenuation.

Wavelength selective devices Can separate or combine signals as a function of wavelength or in the time domain by using wavelength tuning.

Modulators Imprint a data signal on the optical carrier.

Photodetectors Facilitate optical-to-electrical conversion.

Figure 1.2 shows a generalized example of a photonic integrated circuit. It has an optical fiber coupler, coupling light from an external optical fiber to the chip. It has splitters and wavelength selective devices which direct the signals over the chip, split or recombine them according to wavelength. It has a modulator, which modulates the carrier with wavelength λ_1 with a data stream which is fed to the chip as an electrical signal. And it has a detector, resulting optical-to-electrical conversion. Note that the same wavelength can be used multiple times on the same chip. This is e.g. the case for λ_1 which can be modulated with additional data in the lower path despite the presence of the same wavelength on the chip in the upper path.

The choice of the material platform to realize such a photonic integrated circuits depends its desired characteristics. As for any other large-scale technology, cost and compatibility with exisiting technology platforms is important. The following characteristics are considered as essential for photonic integrated circuits:

Loss

Attenuation of the optical signal is a very critial parameter for the photonic circuit performance. The propagaion loss in the waveguide and coupling loss between the chip and the outside world (either electric or optical) should be kept as low as possible. The propagation loss can vary from as low as 0.01dB/cm for the lowest loss silica-on-silicon waveguides to over 10dB/cm for high contrast membrane type devices.

Integration density

The number of devices that can be put on a single chip will increase the circuit's complexity and functionality. Similar to electronic circuits, increasing the device density reduces the chip area required and thereby the cost per chip. A high re-

fractive index contrast [2] between the waveguide core and cladding are necessary to realise waveguide bends with small radius.

Polarization independence

Light travelling through an optical fiber system typically has a mixed and/or unknown polarization. Photonic integrated circuits should be able to handle different polarization states and avoid polarization dependent loss.

Integration with electronics

Since today and for the forseeable future electronics is undoubtedly the most powerful and energy efficient data processing technology available; integrating the photonic circuit with electronics is therefore strongly desired.

Electrical/optical conversion

The material platform should allow embedding and de-embedding of electrical signals onto an optical carrier at high speed.

Vertical integration

The possibility for integrating circuits vertically in an effective way may further increase the circuit density and complexity and enhance thereby its functionality. A material platform that allows for such type of integration, will be more scalable compared to other technologies.

The list of requirements presented above and the emphasis that is put on each of them, in function of a given application, will determine which material platform is the most suitable for realizing the photonic integrated circuit under study. As for any other complex problem, there will exist tradeoffs between the requirements in identifying the most suitable technology and material platform. For instance, for realizing low loss waveguides together with detectors, we cannot define a single material which is transparent (for the waveguides) and absorbing (for the detectors) at the same time.

Silica-on-silicon technology has been the most sucessfull material technology platform for realizing photonic integrated circuits. The platform offers key advantages such as, low-loss waveguides, efficient light-chip coupling, polarization independent operation, reasonable cost and limited sensitivity to fabrication imperfections [4, 5]. However, due to its low refractive index contrast ($<1.5\%$) the size of these circuits is large, limiting the in-plane photonic device density. Similarly, Lithium Niobate ($LiNbO_3$), despite its excellent electro-optic and wave guiding

[2] Refractive index contrast Δn is defined here as the ratio of refractive index of the core and the cladding materal. It is given as $(n_{core}^2 - n_{core}^2)/2n_{core}^2$

properties [6–8] has limited possibilities for scaling and integration with electronics, which ultimately limites its application as a mainstream material for photonic integrated circuits.

III-V semiconductor materials seem to be the ideal choice for realizing photonic integrated circuits: they have a direct bandgap, allowing for efficient light generation, and through bandgap engineering also almost all other requirements listed above can be fulfilled. In addition, they have a high carrier mobility allowing high performance electronic circuits. Integrated circuits built using this material platform have been extensively used for electronic and photonic devices in the telecommunication industry. Integration of lattice-matched, quaternary III-V semiconductor alloys on an InP substrate yields light sources, detectors, amplifiers, and electro-absorption modulators. Despite these excellent advantages, the III-V material platform is very expensive. In comparison to silicon based electronic circuits, which use large wafer scale fabrication technology, III-V wafer processing does not have sufficient market volume to realise considerable cost benefits. The further development of the III-V material platform will depend on whether or not a cheaper alternative will become available.

Possibly, this alternative could be a silicon based photonics platform, compatible with high volume microelectronics platforms, in particular those used for realizing complementary metal oxide semiconductor (CMOS) technology used in microprocessor fabrication. The ability to fabricate high performance photonic integrated circuits with such a high-volume fabrication technology would enable integration of complex electronics and photonic circuits on a single silicon chip. However, there are still a lot of challenges in realizing all required photonic components within this material platform. These will be outlined in the next section.

1.3 Silicon photonic integrated circuits

Silicon is the material that revolutionized electronic circuits. It has been the workhorse of electronic industry for over thirty years. As an optical material, silicon has an indirect band gap, which exclude its use as a light source. Despite this setback, silicon has various advantages. It benefits from the extensive processing knowledge from electronic circuit fabrication, it is transparent in the telecommunication band of the optical spectrum (λ=1300-1620 nm), and finally, it has a high refractive index contrast ($\Delta n \approx 40\%$) with silicon dioxide, thereby allowing for compact waveguide structures, with bending radii as small as 1 μm . In addition, germanium, which has high carrier mobility and absorption in the telecom spectrum can be grown on silicon and provides an optimal material for photodetection.

Over the years various active and passive functions have been demonstrated in silicon. Notable demonstrations include low-loss photonic wire waveguides [9, 10], high-efficiency fiber-chip coupling, compact devices [11], photodetec-

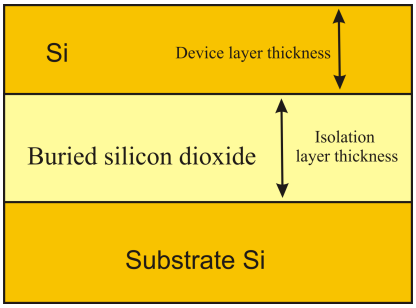


Figure 1.3: Schematic of a silicon on insulator substrate.

tors [12, 13] and high speed modulators [14–16]. With increasing maturity of the individual components also more complex circuits were built including control electronics [17]. Despite these demonstrations, an efficient light source in silicon is still a missing component. However, silicon has been used as a gain medium by exploiting stimulated Raman scattering [18, 19]. The achieved gain is at the cost of complex carrier sweeping procedure to avoid free carrier absorption in silicon. A more natural solution is to use III-V semiconductor lasers. III-V semiconductor can be grown on top of silicon, however, the technology is not yet mature enough to allow for the same material quality as that of pure III-V substrates. Another option is to heterogeneously integrate a III-V quaternary stack using a wafer bonding technique [20–24]. Up till now this technique seems the most viable option to realize active functions such as amplification and light sources integrated with a silicon photonic circuit.

Following these developments of individual components and more complex circuits, also more and more attention was given to a wide spectrum of applications, ranging from more traditional optical communications and datacom to more novel applications such as integrated spectroscopy, bio-photonics [25, 26], gas sensors [27, 28], and particle sensing [29].

Substrate technology

Silicon-on-insulator (SOI) seems to form the ideal substrate for realizing silicon integrated photonic circuits. Figure 1.3 depicts a schematic cross-section of a SOI substrate. Even though it was originally invented to improve device performance in transistors, the material technology was further embraced by integrated photonics. The thickness requirements of the device layer and buried oxide (BOx) are however very different for electronics and photonics applications. The thickness specification has been adapted over the years to suit photonic circuits. The thickness of the low index BOx layer should be sufficiently large enough to avoid

Reference	Top silicon thickness (nm)	Buried oxide (nm)
NTT [36]	200, 300	3000 -
Univ. Calif. LA [37]	3000	1000
IBM [38]	220	2000
IBM [39]	226	2000
MIT [40]	220	1000
MIT [41]	200	3000
Univ. Glasgow [10]	260	1000
Cornell Univ. [42]	240	3000
Univ. Surrey [43]	1000-1500	-
Univ. Surrey [44]	230	3000
Intel [45]	500	1000

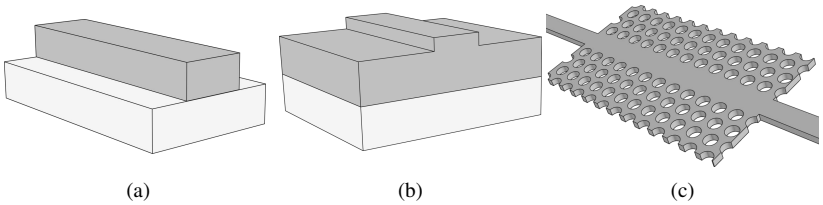
Table 1.1: Some of the SOI wafer thickness specifications for silicon photonics found in the literature.

leakage of light from the device layer to the silicon substrate. It has been shown by Dr. Pieter Dumon in his doctoral thesis that a BOx thickness of 2000 nm is required for sufficient isolation for both transverse electric (TE) and magnetic (TM) polarized light in the device layer [30]. The thickness of the device layer depends on the type of waveguide geometry, which could be based either on a large core layer (1000 nm thick) or a small core layer (200-300 nm thick). Table 1.1 shows some of the SOI wafer stacks used for realizing silicon photonic ICs by different research groups. In addition to the thickness of the device layer, the doping is an important material parameter. Very little is known about doping concentrations in different substrates used in silicon photonics. Since high doping levels can reduce the transmission, it is generally accepted that un-doped or very low doping levels are desirable for photonic applications.

SOI wafers are manufactured in a variety of ways: separation by implanted oxygen (SIMOX) [31, 32] , smart cut [33] , wafer bonding [34], and epitaxial layer transfer (ELTRAN) [35]. Among these techniques smart cut SOI wafers are most widely used in Si photonics because the related device layer is highly transparent for infrared wavelengths. In this work, we used smart cut SOI wafers with a 220 nm device layer on top of a 2000 nm BOx layer.

Waveguide technology

The main purpose of a waveguide circuit is to transport light through a medium between two designated points. In photonic integrated circuits, light is confined either through total internal reflection (TIR) or by using a photonic bandgap effect



(a) (b) (c)

Figure 1.4: Three widely using waveguide configurations in silicon photonic circuits (a) Photonic wire, (b) Rib waveguide and (c) Photonic crystal waveguide.

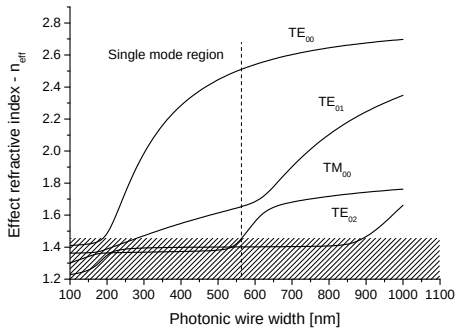


Figure 1.5: Effective refractive index at 1550nm for 220 nm high photonic wires. The hashed region shows lies the light line.

(PBG). The three most used waveguide types used in silicon photonics are shown in figure 1.4: a deep-etched photonic wire, a shallow-etched rib waveguide and a 2D-photonic crystal waveguide. The first two waveguide configurations work through TIR. Photonic crystal waveguides rely on the PBG effect and therefore there transmission bandwidth is limited to the crystal bandwidth, which is much smaller compared to the transmission band of photonic wire or rib waveguides. Hence the application of photonic crystals for waveguiding is limited compared to TIR based waveguides.

Single mode operation is an important requirement for the waveguides. Depending on their dimensions waveguide cross-sections like the ones shown in figure 1.4 a and b can support multiple solutions (modes) of the wave equation. Figure 1.5 shows the effective refractive index (n_{eff}) as a function of the width of a photonic wire. The n_{eff} depends on the waveguide material, cross-section, and the cladding material. Single mode operation is preferred over multi-mode operation for many reasons. The higher order modes travel with a different propagation constant compared to the lowest order mode and are less confined in the waveguides. The different propagation constants result in modal dispersion and reduce the distance-bandwidth product of the waveguides. The low confinement is prob-

lematic for two reasons: firstly, a large field-decay outside the waveguide reduces the maximum density of the devices and secondly, in the waveguide bends the higher order modes become leaky resulting in higher propagation loss. Furthermore, single mode operation allows for more simple device design.

1.4 Challenges in silicon photonics integrated circuit

Despite huge progress being made over the last years, silicon photonics still suffers from important challenges. The most relevant ones are listed below. In the next section we will explain how we have addressed these challenges through this work.

1.4.1 Losses

As mentioned already above, propagation loss is one of the key performance metrics of a photonic integrated circuit. The three primary causes for loss in a photonic waveguide are, material (bulk) absorption, surface absorption, and scattering loss from roughness. In any photonic circuit, these three factors contribute to optical loss in different proportions.

Material loss Even though silicon is considered as a transparent material for the telecommunication wavelengths band, the presence of defects can result in absorbtion of light either due to mid gap-gap states or due to free carriers. These defects can be either located in the bulk or on the surface of the waveguides. The defects in the bulk are usually a consequence of poor material quality or due to doping. Doping (*p* or *n*) can result in absorption loss due to free carrier absorption (FCA) for doping concentrations beyond $10^{18}cm^{-3}$. Even at low doping levels higher power density in the waveguides can result in two photon absorption (TPA), which generates carriers which in turn generate FCA [46, 47]. In a typical circuit, the injected power is low enough to prevent TPA and FCA, however in devices such as resonators and in non-linear applications TPA and FCA result in additional loss. One of the ways to reduce the impact of TPA and FCA is to sweep the carries from the waveguides by applying a voltage across the waveguides or by operating in a pulsed regime [48].

Sidewall and surface scattering Perturbation such as roughness in the waveguides creates scattering of light resulting in scattering loss. Top surface and sidewall roughness are the two primary scattering loss sources in a waveguide. Payne and Lacey [49] formulated scattering loss estimation by considering the mean square roughness and correlation function along with the field distribution and waveguide geometry. As mentioned earlier, the field distribution along the sidewalls is different for TE and TM polarized light hence the influence of sidewall and

top roughness influence the scattering loss accordingly. The TE polarized light is mainly affected by the sidewall roughness, while top surface roughness is of main concern for TM polarized light. The roughness on the top surface of a SOI wafer can be in the order of 0.1 nm, while sidewall roughness can be in the order of few nanometers. The sidewall roughness is a consequence of the pattern definition process, namely, lithography and dry etching. Hence, the scattering loss is primarily due to the quality of the pattern definition process. In addition to process improvements various post-fabrication roghness reduction techniques have been tried to reduce the sidewall roughness and hence the propagation loss [50, 51]. However, achieving low-loss without post processing is desirable to avoid fabrication overhead and complexities.

One way of reducing the scattering loss is by reducing the modal interaction with the sidewalls. This can be achieved by increasing the waveguide width or by using rib waveguide (Fig. 1.4b). It has been shown that propagation loss as low as 0.35 dB/cm is achievable by using multi-mode broad photonic wires. Similarly, propagation loss of 0.27 dB/cm was demonstrated for a multi-mode rib waveguide. Though the propagation loss is low, these waveguide geometries require large bend radius, which is unsuitable for compact circuits. An alternative is to use hybrid waveguide circuits with different waveguide geometries. A rib waveguides can be using in straight while a compact bend can be realized by photonic wire waveguide. Since the mode filed of these waveguides are different, a taper is required to match them. Apart from low-loss capabilities, with hybrid waveguide low-loss waveguide crossing can be easily implemented for complex waveguide routing schemes [52, 53].

Surface absorption The surface defects are generally due to the dry etch process and surface contaminations, such as metallic or organic particles [54, 55]. Similar to roughness, surface defects are present both on the top and sidewalls of the waveguides. The defects in the sidewalls are mainly caused by the etching process used for patterning the waveguides. During this process, the sidewalls are amorphized resulting in defect rich sidewalls. These defects can be cured by passivating the surface. It has been shown that encapsulating the devices with SiN, SiO_2 or H can reduce surface absorption as a result of passivation [56]. In any case high quality etching processes are a prerequisite for realizing low loss waveguides.

1.4.2 Accuracy required

High refractive index contrast devices, such as the ones used on a typical silicon platform are very susceptible to small fluctuations either in the operating environment or in the device dimensions. The photonic device response to changes in the environment is exploited in sensor applications, in particular in bio-sensors

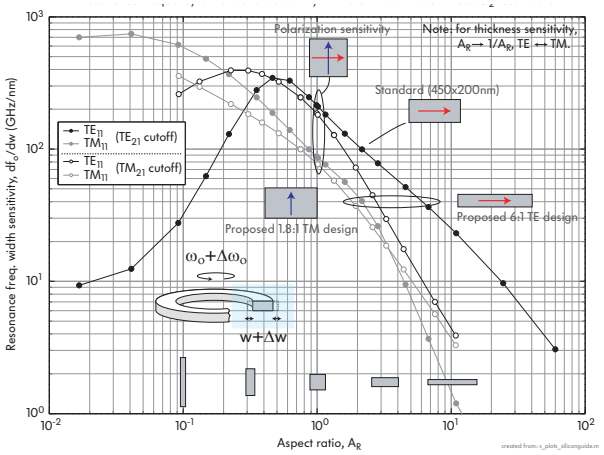


Figure 1.6: Resonance frequency sensitivity to waveguide width error [57].

[25, 58]. However, for other applications, such as communications and on-chip interconnects these variations can be fatal to overall operation of the circuit. For instance, a wavelength (de)multiplexer with 200 Ghz channel spacing would require a dimensional uniformity of $<<1.6$ nm [3] . The spectral response of a silicon photonic device can shift by a nanometer for an equivalent change in width or height of the device. Ultimately, even a monolayer can change the device response measurably (see chapter 4).

Inaccuracies or variations in the device dimensions are a consequence of the fabrication process. Unfortunately, this is one of the main reasons limiting wide spread commercialisation of silicon photonics. In general, the width of the waveguide is less well controlled than the height of the waveguide. The patterning process has to deliver the required accuracy, uniformity and reliability. It is very challenging to achieve these requirements in a high volume microelectronics manufacturing environment, where the dimensional tolerances is usually between 5-10 %. One way of tackling this non-uniformity is by using active tuning or trimming of the devices to compensate for device non-uniformity. For trimming, i.e. a permanent change of the structure, this requires special materials [59] or processes [60] that allow for such a change. On the other hand thermal or carrier injection can be applied for active tuning, however, these techniques require additional power during operation. In order to keep the tuning power low the non-uniformity generated by the substrate and patterning process technology should be minimized.

[3] Relation between frequency variaion Δf and corresponding wavelength change $\Delta\lambda$:
$\frac{\Delta f}{f} \approx \frac{\Delta\lambda}{\lambda} \Rightarrow \Delta f \approx C\frac{\Delta\lambda}{\lambda^2}$

1.4.3 A deposited Silicon-On-Insulator substrate technology

Even though crystalline SOI wafers exhibit superior material quality, they have some limitations. E.g. the accuracy of the device layer thickness is not sufficient for manufacturing silicon photonic integrated circuits with good uniformity and predictable center wavelength. For instance, the vendor specification for the thickness of a SOI wafer is ± 10 %, which means over a 200 mm wafer a 220 nm target silicon layer thickness can vary between 200 and 240 nm. This range of variation is simply unacceptable for a reliable photonic circuit technology for commercial deployment.

An alternative is to deposit a high refractive index material, such as amorphous or polycrystalline silicon with high uniformity and optical quality. Deposited materials are usually high in defects, which leads to high propagation loss. By engineering the deposition process the defects can be reduced. It has been shown that these materials can be deposited with excellent optical properties [61–66]. Various wavelength selective devices have been demonstrated in deposited silicon with performance comparable to crystalline silicon.

Furthermore, the ability to deposit a core material allows innovative device design. For instance, the standard 220 nm thick SOI limits the light coupling efficiency of grating couplers. Over the years, grating based fiber-chip coupler emerged as a versatile coupling technique for silicon photonics [67–69]. Out-of-plane coupling makes grating couplers an ideal tool for wafer scale testing. It has been shown that by using a grating a coupling efficiency of 30 % [67] is achievable. Even though this efficiency is sufficient for research work, it is very low for commercial use. An option to increase the efficiency is to use a different core thickness [70]. If a deposited silicon process is available this can be easily realized.

1.4.4 Integration with electronics

As mentioned earlier, one of the key applications of photonic integrated circuits is to increase the data transfer and computation speed of electronic chips. Integration of photonics with electronics can bring best of both worlds. As in any other engineering problem there are different options for solving this problem of electronic-photonic integration. The three most widely explored integration schemes are, 1) Back-end integration: Photonics on top of electronic chips, 2) Front-end integration: photonics along with the transistors [71], and 3) 3D-integration: stacking separate photonic and electronic circuits on top of each other and electrically connecting them using Through-Silicon Vias (TSVs) [72].

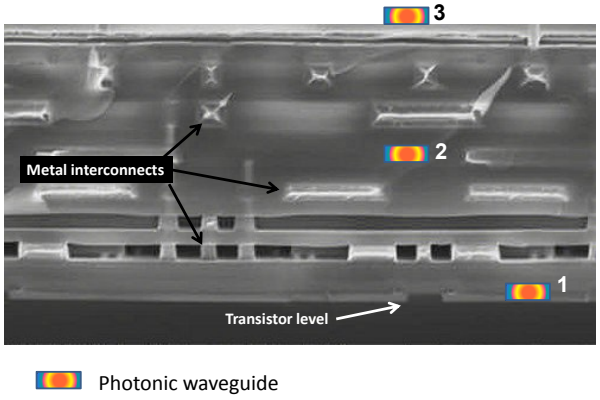


Figure 1.7: Possible integration of photonic circuits in an existing microelectronic circuit. Position 1 shows the fron-end integration, while 2 and 3 are back-end integration schemes.

Front-end versus Back-end processing

In the CMOS fabrication process, each fabrication step is identified as front-end or back-end. This identification is based of the stage at which the process is used. The front-end refers to fabrication process stages/steps involving individual transistor definition before connecting them to form circuits. All the steps involving connecting individual transistors with metal vias and lines until dicing are referred to as back-end processing. Figure 1.7 shows the front-end and back-end in a CMOS circuit cross-section. Apart from classification based on the sequence of the steps, presence of metal and process temperature are also taken into account while addressing the process. Front-end process means processes that can take place at high temperatures (>450 ^{o}C) in the absence of metal in the circut/device which is being processed. Back-end process is where the procesing is done at low temperatures (<450 ^{o}C), which can also allow metals present in the circut/devices during processing.

Front-end integration

Since photonics and electronics can be fabricated in the same material, i.e., silicon, integrating them in the same level seems a natural solution. Front-end integration has many advantages, such as doping and metalization steps that can be shared between electronics and photonic circuits. However, there are some limitations. First of all, the electronic circuits have to be re-designed to create real estate for the photonic circuit. Secondly, light-chip coupling is an issue. Horizontal coupling cannot be achieved as the transistors have to be protected from contamination, while vertical coupling can be an issue as the metals conceal the device, which

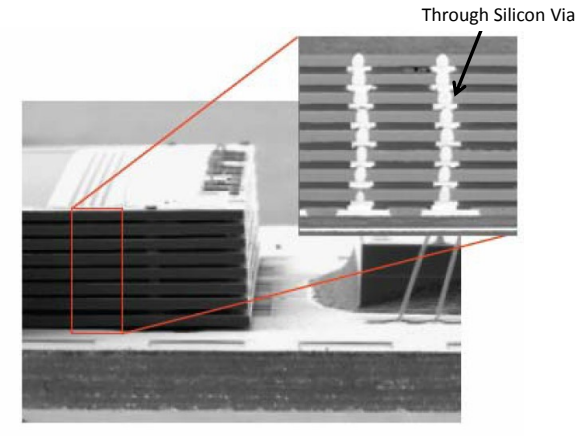


Figure 1.8: Scanning electron microscope image of a 16GB RAM built through 3D integration of eigth 2 GB RAM chips [Samsung].

might require further design and fabrication changes. Despite these challenges, recently, a data communication cable has been commercialised in silicon photonics by Luxtera. This company used a modified 0.13 μm CMOS fabrication process [73]. Two key technology demonstrations are a 20 Gb/s optical transceiver [71] and a 10 GHz optoelectronic oscillator.

Back-end integration

Isolating the photonic and electronic circuit design allows independent circuit developments. By integrating photonics on top of the electronic circuit, e.g. using low temperature deposited layers, the fabrication and design process of both can be partially decoupled. The integration density of both levels can be increased independently. Since the photonic circuit is at the top level it can be easily accessed through grating couplers. There are two primary factors that need to be addressed. Firstly, the photonic circuit layer cannot be built in crystalline material, hence an alternative material with low-loss is required. And secondly, the processing temperature should be limited to $< 450\ ^{o}$C. As mentioned earlier, deposited silicon is an ideal solution to back-end integration. Since the process temperature is restricted ($<$450 ^{o}C), fabrication of carrier injection modulators cannot be carried out in a straight forward way. Instead of heating the whole wafer, laser annealing can be employed to form a junction without causing damage to underlying CMOS [74, 75].

3D-integration

Unlike front-end and back-end integration schemes, 3D integration decouples the process and design of electronic and photonic circuit layers almost completely. As the transistor dimensions are approaching their physical limitations, 3D integration is considered as the next step to increase transistor density in the microelectronic circuits [76, 77]. The scheme relies on stacking of multiple chips on top of each other, which are then electronically connected using Through-Silicon Vias (TSV) (Fig. 1.8). The same scheme can be employed for stacking electronic and photonic wafers. One of the attractive aspects of this approach is that the fabrication of photonic and electronic chips can be done independently. The only constraint is that the placement of the TSVs should overlap between the two levels. Since the photonic layer can be placed on top of the electronic chip, light can be easily coupled to the photonic circuit through grating couplers. Furthermore the level of integration is scalable: multiple chips in several different materials platforms can be integrated. At imec 3D-integration is not only explored for microelectronics scaling but also for electronics-photonics integration [78]. Development of this technology is currently the focus of A. Masood.

1.5 Overview of this work

In this work, we address the challenges discussed above along two major lines: we investigate the possibilities and performance of a high volume manufacturing process for delivering high quality photonic devices and circuits with good uniformity and reproducibility. And secondly, we explore an alternative high refractive index material platform for photonic circuits and electronic-photonic integration.

In chapter 2 we present a brief overview of the most relevant fabrication steps for realizing silicon photonic circuits. In addition to this overview, chapter 2 also introduces the fundamentals of optical lithography and the dry etch process which will be used in this work. In chapter 3, the details of a new fabrication process based on 193 nm optical lithography and an advanced dry etch process for realizing photonic wires and photonic crystals in a 220 nm thick SOI wafer are presented. The fabrication process was aimed at delivering low-loss waveguides. We also present the characterisation results for these waveguides and for photonic crystals waveguides. Furthermore, we present different post-patterning loss reduction techniques.

In chapter 4, we study the process and device uniformity of the fabrication process developed in chapter 3. Extensive thickness and line-width characterisations were carried out to identify and understand the source of non-uniformity observed. Specific circuits were designed to study the non-uniformity of wavelength selective device non-uniformity both in short (within a die) and long distance ranges (within

a wafer). In this chapter, we propose a fabrication process flow route, which could potentially reduce the non-uniformity through integrating both design and fabrication databases.

In chapter 5, we present an alternative wafer technology for realizing high efficiency fiber-chip grating couplers. We present a flexible wafer stack technology, where the core thickness can be tuned irrespective of the starting SOI wafer. Using this technology we have demonstrated photonic components with different core thickness: high efficiency fiber-chip grating couplers with a core thickness of 380 nm and low-loss photonic wire waveguides with a core thickness of 220 nm.

In chapter 6 and 7, we present an alternative high index contrast material platform. We investigated three materials: silicon dioxide, amorphous silicon and polycrystalline silicon as the cladding and core materials for these waveguides. Extensive material studies were carried out to identify suitable material properties for photonic devices. The process is designed to allow the realization of back-end electronic-photonic integrated circuits. In chapter 7, we present optically coupled multilayer silicon photonic circuits using deposited silicon. Various optical via schemes are studied. Finally, in chapter 8, a summary of the work with future perspectives is drawn.

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2

Introduction to Fabrication Technology for Silicon Photonics

2.1 Introduction

Circuit patterns can be defined in many ways. In general, they can be fabricated by using two methods: indirect or direct patterning. Figure 2.1 shows various techniques of patterning based on this classification. In an indirect patterning process, the circuit pattern is first transferred into an intermediate material (resist) and then transferred into a desired material by using an etch process. In a direct patterning process, the patterns are directly defined in the material. These two methods can be further classified as writing and printing techniques. Figure 2.1 illustrates some of the patterning techniques used in the fabrication of photonic devices. The choice of the technique depends on the core material, for instance, diamond waveguides can be more easily made using a direct method (ion beam milling) than other methods. On the other hand, Si photonic devices can be fabricated using a wide range of techniques. However, most of them are not compatible with the high volume CMOS fabrication process.

With indirect patterning technique, dry etching is used to transfer circuit patterns into a desired material. It provides a reliable patterning with high fidelity. Moreover, dry etching is an industrial standard for pattern transfer in CMOS fabrication, which suits our primary requirement.

In the following sections, we discuss different pattern transfer techniques and their suitability for Si photonics. In particular, optical lithography and dry etching fundamentals are discussed in more detail.

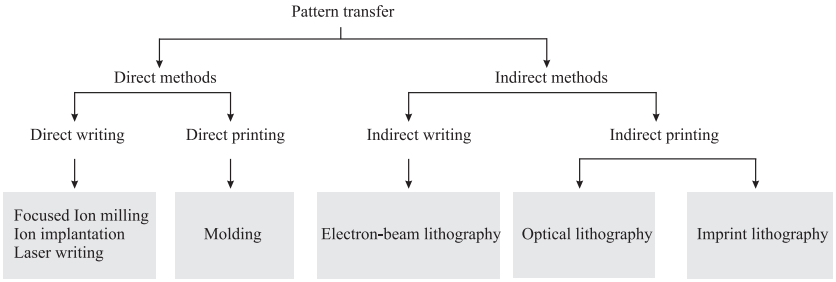


Figure 2.1: Classification of pattern definition techniques.

2.2 Focused Ion beam milling

Focused ion beam (FIB) milling is a physical process of removing material using high energy ions. Generally, liquid gallium is used as an ion source. By controlling the direction and spot size of the ion beam, desired patterns can be milled with high accuracy. Since the process does not require a physical mask on the surface of the core material, it is classified as a direct writing method. In principle, any material can be milled using FIB, which makes it one of the most versatile pattern definition techniques. Both 2D and 3D structures in Si have been demonstrated using FIB milling [1, 2]. Despite its advantages, it is not widely used for Si photonic device fabrication due to two primary reasons. Firstly, the milling process is inherently destructive, creating lattice disorder and ion contamination in the core material, which results in high absorption loss. And secondly, the writing process is slow with small writing field, which limits its application to ”proof of concept” devices and post-fabrication trimming [3, 4].

2.3 Electron beam lithography

Electron beam lithography (EBL) is an indirect writing method, where an electron beam is used to chemically modify an electron sensitive material (called resist) with the desired circuit pattern. The pattern in the resist is then transferred it into the desired material using dry etching. By scanning an electron beam over the resist material it can be either made soluble or insoluble depending on the nature of the resist (positive or negative). The remaining part of the resist is used as an etch mask for the etching process.

Due to its high resolution capabilities e-beam lithography is considered as a benchmarking tool for pattern definition. Even though high resolution pattern definition is achieved with the help of EBL, resist material also plays an equally important role. Some of the e-beam resists that are being used for fabricating Si photonic devices are poly methyl methacrylate (PMMA), methyl acrylate resins (ZEP series) and Hydrogen silsesquioxane (HSQ). For a given electron beam configura-

tion, the resolution of the pattern depends on the resist quality. The resolution of the resist is determined by its chemical composition. The e-beam resist chemistry is under constant development for advanced microelectronic device demonstrations. Silicon photonic, takes advantage of these developments where high resolution is one of the prime requirements. Even though some of the e-beam resists are sensitive to deep-UV light recent high resolution HSQ and ZEP are not, hence they cannot be used in a high volume deep-UV lithography process.

Since e-beam lithography is a relatively affordable tool for academic research, it is widely used by the Si photonic research community. By using e-beam lithography low loss single mode photonics wires (1 dB/cm) were demonstrated [5] using HSQ, which is believed to be a consequence of smooth sidewalls of the photonic wires and also it should be noted that the dry etching process also equally contributes to the loss reduction. Even though 1 dB/cm is now used as the benchmark for photonic wire loss, in literature, the propagation loss is scattered between 1-6 dB/cm [5–8]. A detailed table can be found in chapter 3. Even though one of the requirements (chapter 3) is met with the e-beam lithography, no reports were found on the uniformity of Si photonic devices either within a die or wafer, which is one of the prime requirements for larger volume manufacturing. However, it has been reported that by optimising the EBL writing process, devices could be matched within an accuracy of 25 pm [9].

Despite these demonstrations, e-beam lithography is not yet considered as a mainstream manufacturing tool for integrated circuit. This is mainly due to two fundamental issues. Firstly, the process is slow as a single electron beam is scanned over the substrate surface, which results in low throughput. Since the beam can only be deflected over a certain surface area, the wafer stage has to be moved for further patterning, which results in stitching(alignment) errors. However, EBL is widely used for telecom laser fabrication in large volumes. In order to address the issue of field of view issue, efforts have been made to overcome these issues by using parallel e-beams [10, 11].

2.4 Imprint/nano-imprint lithography

Imprint or nano-imprint lithography is a process of pattern transfer using physical force. Mainly pursued as an alternative fabrication route for sub-45 nm node CMOS circuits, its application is widespread. Imprint is essentially a moulding technique, which requires a pre-fabricated mold for pattern transfer. The mold is usually made by using a writing technique such as e-beam lithography. The pattern in the mold can be either directly imprinted in the material or indirectly through a soft resine. In case of direct imprint, the mold is pressed against the substrate and an external force is applied to transfer the pattern. In case of a polymer, gentle pressure is adequate, however, intense heat is required to deform Si. It has been demonstrated that by using a high power excimer laser Si can be patterned by direct imprint [12]. Typically, apart from polymers, indirect patterning is used. In the indirect imprint process, the mould is pressed against a soft curable resin to

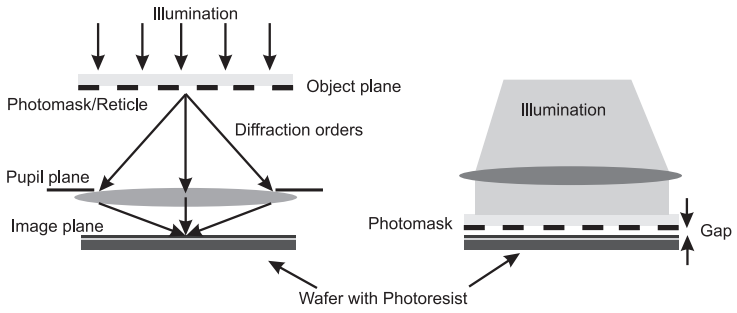


Figure 2.2: General optical lithography process diagram (Left) Projection and (Right) Contact/Proximity.

take the form of the mold and then irradiated with light to freeze the structure. Dry etching is then used to transfer the pattern from the resin to the substrate.

Nano-imprint lithography is a cost effective patterning technique. In the presence of a high resolution mold, nano-imprint lithography is considered as a high resolution and high throughput technique. Various photonic devices in silicon have been demonstrated using nano-imprint lithography, including wavelength selective photonic wire structures and photonic crystals [13]. Despite these demonstrations, this technique is yet to be qualified for large volume manufacturing with good reliability and scalability. In addition, poor pattern fidelity of this technique fails to meet the requirements for silicon photonic devices. However, they are used to fabricate non-planar components [14]. More details on nano-imprint lithography and its application for photonic device fabrication can be found in the doctoral disseration of Dr. S. Scheerlinck [13].

2.5 Optical lithography

Optical lithography is the most widely used patterning technique. Being an indirect printing technique, it requires a predefined pattern called photomask for patterning. By illuminating the photomask, the image from the mask is transferred into a photo-sensitive material called photoresist, which is coated on a substrate. The pattern is then transferred into the substrate by using dry etching. The process mentioned above is the same for all the optical lithography systems, including advanced immersion and extreme ultra-violet lithography systems.

In general, optical lithography can be classified into three categories; contact, proximity and projection lithography. The classification is based on the placement of the photomask with respect to the substrate surface. Figure 2.2 illustrates the patterning technique of different systems. The choice for a given lithography technique is made based on practical and technological requirements.

2.5.1 Contact and Proximity Lithography

Contact lithography is the oldest but still widely used printing technique. As the name implies, it is a contact process wherein the photomask is pressed against the resist-coated substrate and exposed with suitable wavelength light (Fig.2.2). Contact lithography results in defects in both the photomask and substrate surface. In order to avoid this damage a small gap between photomask and substrate is some times introduced, which is then called proximity printing.

In proximity printing, a small gap (5-10 μm) is left between the mask and the substrate. In this mode, the fresnel diffraction from the photomask is used for patterning. Proximity lithography traditionally relied on 365 nm (I-line) and 436 nm (g-line) wavelengths for illumination. These wavelengths are the distinct wavelengths of a mercury vapour lamp. Due to large gap between the substrate and the mask the pattern resolution was not as good as contact printing, hence shorter wavelengths were used for patterning. Using shorter wavelengths, a 500 nm line can be printed with a gap of 200 nm. Similar results can be achieved by improving the photoresist process and novel technologies at larger wavelengths. It has been predicted that the resolution of contact lithography will surpass λ/20 periodicity (or $<$18 nm) [15]. It has been numerically shown that by using surface plasmonics features as small as 20 nm can be patterned using g-line [16]. However, these developments are not widely available as commercial systems, which limits contact/proximity lithography to micrometer scale patterning.

In photonics, it is often used for fabricating micrometer-scale devices in polymer and large core silicon photonic devices. Even though reasonable resolution can be achieved with contact/proximity lithography, it requires flat surface. Nevertheless, contact/proximity printing is widely used for low resolution post-fabrication processes, such as an etch window for under etching and resistive heaters.

2.5.2 Projection lithography

Among the optical lithography techniques, projection lithography is the most successful high volume manufacturing technique. It is an extension of proximity printing system with reduction/projection optics between the mask and the wafer. Figure 2.2 shows a simple projection system. In the projection system, the photomask is illuminated with light of a desired wavelength, which in turn creates diffraction orders. The diffraction from the photomask is then collected by the projected system and the image is formed on the wafer surface. The image formed on the wafer surface is referred to as aerial image. The main advantage of a projection system is that the mask can be reused without damage. Further more, the mask image can be 4-5 times larger that the actual pattern, which reduces mask fabrication complexity and defects.

The two major projection lithography configurations used in a high volume manufacturing environment are stepper (”step and repeat”) and scanner (”step and scan”) systems (Fig. 2.3).

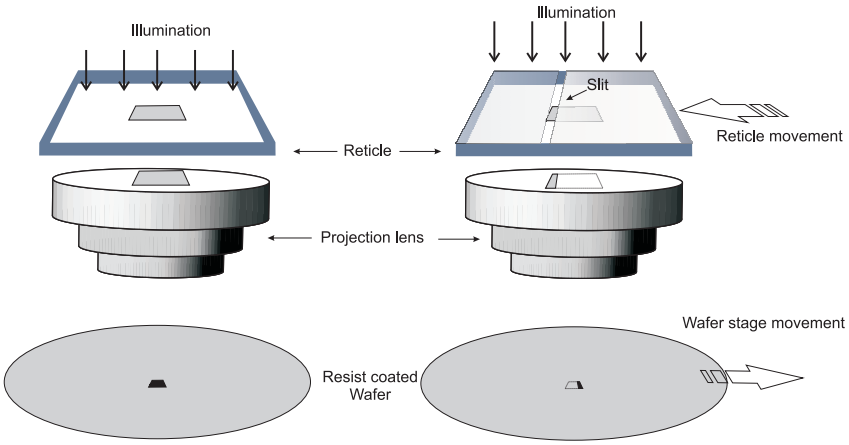


Figure 2.3: comparison of stepper and scanner systems.

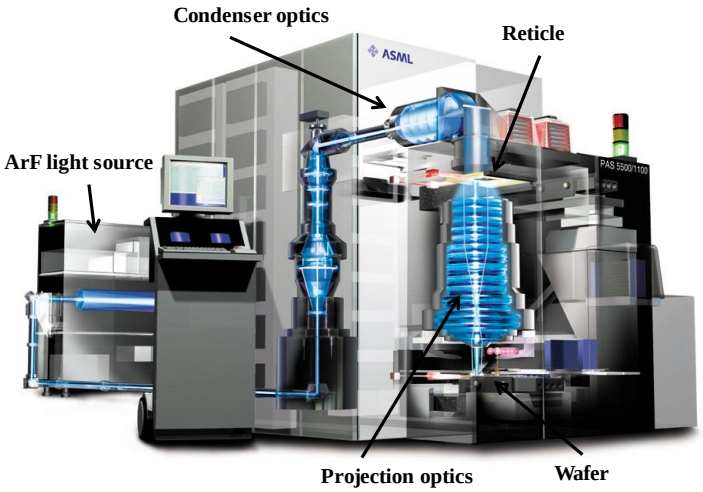


Figure 2.4: ASML PAS5500/1100.

2.5.3 Stepper System

The stepper (or step-and-repeat) system is an improved proximity printing system with reduction/project optics between the mask and the wafer.

With projection printing only a portion of the wafer is exposed with the full mask field. After each exposure, the wafer is moved and the operation is repeated until the total wafer area has been exposed (Fig. 2.3a). A typical size of the exposure field is 26×33 mm.

Since the whole mask (full field) is exposed, the effect of lens aberration and exposure energy (dose) variations is limited by the quality of the optics. Further more, the size of the field depends on the largest lens field with sufficient imaging quality. Despite full field exposure the throughput of a stepper system is lower than a scanner system. One of the main reasons is the exposure time required to reach the dose levels for the photoresists. However, these systems are still used in some production lines for manufacturing and research purposes.

2.5.4 Scanner System

In a scanner system, instead of a full field exposure, a slit is used to scan the mask exposing only a part of the mask field (Fig. 2.3b). The mask and wafer move synchronised until the entire mask has been projected onto the wafer. This technique allows to increase the image field width for a given lens size and reduces the lens aberration and dose non-uniformity issues. Since the scanner uses an exposure slit, the optics need a large field of view only in one direction. The scanner systems also deliver high alignment accuracy, thanks to a local alignment strategy, where by each chip can be individually aligned to the next mask level.

Figure 2.4 shows one of the advanced stepper systems from ASM Lithography, which was used for pattern definition in this work. The lithography process tools consists of four essential modules: the illumination system, the reticle, the projection optics, and the resist-coated wafer.

2.5.4.1 Illumination System

The illumination system consists of a light source and condenser optics. It is important that the source is able to supply highly monochromatic light with high intensity. Monochromaticity is important because the lens system supports aberration-free operation for only a very narrow wavelength band. The light at 193 nm is generated by an argon fluoride excimer laser (ArF) with a bandwidth of 25 pm [17]. Intensity, on the other hand, ensures high throughput by reaching the necessary dose faster. Intensity uniformity is another important property of an illumination system, which is achieved by using Köhler's configuration [18]. In Köhler's configuration, each point in the source creates a plane wave illumination of the mask, provided good condenser lenses are used. In addition, condenser optics create the required amount of spatial coherence of the light and perform spatial filtering. The spatial filter is used to form different source shapes in order to increase the pat-

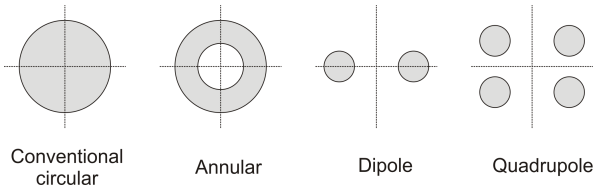


Figure 2.5: Widely used illumination source schemes.

tering resolution [19]. Figure 2.5 illustrates some of the widely used advanced illumination schemes. In addition to the wavelength, these illumination schemes can further improve image quality at the expense of directionality. Hence, when pattering two dimensional structures, such as rings, pattern fidelity can become seriously impaired when using these special illumination schemes.

In this work, we have concentrated only on the conventional circular illumination, which guarantees same pattern quality in all directions. A simple example would be a ring resonator, which has a circular pattern extending in two directions. Since photonic circuits always consist of combination of patterns, special illumination schemes cannot be used. Exception could be for patterning gratings all oriented in one direction.

2.5.4.2 Reticle

The term reticle or photomask refers to a glass plate covered by a film of chromium, which controls the light transmitted through the glass plate. The chromium layer contains the circuit pattern that will be transferred on to the wafers. The quality of the mask and its durability are of critical importance, since defects on the mask will be transferred on to the wafer along with the desired patterns. The resolution of the mask depends on the writing technology and the type of mask (binary, alternating phase-shift, attenuated phase-shift, etc.). Figure 2.6 illustrates the two most widely used mask technologies and their effect on the aerial image on the wafer surface. Binary masks are the simplest and least expensive of the different types of mask technologies, where light transmission is simply controlled by opacity. In advanced mask technologies, such as alternating and attenuated phase shifted masks, the light contrast is controlled by a combination of opacity and phase (Fig. 2.6). Undoubtedly, advanced mask technologies provide a better aerial image at the expense of design complexity and high price tag. In this thesis, we used binary masks fabricated using e-beam technology, similar to 180 or 130 nm technology node reticles. The mask quality, such as accuracy and uniformity of the patterns at the mask level, increase with the decrease in technology node.

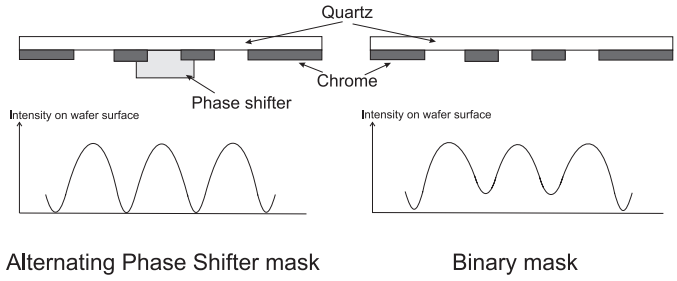


Figure 2.6: Areal image of binary and alternating phase shift mask.

2.5.4.3 Projection Optics

The projection optics consist of complex arrangement of 25-40 glass lens elements providing a reduction factor of $4\times$ or $5\times$. High reduction factor means shrinking the size of the illumination projected field, but it would also minimizes the sensitivity to mask defects and makes mask writing process easier. The light (λ) passing through the mask is spatially diffracted as shown in figure 2.2. These diffraction orders propagate at a small angle for isolated patterns and at large angles for dense patterns on the reticle. A pupil filter that is located in the projection optics allows spatial control of the diffraction orders. This pupil filter is otherwise referred to as numerical aperture or NA of the projection system. The transmitted diffraction orders are then recombined on the wafer surface forming the desired pattern. The NA of an optical system can be given as,

$$NA \; = \; sin\,(\theta) \tag{2.1}$$

Where θ is the acceptance cone angle of the lens. The number of diffraction orders from the mask passing through the lens can be controlled by increasing or decreasing the acceptance angle. Resolution of an optical projection system is determined by the size of the minimum resolvable feature, and it is limited by the NA. Here resolution means pitch or period of a periodic structure. Theoretically, an isolated feature produces a continuous spectrum of diffraction orders such that some of them always pass through the pupil. This essentially means isolated structures like photonic wires can be resolved irrespective of their dimension. On the other hand, periodic structures like photonic crystals and gratings diffract a finite set of diffraction orders at an angular interval of $\frac{2\pi}{P}$, where P is the pitch. Since at least two diffraction orders are required to resolve the pattern on the resist surface, the minimum resolvable pitch is determined by the NA of the projection system. Hence, for a coherent light source the minimum pitch can be given as [20],

$$P \; \propto \; \frac{\lambda}{NA} \tag{2.2}$$

Where, λ is the wavelength of the illuminating light source. The spatial coher-

ence created by the illumination system and NA of the projection system result in a factor called partial coherence. The partial coherence factor (σ), gives the relative size of the source image in the pupil plane with respect to the size of the pupil and it is given as,

$$\sigma = \frac{R_s}{R_{NA}} \tag{2.3}$$

Where, R_s is the radius of the source image and R_{NA} is the size of the pupil filter (Fig.2.2) as measured in the pupil plane. With the introduction of σ, the minimum printable pitch P_{min} can be then be modified from Eq. 3.1 as [21],

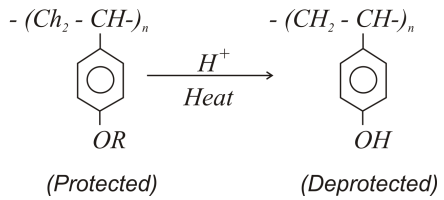
$$p_{min} \propto \begin{cases} \frac{\lambda}{NA}, & for\ \sigma = 0 \\ \frac{\lambda}{NA}\frac{1}{1+\sigma}, & for\ 0 < \sigma < \infty \\ \frac{\lambda}{2NA}, & for\ \sigma = \infty \end{cases}$$

In addition to NA, σ adds another degree of freedom in resolution improvement. Large value of σ benefits dense structures, while small values are preferred for isolated structures. Larger σ also helps to reduce proximity effects. Hence, the choice of the illumination settings NA and σ depends on the type of structure to be printed.

2.5.4.4 Photoresist

The reconstructed image on the wafer surface is transferred into the photoresist through a photo-chemical reaction. The photoresist is a photosensitive organic polymer, whose solubility can be changed by photons. In advanced lithography processes (193 nm and higher), the photo-chemical reaction is amplified by an additive called photo-acid generator (PAG). A simplified process of pattern definition is shown in equation 2.4 and 2.5. When illuminated by a photon, the PAG present in the photoresist generates protons (H^+). The generated protons upon heating (catalyst) break the polymer chain resulting in a deprotected and soluble material. Hence, after exposing the desired pattern on the photoresist the wafer is baked at a desired temperature in order to deprotect the polymer. The deprotected photoresist is then removed by a wet chemical etch process.

$$PAG \xrightarrow{h\nu} H^+X^- + Byproduct \tag{2.4}$$



(2.5)

Photoresists are available in two forms, positive and negative tone. Positive tone photoresists become soluble upon exposure of light, while negative tone is stabilized on exposure. It is well known that due to diffraction effects, the aerial image produced by an open mask surface (space) is better than the image produced by opaque mask area (line) and therefore, positive resists are preferred in practice [20]. Resist contrast and thickness are also important to achieve a good quality patterns, which depends on the photo material and process parameters.

2.6 Dry etching

Etching processes are used to partly remove material in order to create patterns to obtain the desired device geometry. They are used in conjunction with photolithographic techniques to transfer a desired circuit pattern into the substrate. Particles in the etchant remove material by attacking the exposed surface. The material may be removed isotropically, as often encountered in chemical or wet etching, or anisotropically for which a dry etching process is used. An isotropic etch is a situation where the etch rate is equal in both vertical and horizontal direction. In contrast, the situation where the vertical etch rate is higher than horizontal etch is termed as anisotropic[1]. Dry etching in general refers to plasma based etching. The constituents of the plasma, namely, reactive radicals and charged particles, engage directly or indirectly in the etching process. The fundamental idea behind dry etching is to form volatile chemical products of the material that needs to be etched.

One of the prime requirements for a plasma etch process is to generate a plasma and sustain it for a reasonable duration. Even though there are various ways to generate a plasma, for dry etching, it is usually generated by electrical discharge. Figure 2.7 illustrates a simple plasma reactor/chamber used for dry etching. A plasma is generated between the two electrodes by applying a sufficiently high voltage between them. In a plasma, the gas molecules are dissociated into neutrals and charged particles, which emits a characteristic glow. The surface of the substrate is exposed to the reactive radicals generated in the plasma, which can form volatile products that evaporate resulting in etching process. In the following section, we will discuss the etching process more in detail.

2.6.1 Etch mechanisms in a plasma

Etching in general can be done in two ways, either by a chemical or a physical mechanism (Fig.2.8). As mentioned earlier, the main philosophy behind etching is to create volatile products. The physical process of etching is also known as sputtering, where by highly energetic ions from the plasma are directed onto the surface to eject atoms from the bounded surface.The Chemical mechanism, on the other hand, converts the substrate material into a volatile product with a high

[1] Some wet chemicals, for instance, potassium hydroxide (KOH) etches Si anisotropically. In this case, it is not a directional etch, but a preferential etch to a particular crystal orientation.

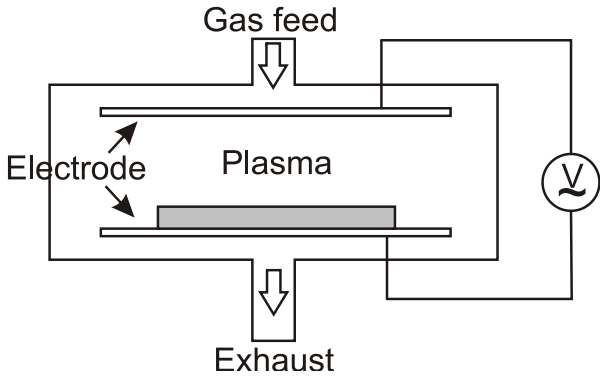


Figure 2.7: A simple reactor which can be used for plasma processing.

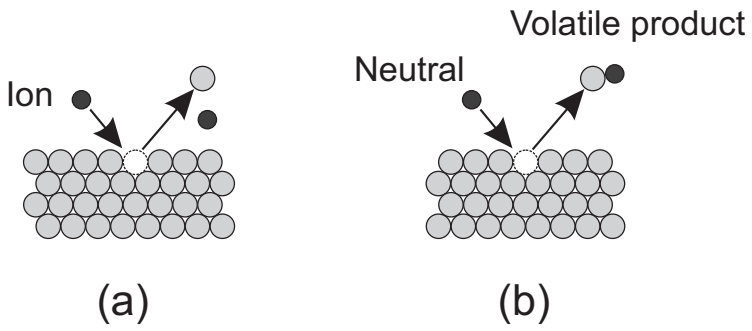


Figure 2.8: Schematic of two etch mechanisms (a) physical sputtering and (b) chemical etching.

vapour pressure to facilitate material removal. In addition to chemical and physical mechanisms, ion-enhanced etching is considered as another etch mechanism. It is a combination of a chemical and physical etch process. When a neutral radical is not capable of forming a volatile product on its own, energetic ions may modify the surface assisting the etch process [22].

In sputtering, the atoms or molecules that are ejected from the surface should not return to the surface to achieve a net material removal. To achieve this, a low operation pressure is required, where the mean free path (MFP) is comparable or larger than chamber size. If the MFP is short the ejected product collide in the gas phase and redeposit on the substrate surface inhibiting the etch process. As a mechanical process, sputtering lacks selectivity between the mask and the substrate. It is sensitive to the bonding force and surface structure, rather than to its chemical nature. It can sometimes etch different materials at a similar rate. On the other hand, the highly energetic ions from the plasma are highly directional, which allows anisotropic etching. Anisotropic etch refers to differential etch rate

in vertical and horizontal directions. Despite the lack of selectivity, sputtering finds application in conformal material filling when combined with a deposition process (see chapter 6).

In chemical etching, gas phase ions react with a surface molecule resulting in a volatile molecule. A classical example is the formation of the volatile SiF_4 molecules when fluorine (F) is used to etch Si atoms. The primary purpose of a plasma in chemical etching is to generate etchant species, F-radicals in this example. In the plasma, etchant (F) species are generated by dissociating the feed gas (e.g., F_4, NF_3 and CF_4) through collision with high energy electrons.

Chemical etching is the most selective etch process, since the chemical reaction is sensitive to bonds and elements involved. Despite its high selectivity, the process is usually isotropic. Isotropic etch refers to equal etch rate in vertical and horizontal directions, which makes it impossible to form fine narrow structures.

2.6.1.1 Directional etching

In most of the silicon photonics applications an anisotropic etch profile is desired. However, this cannot be attained either with sputter or chemical etching alone. One of the main issues with sputtering is non-selective etching, the mask material would etch at the same rate or even higher rate in case of a soft mask like photoresist. Hence, the thickness of the mask required can be a multiple thickness of the etch depth required. Chemical etching, on the other hand, is very selective. However, due to anisotropic etch the etch process always results in mask undercut. In order to attain the desired etch profile, a combination of etching processes is required. Directional etching can be achieved by using high energy ions and etch by-products. Figure 2.9 illustrated the mechanism of a directional etch process. The directionality is achieved by a sidewall inhibition or passivation layer. The horizontal etch is arrested by depositing a thick layer of a chemically resistant compound on the sidewall surface. The composition of the passivation layer determines the chemical and physical (thickness) nature. The constituents can originate from different sources; resist material, feed gas, and etch by-product. The properties of the passivation layer can be controlled by the constituents. More details about the passivation layer and its role in achieving an anisotropic etch profile is elaborated in Chapter 3.

2.6.2 Etching chambers

The choice of hardware and chemistry for dry etching strongly depends on the requirement, such as a research or a volume production environment. The requirement might vary from manual, large batch, high pressure, barrels; to computer-controlled, single wafer, low pressure, complex etcher. The design of an etch chamber is not only aimed at generating the plasma but also to manipulate the plasma. In a CMOS fabrication process, the two major type of dry etching reactors utilized are capacitively coupled and Inductively coupled Plasma etchers. In the following section, we will briefly discuss these two reactors and their use.

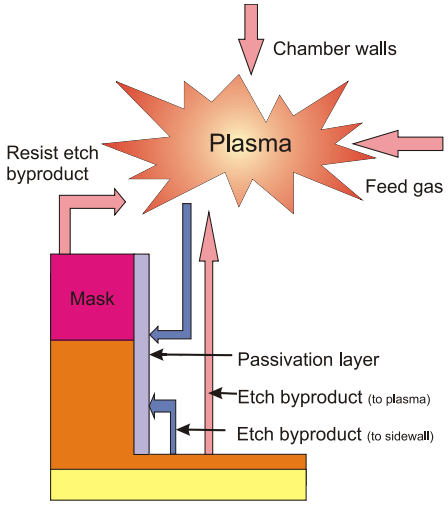


Figure 2.9: Illustration of anisotropic dry etching using sidewall inhibitor.

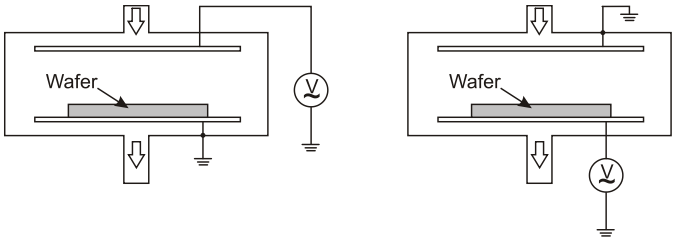


Figure 2.10: Schematic diagram of a simple (Left) Plasma etcher and (Right) reactive ion etcher.

2.6.2.1 Capacitively Coupled Plasma reactor (CCP)

The Capacitively Coupled Plasma (CCP) etcher is the simplest form of dry etch tools. In a CCP reactor, a plasma is generated between the two parallel plate electrodes which are coupled to an RF energy source. A CCP etcher can be operated in two modes; anode loaded and cathode loaded (Fig. 2.10). In an anode loading etcher, the wafer rests on the ground electrode, while it is placed on the generator electrode in a cathode loaded etched. An anode loaded CCP is called plasma etcher and cathode loaded CCP is called as a reactive ion etcher. In addition to loading the size of the electrodes are also different in these two systems.

A plasma etcher is often used for non-critical pattering. Since the ion energy is low and hence the etch process is chemical, the process is very selective. In addition, the plasma etcher is a low damage process, thanks to the low ion energy.

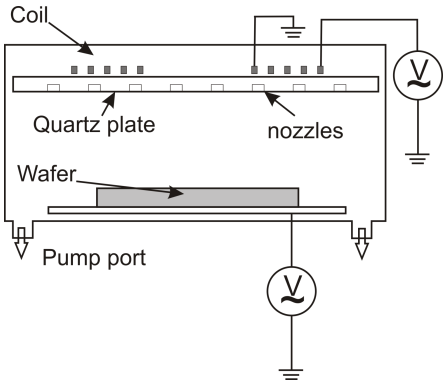


Figure 2.11: Schematic diagram of a simple inductively coupled plasm reactor.

However, the etching process is isotropic, which limits its application. Due to their low damage and selectivity,plasma etcher are commonly employed to strip photoresist after dry etching.

Reactive Ion Etching (RIE) is analogous to RF sputtering, where the wafer is placed on the RF generator electrode, usually operating at 13.56 MHz. By increasing the RF power, the ion energy and ion density can be increased. Anisotropic etching is achieved by increasing the ion energy. The more directional ions also increase the etch rate, which is vital for throughput. However, increased etch rate is overshadowed by low selectivity and plasma damage. These two disadvantages can be resolved by de-coupling ion energy and density. This is achieved by a applying an additional field in the form of an electric (Triode RIE) or magnetic (Magnetically enhanced RIE) field into the plasma. The additional field helps in increasing the ion density, while the ion energy is kept reasonably stable. Though these advancements partially resolve the issue, the hardware complexity and process design did not make them successful. However, RIE is still used in a CMOS fabrication process for dielectric and metal etching. Furthermore, it is used for deep high aspect ratio structures in micro-electromechanical systems (MEMS) with some process modifications, such as using an inorganic hard mask.

2.6.2.2 Inductively Coupled Plasma reactor (ICP)

The most practical solution for controlling ion energy and density independently is provided by an Inductively Coupled Plasma reactor (ICP). Figure 2.11 shows a simple ICP reactor. An ICP reactor consists of an inductive coil, which allows to control the plasma density. By passing current through the coils an alternating magnetic field is generated, which confines the electrons into the plasma. The confined electrons in turn produces a high density plasma. By applying a RF power to the wafer plate, the ion energy can be controlled independent of the plasma density.

Due to its flexible process control, most of the critical patterns in CMOS are fabricated using an ICP etcher. In this work, we have used an ICP etcher for all our device fabrication. The details about the dry etching process are elaborated in section 3.3.

2.7 Conclusion

In this chapter, we introduced various fabrication techniques for silicon nanophotonics. Among the patterning techniques, indirect patterning is identified as a suitable technique for high resolution pattern transfer. In particular, step-and-scan projection lithography systems have some distinct advantages over other patterning methods and it is the state-of-art technology used in microelectronics industry. The achievable resolution limit meets the requirement for silicon photonic circuits. In addition to the step-and-scan system, the inductively coupled plasma etch process is found to be the best suitable etching technique for silicon etching. It can provide a highly selective and directional etch process.

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3

Silicon Photonics device fabrication using advanced CMOS Technology

3.1 Introduction

Microelectronics fabrication technology is undoubtedly the most advanced pattering technology. It is also referred to as CMOS (complementary metal-oxide semiconductor) fabrication technology. The primary goal is to increase the device density, through miniaturization. Fabrication processes are constantly evolving to achieve required resolution without compromising throughput. In this work, we exploit these developments for Si photonic device fabrication. Even though the technology can be used as such, the requirements for Si photonics are very different from CMOS devices. As mentioned in chapter 1, Si photonic devices require extreme process control and uniformity of $\pm 1\%$ compared to $\pm 10\%$ in CMOS processes.

In this work, the 200 mm pilot line fabrication facility at IMEC, Leuven was used for the development of the fabrication process for silicon photonics. Figure 3.1 shows an overview of the fabrication process of a photonic wire (PhW) starting from a commercial silicon-on-insulator wafer followed by 193 nm lithography and dry etching. In the following section, we elaborate on the process development and optimization of the lithography and dry etching process to meet Si photonic device specifications. In addition to the experimental data, simulation of lithography processes were done using PROLITH, a photolithography process simulator.

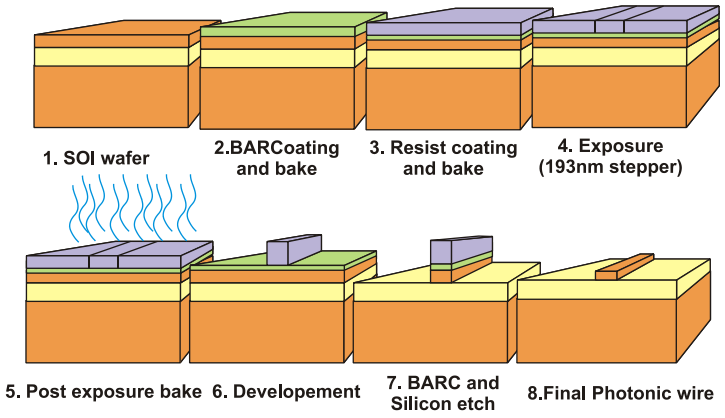


Figure 3.1: Fabrication process overview of a photonic device in SOI using 193 nm optical lithography.

3.2 193 nm optical lithography process

Despite tremendous improvements in the optical lithography systems, the overall process sequence had changed little compared to the material used in the processing. As shown in figure 3.1, first, the wafer is coated with an anti-reflective coating and photoresist. Since these two coatings consists of solvent diluted organic materials, they are baked to remove the solvent. The resist-coated wafers are then exposed with the image of the mask using a 193 nm ArF laser in a scanner. After exposure, the wafer is baked and finally developed to remove the exposed resist. The wafer is then taken for dry etching to transfer the pattern into Si.

All the lithography process steps can be classified into two sections: the illumanition process and the photoresist process. These two processes and their parameters determine the resolution, control and uniformity of the lithography process.

3.2.1 Illumination process

3.2.1.1 Numerical Aperture and coherence

The illumination parameters, numerical aperture (NA) and partial coherence (σ), are chosen according to the nature of the pattern (isolated or dense). In the lithography system that was used in this work, the NA can be varied between 0.5-0.74 and σ can be varied between 0.4-0.85. Since both isolated photonic wires and dense photonic crystals have to be patterned with a single exposure, the choice of these parameters has to be an optimal for both structures. As explained in chapter 2, photonic wires generate a continuous diffraction order, whereas a photonic crystal has discrete diffraction orders and requires sufficient NA to capture them for image formation. Figure 3.2 clearly shows the effect of NA on the aerial im-

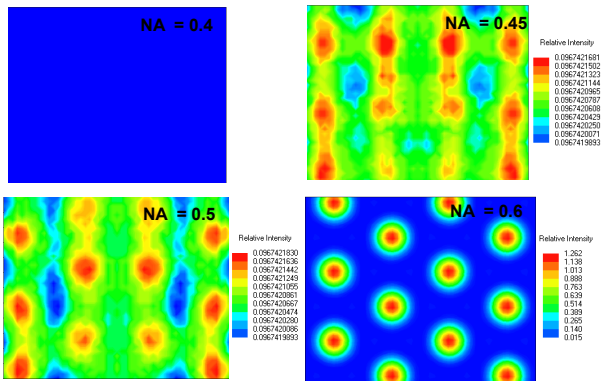


Figure 3.2: Simulated aerial image of a photonic crystal of 450 nm pitch/250 nm hole diameter imaged with a coherent light (σ=0) at different NA.

age of a photonic crystal. Due to insufficient diffraction orders, there is no image formed at low NA (0.4). When the NA increases the image starts to emerge and at 0.6 NA a good image contrast is obtained. We have also used other illumination settings to compare the effect on the process.

3.2.1.2 Exposure dose

Exposure dose can be defined as the light intensity available on the surface of the photoresist for imaging in the case where there is no mask pattern. The modulated light on the photoresist initiates a photochemical reaction resulting in pattern transfer. As mentioned in chapter 2 a sufficient dose is required to chemically modify and develop the full thickness of the photoresist. A too low dose can result in partial removal of photoresist inhibiting dry etching (Fig.3.3). The sidewall angle of the developed photoresist is also an important parameter. Especially for dry etching, where the photoresist sidewall will affect the pattern integrity. Ideally, the photoresist profile should have vertical sidewalls. The optimum dose depends on the properties of the photoresist, in particular, contrast and absorption.

Various factors influence the light intensity on the photoresist surface: illumination wavelength, reticle type and transmission, structure on the reticle, NA, and σ. Most of these factors are kept constant for a particular lithography process. In practice, optimum dose for a desired pattern is experimentally determined (Section 3.2.1.4).

3.2.1.3 Depth of Focus

The quality of the aerial image formed on the surface of the resist can become blurred because of focus offset. Depth of focus (DoF) is defined as the distance over which the image is adequately sharp. In other words, it is the tolerable movement in the image plane over which the structure is within a specified dimension.

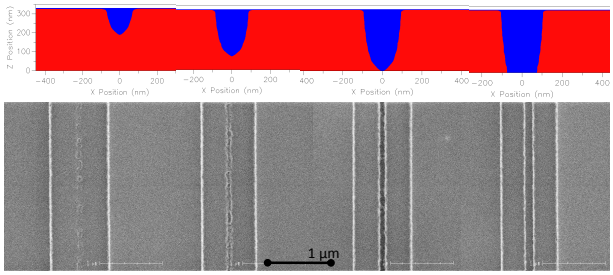


Figure 3.3: (Top) Simulated photoresist profile of a trench with increasing exposure dose and (Bottom) scanning electron micrography of the pattern on the photoresist.

It can be expressed as [1],

$$DoF = \pm k_2 \frac{\lambda}{NA^2} \tag{3.1}$$

Where λ is the illumination wavelength, NA is the numerical aperture of the projection optics and k_2 is the proportionality constant. Increasing the NA in an attempt to improve resolution (3.2.1.1) will result in a rapid decrease in DoF. The thickness of the photoresist also plays an important role in DoF at a given illumination setting. In an ideal case, half the resist thickness is the optimum focus plane. DoF should be accurately controlled to achieve good quality image despite resist thickness and topographic non-uniformity.

3.2.1.4 Focus-Exposure Matrix

A Focus-Exposure Matrix (FEM) is a process whereby exposure dose and focus are swept along the two axes of the wafer at a fixed NA and σ. By inspecting the pattern fidelity and feature dimension over the matrix, the optimal dose and focus can then be identified. The pattern fidelity degrades outside the optimal dose and focus. Figure 3.4 shows the simulated FEM. Figure 3.4a and 3.4b shows the effect of exposure dose and focus on the linewidth [1] and sidewall angle of a 450 nm photonic wire respectively. At an optimum dose $\approx$ 17 mJ/cm^2, the linewidth does not change with the focus shift (Fig. 3.4a), which cannot be true, unless the structure is specially designed. When comparing the sidewall angle map (Fig. 3.4b), we see that a vertical sidewall is only guaranteed for a limited defocus margin. Manual inspection of the feature is necessary to identify the best exposure conditions, since linewidth measurement alone can be misleading. Figure 3.5 shows an experimental result from a FEM of a PhW, where the pattern quality degrades from an optimum focus, while the pattern quality is preserved at an optimum focus despite dose variation. More details on using FEM are presented in section 3.2.3 and 3.2.4 for PhW and PhCs respectively.

[1] Linewidth: It is the distance between the two edges of a line(photonic wire).

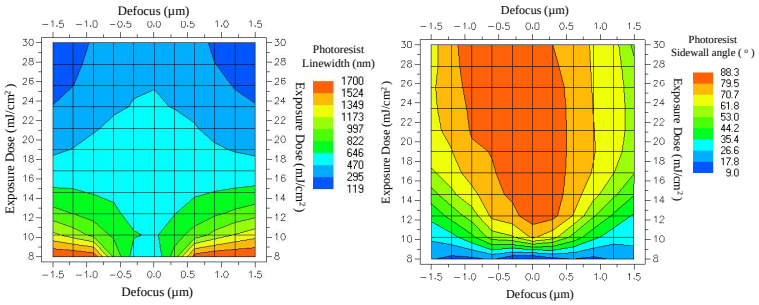


Figure 3.4: Simulated focus exposure matrix of a 450 nm photonic wire (a) linewidth and (b) sidewall angle.

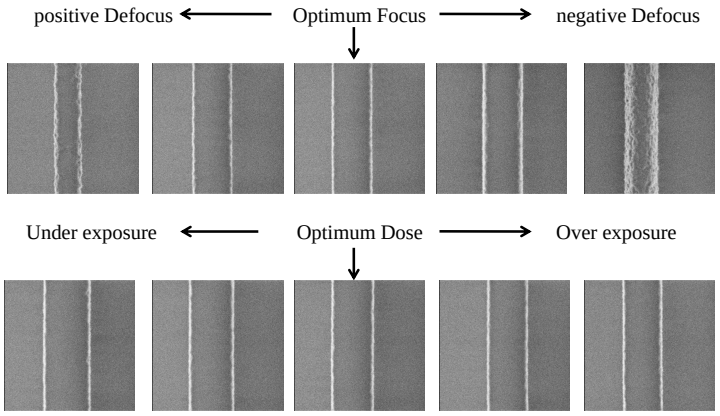


Figure 3.5: Top-down scanning electron microscope image of photonic wire from a focus exposure matrix (FEM) wafer.

3.2.2 Photoresist process

3.2.2.1 Photoresist and BARC

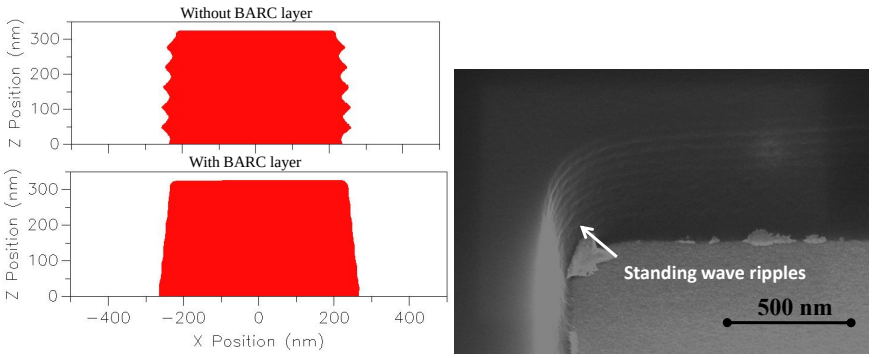
The type of photoresist determines the resolution of the pattern. In this work two positive tone chemically amplified photoresists were used; AR237J and AR1682J , which are used in front-end patterning for CMOS circuits. Since AR237J was phased out during this work, it has been replaced with AR1682J. Hence, process development results for both photoresists are presented.

In practice, for a given photoresist, the thickness is dictated by its etch resistance. High resolution can be achieved by using a thin photoresist layer, which requires an inorganic hard mask to transfer the pattern into Si. Since deposition and removal of the hard mask increase the process complexity a photoresist mask is chosen as an etch mask. We chose 330 nm as the photoresist thickness. The same thickness is used in the CMOS process for transistor definition (shallow trench isolation-STI)and the layer is thick enough to etch 220 nm of Si.

Photoresist alone is not sufficient for reliable imaging. When illuminated, the reflection from the substrate generates a standing wave pattern in the photoresist (Fig. 3.6). By adding an anti-reflective layer either at the top or bottom of the photoresist these reflections can be suppressed. In our case, we used an organic bottom anti-reflective coating (BARC) ARC29 to avoid reflection from the SOI substrate. The reflection from the substrate is suppressed by destructive interference of the light reflected from the substrate with the light reflected from the top surface of the BARC. In addition to reflection suppression, a BARC helps to reduce the critical dimension variation as a consequence of photoresist thickness variations. The light that is reflected from the substrate interferes constructively or destructively leading to a variation of the effective exposure dose in the photoresist. Figure 3.7a shows the linewidth variation of a 500 nm PhW for different photoresist and BARC thickness and figure 3.7b shows a line scan for three BARC thicknesses (60, 80, and 100 nm). It can be clearly seen from figure 3.7b that the linewidth follows a sinusoidal function for non-optimal BARC thickness. This variation in the linewidth with photoresist thickness is referred to as the swing curve. By using an optimal thickness of BARC the linewidth variation is reduced. From these simulations and experiments, we have chosen 330 nm and 77 nm as optimal thickness of photoresist and BARC respectively. Since any variation of this thickness can affect the linewidth uniformity, good thickness uniformity is maintained over a 200 mm wafer through regular process control. Details and characterization on the uniformity are presented in chapter 4.

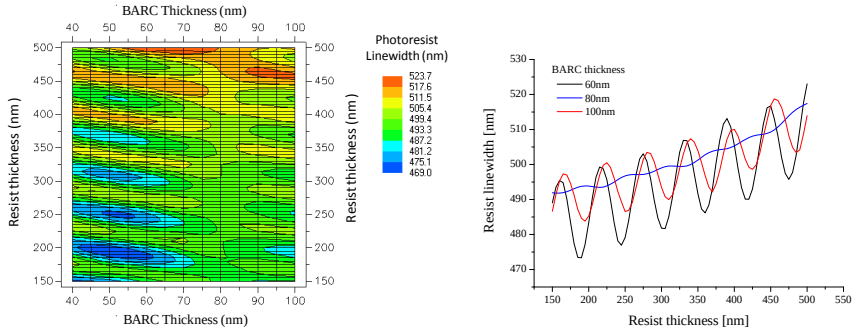
3.2.2.2 Baking and developement

Baking is one of the important steps in photoresist processing. After each coating (photoresist and BARC), the wafer is baked at an optimum temperature for an optimum duration. The baking temperature and duration are critical, since over or under baking can change the optical and physical properties of the material. These



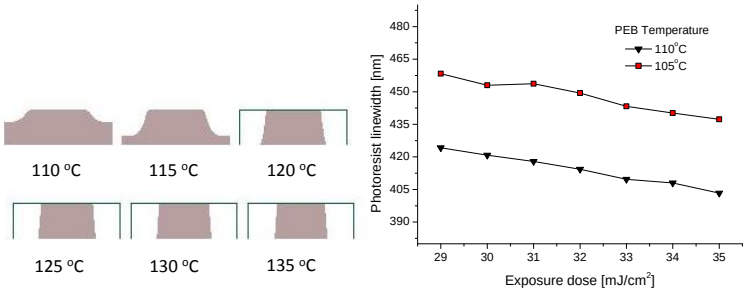
(a) (b)

Figure 3.6: (a)Simulated photoresist profile without and with bottom anti-reflective coating and (b) Scanning electron micrography of a standing wave formation on the resist without anti-reflective layer.



(a) (b)

Figure 3.7: (a)Simulated linewidth variation as a function of photoresist and BARC thickness variation and (b) Line scan .



(a) (b)

Figure 3.8: (a)Simulated resist profile for different post exposure bake (PEB) temperatures. The bake time and the development time were fixed at 60 seconds and (b) Experimental linewidth variation for two different PEB temperatures.

critical values are normally prescribed by the photoresist and BARC vendors. In addition, optimal operating points can be experimentally determined.

Among the baking steps, post-exposure baking (PEB) is one of the most important steps. The protons that are generated as a result of exposure react with the polymer to form a soluble product. This reaction is only possible in the presence of thermal energy, hence baking at an optimal temperature is essential (Fig. 3.8a). As can be seen in figure 3.8a an insufficient PEB temperature can lead to under development, while over baking does not notably modify the photoresist profile. However, increase in PEB temperature beyond an optimal point changes the feature dimension. In case of a PhW, the linewidth decreases as a function of PEB temperature due to enhanced proton diffucion (see chapter 2) . Figure 3.8b illustrates such change, where we experimentally observe a deviation of 7 nm/^oC. Hence closely monitoring the temperatures of the baking plates is necessary to achieve good process uniformity and reliability.

Development of the exposed photoresist is the final stage of the photoresist processing to transfer a 2D pattern from a reticle into a 3D structure in the photoresist. The de-protected photoresist after PEB is dissolved in an aqueous developer solution of Tetramethylammonium hydroxide (TMAH). The developer is dispensed on top of a spinning wafer. The amount of liquid dispensed and the rotation speed of the wafer determines the time required to dissolve and remove the photoresist. Insufficient duration or amount of developer will result in only partial development of the resist (Fig.3.9). Figure 3.9 also shows that the development process is non-linear hence an over-development would reduce the risk of partial resist removal and sloped sidewall angle. Since the BARC layer is insoluble in the developer it is removed during the dry etch process. Figure 3.10 shows one of the developed PhW structures in the photoresist with an optimum illumination and photoresist process.

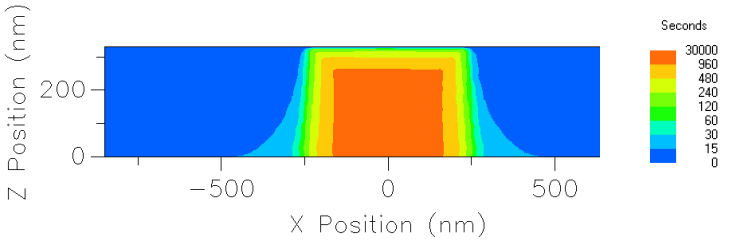
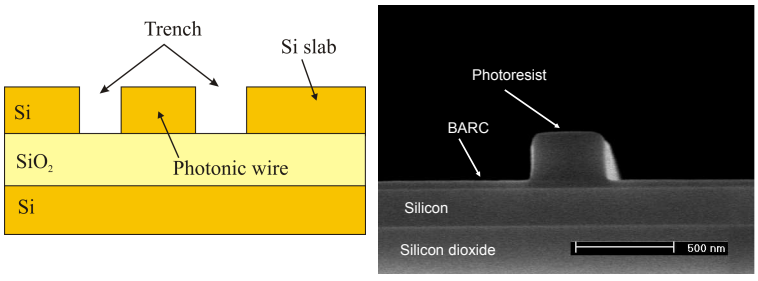


Figure 3.9: Simulated resist profile for different developement time.



(a) (b)

Figure 3.10: (a) Schematic of a photonic wire defined by making two trenches in the Si slab and (b)Resist profile after exposure and development.

3.2.3 Lithography process for Photonic wires

A 450 nm PhW, which is the basic component for most PhW circuits in this work, was taken as a test structure. The wires are defined by two trenches in Si slab (Fig. 3.10). The distance between the trenches defines the PhW width and the width of the trenches were sufficiently wide (≈ 2 μm) to optically isolate the wires from the lateral slab. This way of PhW definition allows contorl of the open area over the complete mask and also creates an uniform environment for all the PhW structures, which is vital for linewidth uniformity (see chapter 4).

The illumination setting for the PhW is chosen considering the multitude of structures printed along with the PhW, such as PhCs and trenches. Based on this requirement, a NA of 0.63 and a σ of 0.85 is chosen as an optimum illumination setting. The focus and exposure dose were optimised from a FEM (see section 3.2.1.4). Fig. 3.11 depicts the measured linewidth as a function of focus and exposure dose [2] for two kinds of photoresists. By changing the exposure dose, the PhW width can be varied from the design width (Fig. 3.12a) resulting in a wealth of information from a single device design. Since devices with varying linewidth have to be printed in the same circuit layer, good linewidth linearity is essential. With a single illumination condition, we could print linewidths from 150-500 nm without any dimensional correction hence achieving a linear response (Fig.3.12b). From these measurements, we extract the process window, which can be defined as the area in the parameter space, where the dimensional variation is within an allowed tolerance. The illumination parameters, mainly, focus and exposure dose can vary due to various factors, such as resist thickness, substrate reflectivity or lithography tool related issues. Hence a sufficiently large process window is necessary for a stable lithography process.

Fig. 3.13 shows the process window for a 450 nm PhW with $\pm 1\%$ linewidth variation or $\pm$4.5 nm. Any variation of exposure dose or focus within the shaded ellipse will not change the linewidth more than 1%. From this data, exposure latitude (EL) is extracted, which gives exposure dose tolerance for a specific linewidth tolerance at a given DoF. Figure 3.14 shows the percentage tolerance from the optimal exposure dose. At an optimum focus and exposure dose, AR1682J shows better exposure latitude (EL) in comparison to AR237J. An exposure latitude of 5% and 10% at 0.3 μm DoF was observed for AR237J and AR1682J respectively. Large EL compensates for dose variations as a result of reticle and illumination lens transmission variations.

The EL and DoF depend on the illumination settings, NA and σ. By varying these settings acceptable EL and DoF can be achieved. Figure 3.15 illustrates the effect of the illumination setting on EL and DoF for a 450 nm PhW. An increase in NA clearly shows an increase in EL, however with a decrease in DOF, which clearly agrees with the theory presented in chapter 2. Even though a NA of 0.6 and a σ 0.6 gives maximum values of EL and DoF it was not used for two main reasons. Firstly, this setting cannot be used for printing dense PhC patterns due to low σ and secondly, low σ can result in higher proximity effect. Hence, a NA of 0.63 and a σ of 0.85 is chosen as optimum for printing a variety of structures

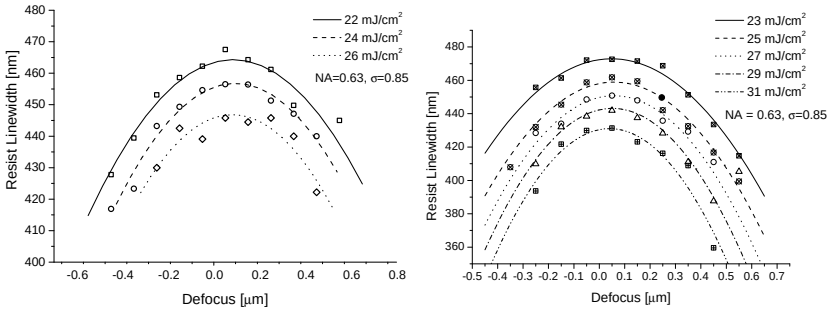


Figure 3.11: Bossung curve for 450 nm photonic wire photoresist linewidth in (a) AR237J and (b) AR1682J.

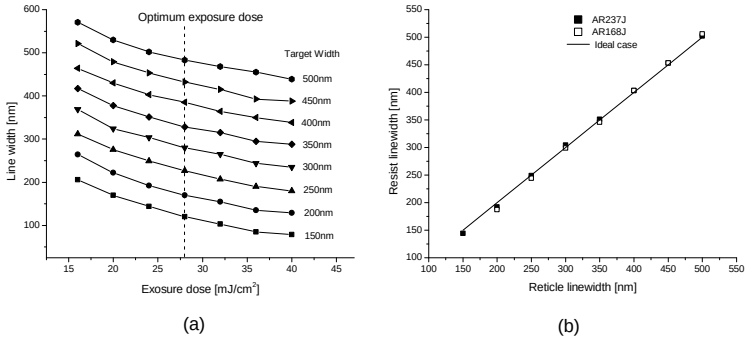


Figure 3.12: (a) linewidth as a function of exposure dose at optimum focus (NA =0.63, σ=0.85) and (b) Different linewidths can be printed on target without individual optimization. The process is optimized for 450 nm photonic wire which shows high linearity.

with acceptable DoF and EL. The choice of the illumination settings and their implications for printing PhWs and PhCs together is presented in section 3.2.5.

3.2.4 Lithography process for Photonic crystals

Photonic crystals are very challenging structures to fabricate by optical lithography. Especially, PhCs with a triangular lattice, where the pitch of the crystals varies in two directions. In CMOS circuits, two dimensional arrays of circular holes are used for contact holes. However, the density of such structures is typically much lower than for PhCs. PhCs can be used either in a square lattice configuration or a triangular lattice configuration. In this work, we concentrated on the densely packed triangular lattice.

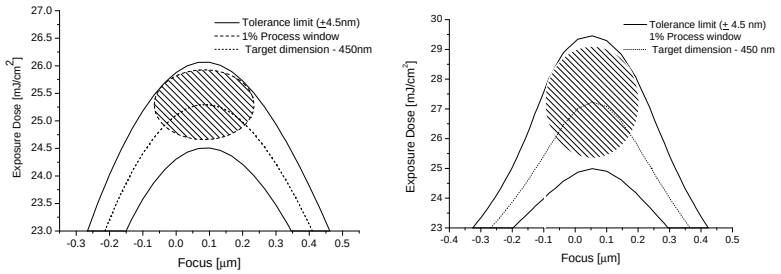


Figure 3.13: Process window of a 450 nm photonic wire using photoresist (Left) AR237J and (Right) AR1682J. Any change in the dose or focus within the ellipse will result in wire width variation within 1% or 4.5 nm.

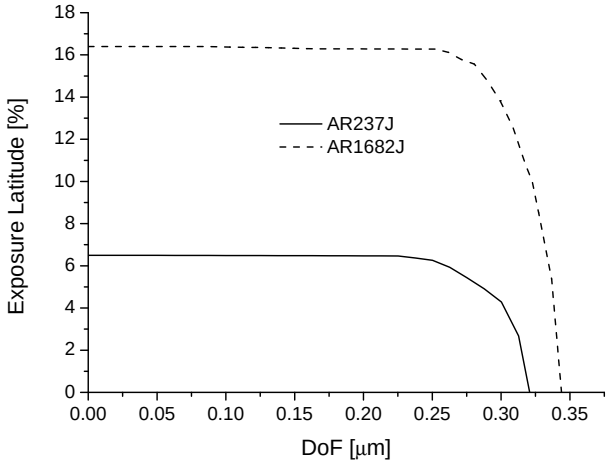


Figure 3.14: Comparison of exposure latitude and depth of focus of AR237J and 1682J at NA=0.63 and σ=0.85.

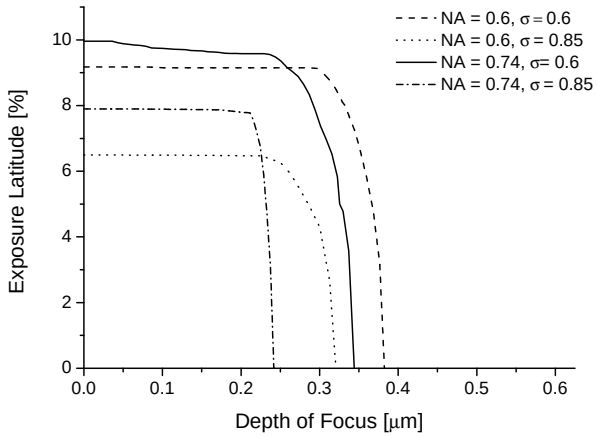


Figure 3.15: Exposure latitude and depth of focus comparison for different illumination settings.

PhCs with different pitch and fill factors were fabricated with the lithography settings optimised for a PhW (NA=0.63 and σ=0.85). Fig. 3.16 shows the fabricated hole diameter for various pitches (400, 460, 500 and 560 nm) as a function of the exposure dose. The two main observations from figure 3.16 are, the hole diameter can be lithographically tuned by varying the exposure dose. Secondly, the exposure dose required for small holes is higher than for the large holes. This is a consequence of energy contributed by the number of diffraction orders for small holes and large holes. Fig. 3.17a shows an overexposed PhC structure with design pitch of 500 nm and 440 nm hole diameter (fill factor = 47 $\%$). The pitch of a PhC is the distance between the two consecutive holes. By over exposure (higher dose), the hole diameter is increased to 490 nm resulting in a mere 50 nm vein of thin resist between the holes. This thin resist is still sufficient to etch a 220 nm hole in the Si layer (Fig.3.17b). With an optimized lithography process, pitches as low as 300 nm can be defined (Fig. 3.17c and d), which was the minimum pitch available in our test mask. Fig. 3.18 shows the process window of a PhC with 400 nm pitch and 240 nm hole diameter. Any variation of exposure dose or focus within the ellipse will change the hole diameter not more than 2%.

Even though various pitches can be printed with the PhW setting, there is a large variation in dose-to-target through pitch (Fig.3.16). Since the exposure dose can be increased linearly(dose sweep), this is not an issue in a research environment. However, in a production environment a uniform exposure dose is preferred. Hence exposure conditions have to be optimised to obtain an overlapping process window or bias has to be applied on the mask design.

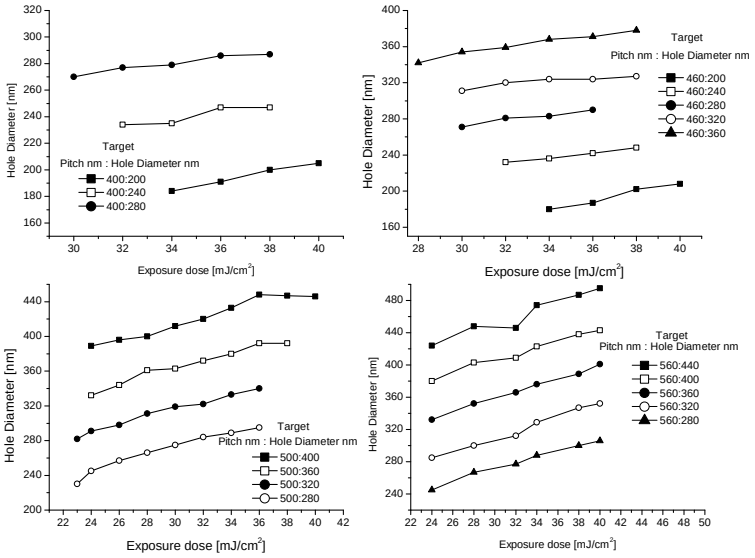


Figure 3.16: Photonic crystal hole diameter as a function of exposure dose.

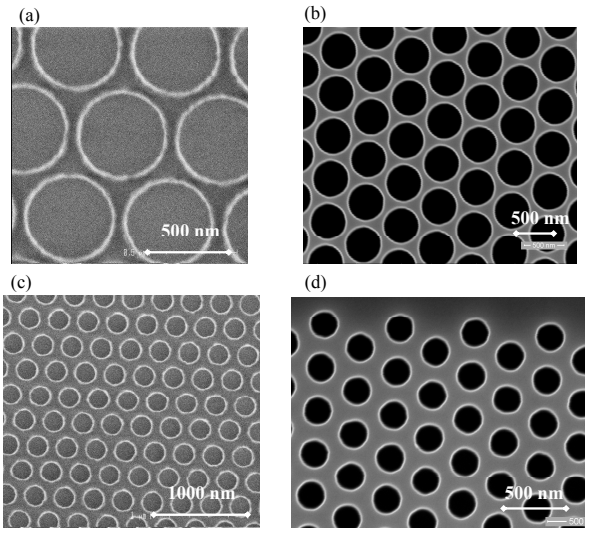


Figure 3.17: Top-down SEM image of photonic crystals a) resist pattern pitch =550 nm, hole diameter = 450 nm , b) same pattern on Si after etching, c) resist pattern pitch =300 nm, hole diameter = 240 nm, d) same pattern on Si after etching

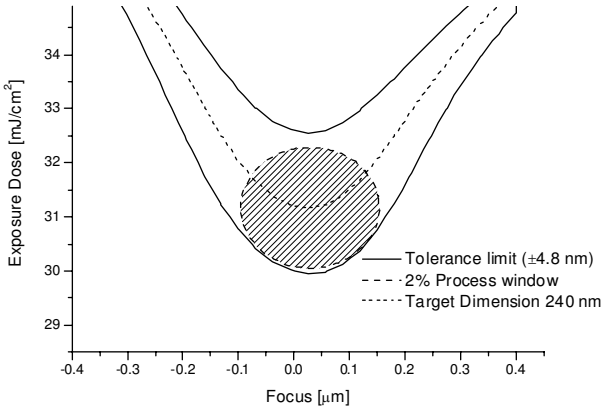


Figure 3.18: Process window of photonic crystal of 400 nm pitch and 240 nm hole diameter. Any change in the dose or focus with-in the ellipse will result in hole diameter variation within 2% or 4.8 nm.

3.2.5 Overlapping process window

A typical photonic integrated circuit would contain a variety of devices with different geometry and density. For example, a distributed Bragg grating in a PhW or a PhC waveguide butt coupled to a PhW. In all these instances, the lithography process should be able to print all the structures within the specifications. In CMOS, this issue is solved by printing them in separate lithography steps, for photonic circuits this will result in unacceptable overlay/alignment errors. For instance, the tool specification for overlay is ≈15 nm, however, in practive this can be ≈50 nm. Hence, being able to print them with a common illumination condition (NA, σ, focus and exposure dose) is essential.

Figure 3.19 shows the overlapping process window of a 450 nm PhW and a grating of 450 nm pitch and 300 nm trench width printed with optimised PhW setting. In this case, there is a good overlap between the two structures. Hence they could be printed with the same illumination and exposure conditions. However, for a PhC of 400 nm pitch and 240 nm hole diameter there is no overlap with the PhW (Fig. 3.20a). In this case, it is impossible to print both the structures with the same exposure condition. This issue can be resolved in two ways. Firstly, the illumination conditions can be tuned to find an overlap between those for PhC and PhW. Figure 3.20b shows such an overlapping window when the NA is increased from 0.63 to 0.74 and σ is decreased from 0.85 to 0.6. Despite the overlap, the DoF($<0.2\mu$m) and EL($<3\%$) are too small for practical use. Secondly, a dimensional correction or bias can be applied to one of the structures without changing the illumination conditions. These corrections should be known in advance to apply them during mask fabrication; hence, an extensive characterization using suitable test structures is a must before designing masks for manufacturing photonic circuits. Bias can be either applied to isolated structures or dense structures. How-

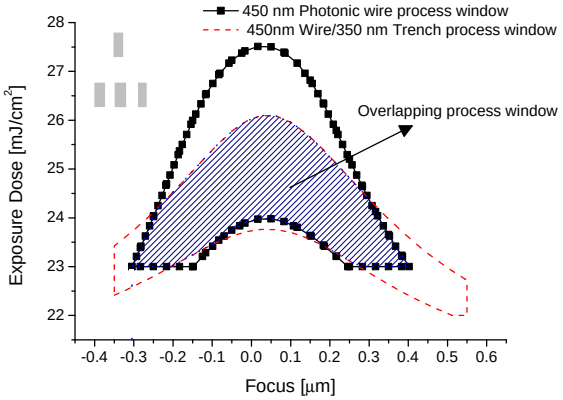


Figure 3.19: Overlapping process window of 450 nm photonic wire and 450/300 nm grating. The inset shows the arrangement of an isolated line and the grating.

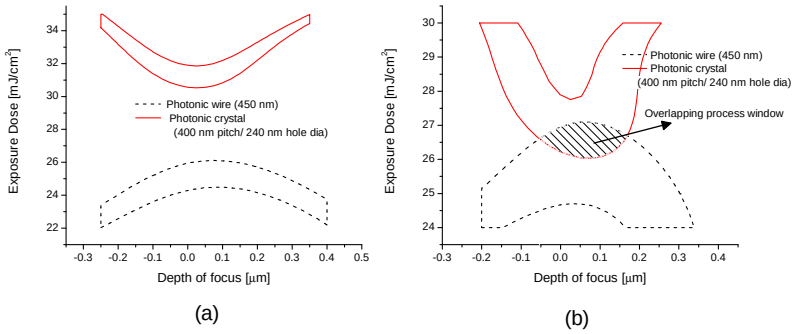


Figure 3.20: Overlapping process window of 450 nm photonic wire and 400/240 nm Photonic crystal (a) NA=0.63, σ=0.85 and (b) NA=0.74, σ=0.6.

ever, it is easier to apply bias to an isolated structure like a PhW than to a dense PhC. The amount of bias required depends on the distance between the process windows.

3.2.6 Optical proximity effect

The optical proximity effect (OPE) refers to a condition where the actual size of the feature depends on the proximity of other features. Eventhough the proxmity effect is primarily caused by diffraction, the magnitude of the efffect also depends on resist processing steps. In photonic circuits, the two primary concerns of proximity effect are in PhC waveguides and PhW directional couplers. In PhC waveguides, due to periodicity breaking, the edge holes in the waveguides are normally printed smaller than the bulk. This deviation of edge holes from the design diameter will

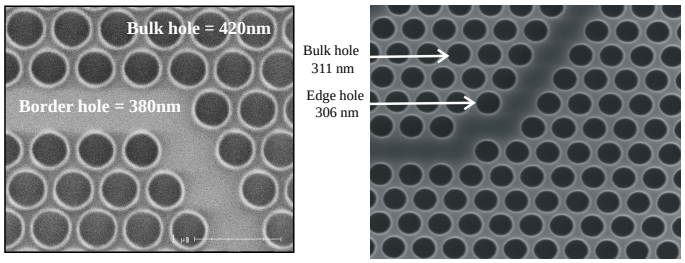


Figure 3.21: Optical proximity effect in photonic crystal waveguide using (a) 248 nm optical lithography and (b) 193 nm optical lithography.

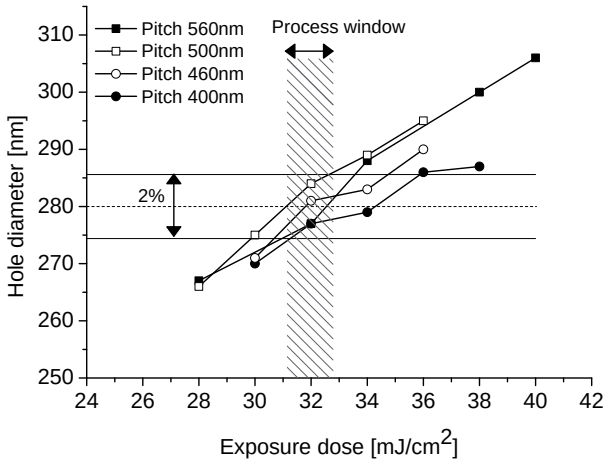


Figure 3.22: Dose-to-target of various photonic crystal pitches (560, 500, 460, and 400 nm) with target hole diameter of 280 nm.

result in a shift and a reduction in width of the transmission bandwidth [3]. For instance, a 10 nm change in the hole diameter would shift the photonic band gap by a significant 20 nm. In PhW directional couplers, OPE results in coupling strength variation, and unwanted reflections and scattering. Hence, OPE has to be taken into account when designing semi-periodic structures. OPE depends strongly on feature proximity, illumination settings (NA, σ, source shape) and wavelength. OPE can be partially corrected (optical proximity correction - OPC) at the mask level by adding sub-resolution assist features (SRAF). This is a standard procedure in mask design for microelectronics circuits [4], which can add significant cost and design effort.

Using 248 nm DUV optical lithography, Bogaerts et al [5] reported an OPE of 40 nm for the holes in a PhC waveguide (Fig. 3.21a). In this work, by us-

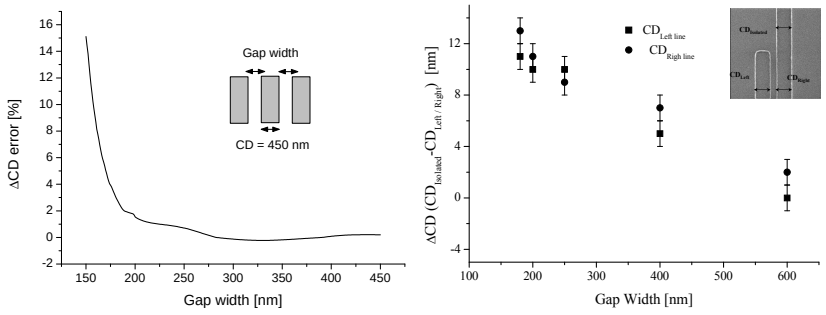
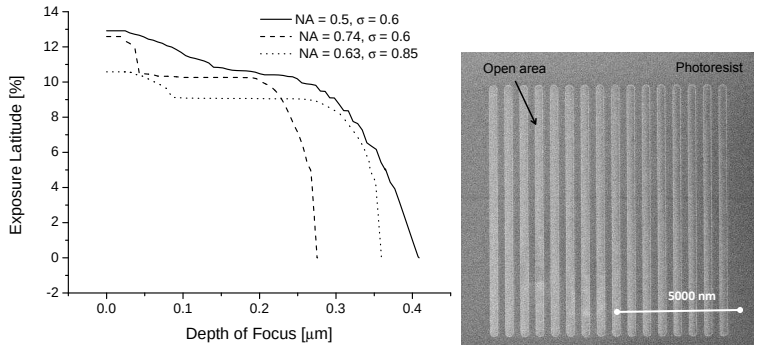


Figure 3.23: (a)Simulated optical proximity effect in a grating and (b) measured optical proximity effect in photonic wires.

ing 193 nm optical lithography, we observe a substantial reduction in OPE (Fig. 3.21b). The difference between edge holes and bulk holes is reduced from 40 nm (248 nm Litho) to 5 nm (193 nm Litho). This reduction in OPE is a consequence of two factors, firstly, shorter illumination wavelength and secondly, illumination settings ($0.63NA/0.85\sigma$) with a larger σ, which is known to reduce OPE. Similar observations were also reported by Settle at al [6].

OPE can become more severe in case of complex heterogeneous cavities formed by varying PhC pitches [7, 8]. In such a case, a thorough characterisation of the PhC process is necessary to compensate the design. Figure 3.22 shows such characterisation, where the dose-to-target of different pitches with the same hole diameter are overlapped to find an overlapping process window for a given tolerance. In this case, a 2% variation of a 280 nm hole gives 6.25% overlapping exposure latitude, which means that each pitch should at least have an overlapping exposure latitude of 3.125 $\%$ at optimum focus. Even though the required exposure latitude is small, achieving this for a wide range of pitches and fill factors makes OPE a challenging task for optimisation.

OPE not only affects superdense PhCs, but also PhW structures. When an isolated line comes in close proximity with another line (e.g. in a directional coupler), the linewidths of both lines reduce as a function of the distance between them. Figure 3.23a shows the change in linewidth of a PhW in the presence of two other wires as a function of the gap between them. It can be clearly seen that the linewidth reduces with decrease in gap width as a consequence of OPE. Figure 3.23b illustrates an experimental observation of OPE in a double line configuration, the inset shows the arrangement of the double lines. Best practice to avoid OPE is to design devices considering OPE data from experiments and adding subresolution assist features to mimic periodicity or by applying bias.



(a) (b)

Figure 3.24: (a)Exposure latitude of fiber coupler (630 nm pitch 50% fillfactor) and (b) SEM image of fiber coupler in photoresist.

3.2.7 Fiber couplers

Unlike PhW and PhC, grating fiber couplers require a shallow etch depth of 70 nm in Si, hence they have to be processed in a separate layer. Grating fiber couplers are implemented as line/space structures with a typical period of 630 nm and a 50 % fill-factor. This design has a peak coupling efficiency at 1550 nm. In addition to grating fiber coupler, other structures such as, low contrast waveguides and deep-shallow transitions are also defined in this lithography layer. However, grating fiber couplers are taken as a target device. The resist stack is kept unchanged from the PhW and PhC process, 330 nm of photoresist on top of 77 nm BARC. Figure 3.24a shows the EL and DoF for various illumination settings. For an EL of 5%, a large NA results in a DoF of 0.27 μm, which is insufficient for a reliable process. At a reduced NA of 0.6 and σ of 0.5, a decent 0.36 μm DoF is achieved for a CD tolerance of 2%. A comparable DoF of 0.34 μm is achieved with the PhW settings of $0.63NA/0.85\sigma$. Based on other structures present along with the fiber couplers, either of these two settings can be used. Figure 3.24b shows one of the grating fiber coupler structures in photoresist, in this case illuminated with $0.63NA/0.85\sigma$.

3.3 Dry etching

After lithography, the structures defined in the photoresist are transferred into Si using Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE). As mentioned earlier in chapter 2, ICP-RIE allows better plasma control for delicate etching. A Highly selective Si etch was developed in the front-end of line etch clusters. The Si etch process was developed considering the following requirements for photonic devices:

1. High selectivity between silicon and silicon dioxide (BOx) to avoid damage

Step No.	Process step	Etch gas	Gas ratio (%)
1	BARC Open	HBr/O_2	75/25
2	Photoresist hardening (PRH)	HBr	100
3	Oxide break through (BT)	CF_4/CH_2F_2	89/11
4	Main etch 1 (ME1)	$Cl_2/HBr/CF_4/O_2$	17/34/48/1
5	Main etch 2 (ME2)	HBr/O_2	100-97.5/0-2.5
6	Over etch (OE)	$HBr/O_2/He$	32/1/67
7	Resist strip	O_2/SF_6	95/5

Table 3.1: Etch process sequence and gases.

to the BOx layer.

2. Smooth sidewalls for low-loss waveguides.
3. Good dimensional uniformity for device uniformity.
4. Stable and reliable process.

Since etch experiments consume a considerable amount of test material, it is not economical to used device grade substrates for process developments, hence dummy SOI wafers were used. These wafers were fabricated by depositing polycrystalline Si on top of surface polished SiO_2. The layer thickness was chosen to match the device wafer stack; 220 nm Si on top of 2000 nm of SiO_2. Two etch depths were targeted; 220 nm for high confinement PhW/PhC devices and 70 nm for low contrast waveguides, transition structures, and grating fiber couplers.

3.3.1 Deep etch process

The wafers with a circuit pattern in the photoresist are transferred into an etch chamber for pattern transfer. A sequence of steps was executed, resulting in the desired pattern in Si. Table 3.1 shows the sequence of steps performed inside the chamber. Before etching the wafer, the chamber is cleaned with a F based plasma to create a stable chamber condition for the subsequent etch process. After chamber cleaning, the wafer is loaded into the chamber for etching followed by the BARC open etch using HBr/O_2 gases. The selectivity between BARC and photoresist is poor: both are etched at comparable rates (1:1.1); 82 nm of photoresist is consumed to open a 77 nm of BARC layer. After the BARC open etch, the photoresist is hardened using HBr to improve etch selectivity between the photoresist and Si [9]. Ellipsometry measurements showed that the hardning process increased the refractive index or the density by 9.4 %. In addition to hardening, this step also smoothens high frequency sidewall roughness in the photoresist by consuming ≈62.5 nm of the thickness of the photoresist. These photoresist losses result in an effective photoresist thickness of 263 nm.

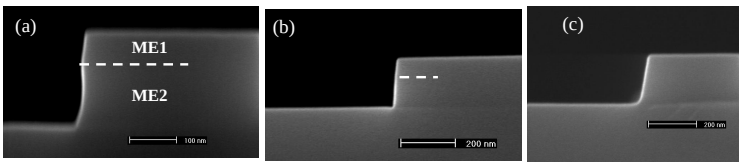


Figure 3.25: Silicon etch profile as a function of O2 concentration a) 0 % ,b)0.8 % and, c) 2.3 %. The dotted lines shows the pattern defined by ME1 and ME2

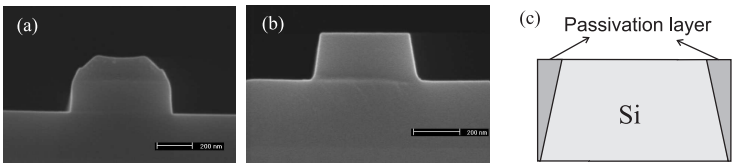


Figure 3.26: Silicon etch profile a) before, b) after resist strip and clean and c) schematic of passivation layer thickness on the sidewalls

After resist hardening, the Si etch is done in 4 steps: the break-through etch (BT), the main etch 1 (ME1), the main etch 2 (ME2) and the over-etch (OE) (Table 3.1). Firstly, the native oxide on the surface of Si is removed by the F rich BT plasma followed by the main etch sequence. One of the main requirements for a good etch process for a photonic device is good control over the dimensions of the devices (i.e linewidth, hole diameter, trench width, etc.). Therefore, ME1 is tailored to decrease the bias between isolated structures (wires) and dense structures (photonics crystals) [10]. After ME1, we switch to ME2, which uses HBr/O_2 chemistry to etch the major part of Si. The HBr/O_2 chemistry used in ME2 is very selective towards $SiO2$ and hence the etch process will terminate when all the Si is removed. An overetch is applied with a more isotropic etch process condition to remove any remaining footing at the bottom of the etched feature. Since ME2 etches most of the Si, the etch profile strongly depends on the ME2 etch conditions, in particular its chemistry. The etch chemistry in ME2 is tailored to achieve vertical sidewalls because the sidewall angle plays an important role in device performance, for example, polarization crosstalk [11].

When exposed to a pure HBr plasma, we observe isotropic Si etching (Fig.3.25a) due to the absence of a passivation layer on the sidewalls, which exposes Si to aggressive Br radicals. Anisotropy can be achieved by protecting the sidewalls with a passivation layer containing $Si/O/Br/C$, which is chemically resistant to Br radicals. In particular, SiO_xBr_y like compounds are good sidewall inhibitors to achieve anisotropic Si etching [10]. The thickness of the passivation layer depends on the amount of Si, O, Br and C in it. By increasing the concentration of any of the constituents, the thickness can be increased. In our case, when a small amount

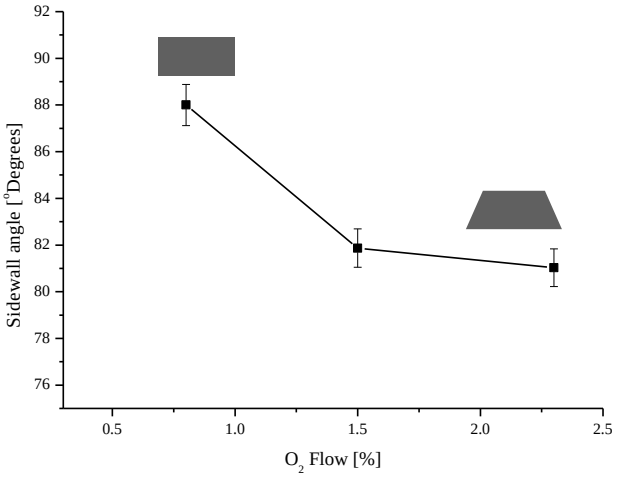


Figure 3.27: Sidewall angle as a function of O_2 concentration in HBr/O_2.

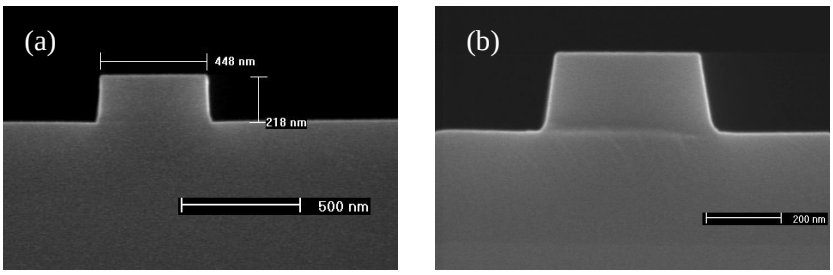


Figure 3.28: Silicon photonic wire with (a) sloped and (b) vertical profile sidewall profile.

of O_2 is added in the feed gas, the etch process is made anisotropic (Fig. 3.25b & c) as a result of sufficient passivation layer deposition on the sidewalls.

We observe a slight increase in the Si etch rate with an increase in O_2 concentration. An etch rate of ≈60 nm/min and ≈72 nm/min was observed for 0.8 and 2.3 % of O_2 in the ME2 feed gas. The increase in the etch rate can be attributed to unsaturation of polymeric volatile etch byproducts by O atoms. This unsaturation releases reactive Br atoms from etch byproducts and allows them to react with Si again. However, at a higher concentration, O atoms chemisorb on to the Si surface and reduces the etch rate. Thus by using an optimum amount of O_2 the Si etch rate can be kept high enough for fast wafer throughput.

In addition to facilitating anisotropic etching, the passivation layer modifies the etch profile. During the etch process the top of the PhW is exposed longer than the bottom. This result in a thicker passivation layer at the top than at the bottom (Fig.

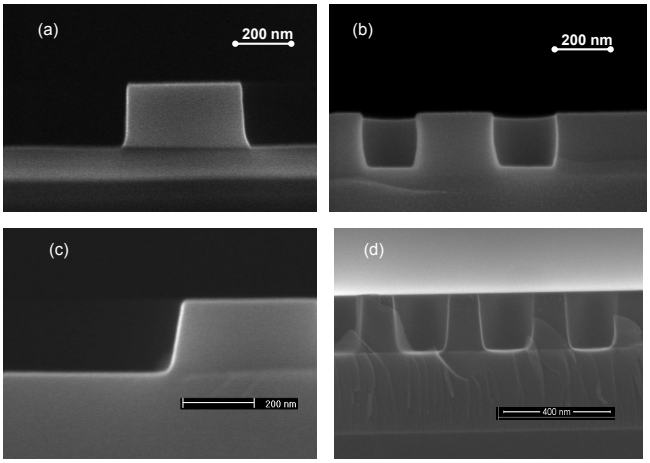


Figure 3.29: Aspect ration dependent etch profile variation of vertical (a&b) and sloped (c&d) PhW etch process.

3.26c). Fig. 3.26a shows a PhW before photoresist removal and cleaning, where a vertical sidewall can be clearly observed. However, after cleaning the photoresist and passivation layer, the actual etch profile is revealed (Fig.3.26b). This clearly shows the gradient in the passivation layer thickness along the height of a PhW sidewall. By controlling the thickness the sidewall angle can be tuned (Fig. 3.27). Fig. 3.28a shows a PhW fabricated with the optimum concentration of O_2 (0.75%) in ME2 and a modified ME1 etch duration.

Even though a vertical sidewall PhW is desired for devices, this process cannot be used for dense and high aspect ratio devices such as slots and PhCs. The main reason for this is the aspect ratio dependent etch effects. Aspect ratio dependent etch (ARDE), as the name indicates is related to the aspect ratio (depth : width) of the structures. The aspect ratio of the structure affects the etch process in different ways than the absolute feature size itself. The two main consequences of ARDE are micro and macro-loading. Micro-loading is caused by a localized depletion of the reactive species or accumulation of reaction by-products as a result of the local pattern density on the wafer. For example, identical structures can etch at a different rate due to difference in local density. On the other hand, macro-loading is caused by the consumption of reactive species during the etch process. For instance, a trench of 100 and 1000 nm would etch slower compared to a trench of 500 nm. In case of 100 nm trench, the etch radials cannot get into the trench due to smaller size resulting in slow etch rate, while in 1000 nm trench the etch rate will be slower due to an insufficient number of etch radicals. This is also referred to as etch lag.

In case of a dense and high aspect ratio structure like PhC and trenches, lack of sufficient etch by-products results in poor passivation layer thickness on the sidewalls. Figure 3.29 shows the effect of ARDE on etch profile of an isolated PhW

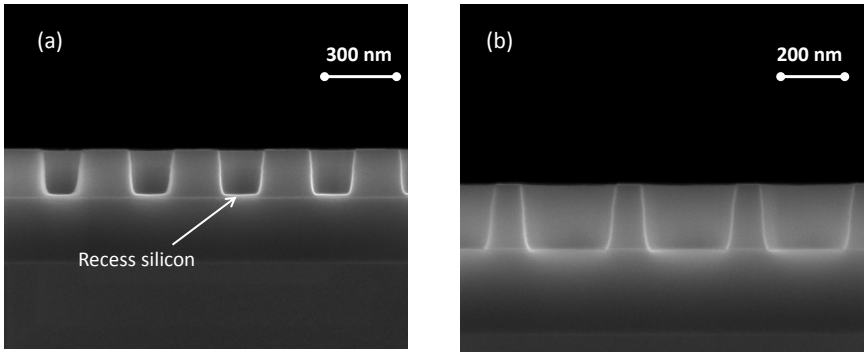


Figure 3.30: Aspect ratio dependent etch resulting in recess Si due to etch lag between a) small holes and b) large holes.

and dense PhC of a vertical and sloped etch process. When using a vertical etch process with 0.75$\%$ of O_2, the PhW shows a vertical sidewall, while the sidewalls are bowed in case of a PhC (Fig. 3.29 a and b). The bowing in PhCs is a result of lateral etch due to insufficient thickness of passivation layer on the sidewalls, while sufficient passivation layer is available on PhW sidewalls. This etch process is simply not acceptable for a wide variety of photonic devices. Hence to compensate for passivation layer thickness in the high aspect ratio features, the O_2 concentration in the feed gas is increased from 0.75 $\%$ to 2.3 $\%$ to decrease the profile difference between PhW and PhCs (Fig. 3.29 c and d). We have to note that addition of O_2 facilitates passivation layer thickness compensation and does not affect the etch lag between PhW and cPhC and among PhCs of different aspect ratio. Figure 3.30 shows the effect of etch lag on PhCs of two different aspect ratios. The issue of etch lag is overcome by increasing the etch duration. This can be easily implemented since the etch chemistries of ME2 and OE are very selective to SiO_2.

3.3.2 Litho-etch bias

Post-etch lateral dimension of the features depends on their etch profile. The change in the dimension between lithography and dry etch is referred to as litho-etch bias. It is essential to know this bias value for compensation. During the etch process, as mentioned earlier the steps before the actual Si etch already modify the feature's dimensions and resist profile. Since BARC etch and resist hardening attacks the sidewalls of the photoresist, the linewidth decreases after these two processes (Fig. 3.31a). However, after Si etch an increase of $\approx$15 nm in Si linewidth is observed. This increase is due to the sloped etch profile ($\approx 8^o$), as the linewidth is measured at the bottom (70 $\%$ from top) of the PhW. The evolution of hole diameter of a PhC follows a similar but opposite evolution: the hole diameter decreases due to sloped sidewalls.

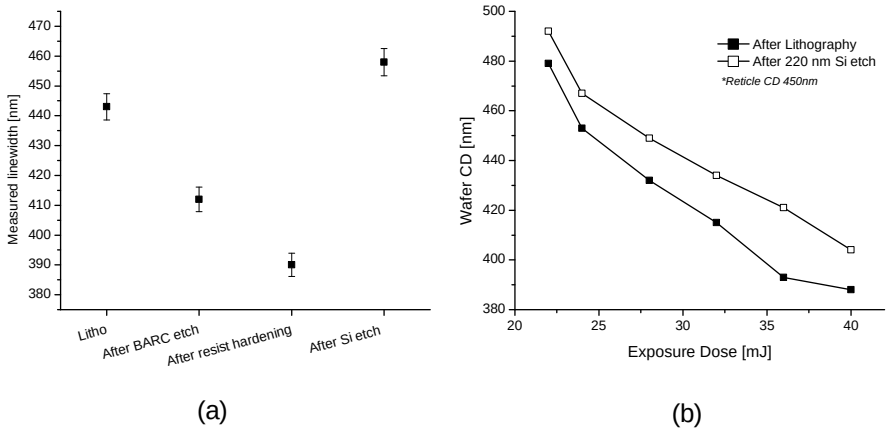


Figure 3.31: Litho-etch bias. a) linewidth evoluation of a photonic wire and b) litho-etch bias through dose of a 450 nm photonic wire.

Step No.	Process step	Etch gas	Gas ratio (%)
1	BARC Open	HBr/O_2	75/25
2	Oxide break through (BT)	CF_4/CH_2F_2	89/11
3	Main etch 1 (ME1)	$Cl_2/HBr/CF_4/O_2$	17/34/48/1
4	Resist strip	O_2/SF_6	95/5

Table 3.2: Etch process sequence and gases of a shallow etch process.

3.3.3 Shallow etch process

As explained before, a grating fiber coupler is an elegant solution for coupling light in and out of a silicon photonic circuit. Unlike PhW and crystals, the optimal etch depth for grating fiber couplers (FC) is 70 nm. Hence FC have to be processed in a separate layer. This shallow etch layer also accommodates shallow waveguides and deep-shallow transitions. Since the etch is only 70 nm in a 220 nm thick Si, there is no etch stop layer like in the 220 nm deep etch. Therefore, the etch process sequence is adapted (Table 3.2 for a non-selective Si etch, which was timed to achieve an etch depth of 70 nm. In comparison to the waveguide etch sequence (Table 3.1), the photoresist hardening step is not used since the unhardened selectivity is sufficient for 70 nm etch depth. Figure 3.32 shows the cross-section of a grating fiber coupler with a targeted 70 nm etch depth in Si. Since the etch process is timed, the etch depth can be simply tuned by changing the duration of the etch process. Using this process, a variety of components has been fabricated and demonstrated good performance, including low-loss waveguide crossings [12].

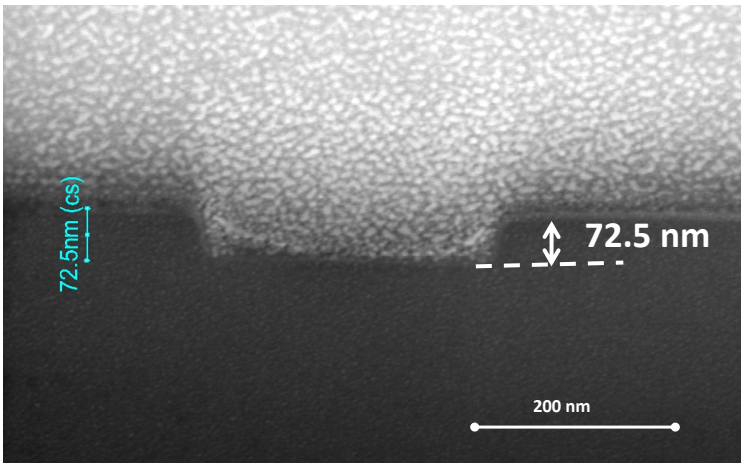
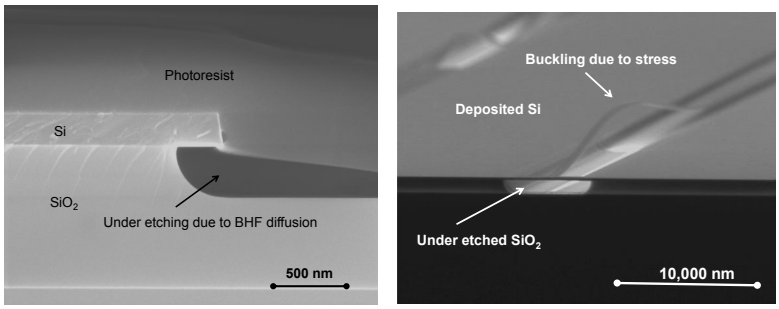


Figure 3.32: Cross-section micrograph of a shallow etched grating fiber coupler with 70 nm etch into Si.

3.4 Photonic crystal membrane

2D photonic crystals need symmetric refractive index in the vertical direction for low-loss operation. Hence either an oxide cladding or free standing membrane is required. Membrane PhCs are preferred over oxide cladding since the area under the light cone can be made large and furthermore it can provide maximum index contrast for confinement. PhC membrane can be formed by removing the BOx layer underneath the PhCs. The process of forming PhC membrane is presented in this section.

After PhC definition, a window is defined in photoresist on top of the PhCs, while protecting all the other devices. A thicker photoresist (800 nm) was used for maximum protection. Since the windows were wide $\approx$10 μm 248 nm optical lithography was used. The wafer is then placed in buffered hydrofluoric acid (BHF) to under etch the BOx layer. Figure 3.33 shows the two primary results. Firstly, in spite of a thick photoresist layer the BHF diffuses through the photoresist resulting in damaging the protected area. Secondly, since we were using deposited Si on insulator wafers the stress in the film results in buckling of PhW as a consequence of under etching. A simple solution to the later issue is to use crystalline SOI wafers for process development instead of dummy wafers. However, the issue of BHF diffusion is related to BHF-resistance of the photoresist material. Since the conventional photoresists used in the CMOS processes are not designed for such a purpose, inorganic materials with high etch selectivity to BHF, such as silicon nitride or silicon carbide can be used. However, incorporating inorganic layers required additional process steps; deposition, lithography and dry etch for window definition. Hence a simple and economical solution is contact lithography



(a) first (b) second

Figure 3.33: (a) Diffusion of BHF resulting in under etched Photonic wire and (b) Buckling of Photonic wire as aresult of stress in deposited Si on insulator wafer.

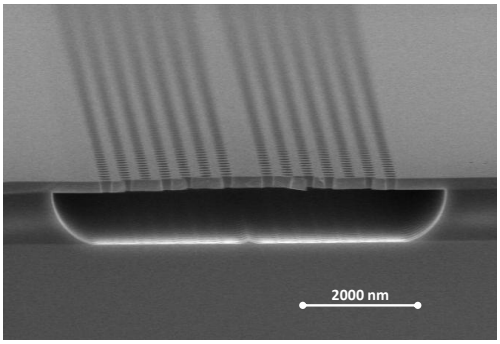
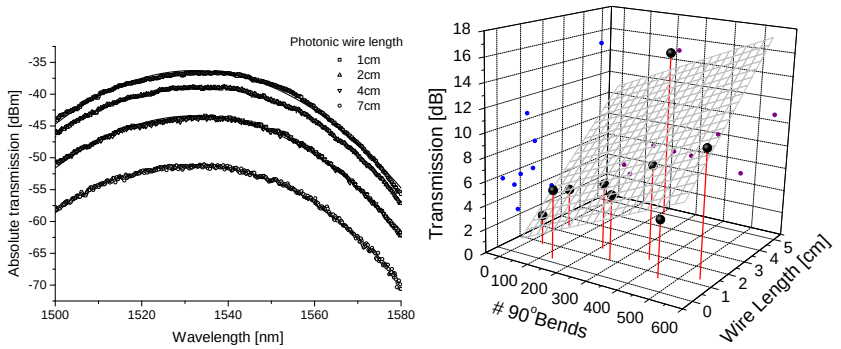


Figure 3.34: Photonic crystal membrane formed by under etching BOx layer using contact lithography and BHF.

with thick photoresist (≈1500 nm). For this work we processed individual dies, however the processing is also possible on wafer scale. Figure 3.34 shows one of the PhC membranes fabricated using such a process. Since the BHF solution has to go through the PhC holes to reach the BOx layer, the under-etch rate cannot be estimated from the bulk etch rate. Hence it has to be determined empirically.

3.5 Optical characterization

The 193 nm optical lithography and dry etching process are evaluated through optical transmission characterization. PhWs, micro-bends, PhCs and wavelength-selective PhW devices were fabricated and characterized for their performance. The devices were fabricated in a 200 mm crystalline SOI wafer with 220 nm of Si on top of 2000 nm SiO_2 buried oxide. All the devices were fabricated with shallow etched TE grating coupler at the input and output of the circuit for efficient light



(a) (b)

Figure 3.35: (a) Transmission spectrum of photonic wires of different length, the parabolic spectrum is due to the fibre coupler and (b) projection of transmitted power at 1550 nm for various photonic wire lengths and bend radius.

coupling at 1550 nm.

3.5.1 Measurement setup

In order to couple light into the fiber couplers, vertically mounted fiber stages were used. This setup is used throughout this thesis for device characterization, unless mentioned otherwise. To characterize the devices a broad band light source or a tunable laser is used as the light source and the transmitted power is measured using a spectrum analyser or a photodetector with required spectral resolution. The input polarization (TE:(E_x) - parallel to the wafer plane) of the light is controlled using polarization controlling wheels. The output light from the chip is directly connected to either a spectrum analyser or a photodetector. The details on the setup can be found in the doctoral dissertation of Dr. Wim Bogaerts [3].

3.5.2 Photonic wires and bend loss

The PhW waveguide was designed to be 500 nm wide and by using a dose sweep from left to right of the wafer the width was varied between 550 and 450 nm. Spiral PhW with different wire length and bending radius were used to measure the propagation and the bend loss. The PhW length was varied from 0.5 cm to 5 cm, while the number of 90° bends were varied from 50 to 550 with a bending radius of 1, 2, 3 and 5 μm. After measuring the transmitted power, the spectrum is fitted with a parabolic function to remove noise from the spectrum (Fig. 3.35a). From the fit transmitted power at 1550 nm is projected against the length and number of bends (Fig. 3.35b). Finally, propagation loss and bend loss is extracted by fitting an intersection plane.

We characterized PhWs with two cross-section profile; a vertical and a sloped sidewall. From the propagation loss characterization, we did not observe a significant difference between sloped ($\approx 81^o$) and vertical($\approx 90^o$) PhW (Fig.3.36a). We observed a propagation loss of $3 \pm 0.1 dB/cm$ and $2.7 \pm 0.09 dB/cm$ for vertical and sloped sidewall wires, respectively. A difference of $0.3 dB/cm$ in propagation loss can be attributed to slight increase in the sidewall roughness due to thinner passivation layer thickness on the PhW with vertical sidewalls.

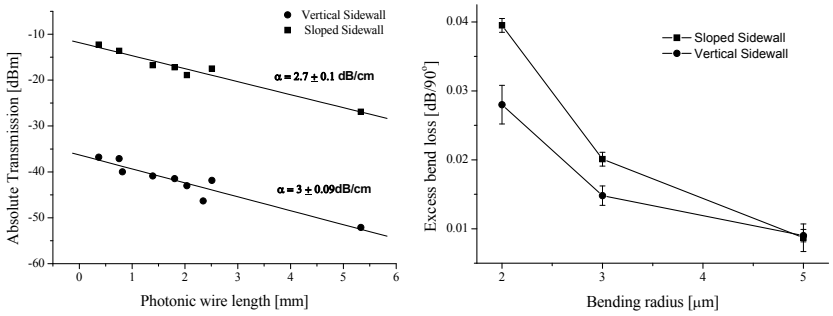
However, we observed a decrease in bend loss of PhWs with vertical sidewalls. Fig. 3.36b shows the bend loss of micro-bends with different bend radius and sidewall angle. There is a clear indication that the bend loss of a vertical sidewall PhW decreases by $\approx 25\%$ from a sloped sidewall PhW. We observe bend loss as low as 0.015 and 0.028 dB/90^{o}bend for bend radius of 3 and 2 μm respectively for vertical PhW bends, while for sloped wires the bend loss stood at 0.029 and 0.039 dB/90^{o}bend for 3 and 2 μm bend radius respectively. The improvement in the bend loss of narrow bends can be attributed mainly to a reduction in the polarization conversion loss in the bends due to a more symmetric waveguide profile. However, no significant change was observed for large bends (5 μm), where the perturbation is less significant. The results obtained from our experiments agrees well with the trend obtained from 3D FDTD simulations by Sakai et al [11].

PhW loss is considered as a bench mark metric for qualifying a fabrication technology for device and circuit fabrication. Since the beginning of Si photonic integrated circuits efforts have been spent to reduce the propagation loss in PhW. Table 3.3 shows some of the PhW propagation loss from the literature. As it can be seen in table 3.3, the loss varies irrespective of the fabrication technology. Even though different waveguide geometries were used in the literature the main idea is to use a single mode high confinement waveguide, which allows compact circuits. In this scenario, it is valid to compare the PhW loss among different cross-section dimension given that the PhW is single mode with high modal confinement.

The propagation loss achieved in this work with CMOS fabrication technology is very close to the literature values reported for e-beam technology. Compared with similar technology, the achieved results are at least 50 $\%$ better, which demonstrates the quality of the fabrication process. One of the important results that we observed is the effect of the mask on the propagation loss. Despite using same fabrication process, optical lithography and dry etching, the propagation loss varied slightly $\approx$ 0.2-0.3 dBcm between different masks. In addition to the fabrication process, the mask fabrication technology and layout(density) also affect the propagation loss.

3.5.3 Photonic crystals waveguide loss

The PhC waveguide loss was measured using the cut-back method. The PhC waveguides were designed by removing a row along the Γ-M direction creating a W1 waveguide. The W1 waveguide is then butt coupled to a PhW for coupling light in and out of a W1 waveguide. The PhCs were designed with the following design parameters: 400 nm pitch and 220 nm hole diameter. The length of the



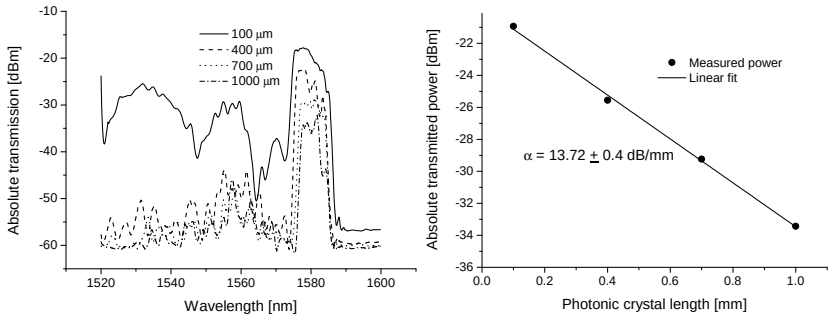
(a) (b)

Figure 3.36: Propagation (a) and micro-bend (b) loss of sloped and vertical sidewall photonic wire.

Reference	Cross-section (nm)	TE loss (dB/cm)	measurement method	Cladding	Fabrication Technology
IBM [13]	510×226	1.7±0.1	Cutback	Air	e-beam
Glasgow Univ. [14]	500×260	0.92±0.14	Fabry-Perot	Air	e-beam
NTT [15]	400×200	2.8	Cutback	SiO_2	e-beam
	300×300	7.8			
CEA-LETI [16]	512×220	4.18±0.21	Cutback	Air	193 nm optical
MIT-BAE systems [17]	370×200	11.6±0.5	Cutback	SiO_2	248 nm optical
	420×200	8.2±0.5			
	470×200	5.7±0.5			
	520×200	4.6±0.5			
	570×200	4.3±0.5			
Ghent Univ.-imec [18]	400×220	33.8±1.7	Fabry-Perot	Air	248 nm optical
	440×220	9.5±1.8			
	450×220	7.4±0.9			
	500×220	2.4±1.6			
Ghent Univ.-imec	515×220	2.74±0.06	Cutback	Air	193 nm optical
this work -mask1	500×220	2.73±0.1			
	485×220	2.85±0.07			
Ghent Univ.-imec	515×220	2.43±0.04	Cutback	Air	193 nm optical
this work -mask2	500×220	2.42±0.06			
	485×220	2.64±0.05			

Table 3.3: Propagation loss of Photonic wire waveguides comparison from the literature.

W1 waveguides varied from 100 - 1000 μm. The PhWs that are butt coupled to W1 waveguides were adiabatically tapered from a 10 μm broad (from fiber cou-



(a) (b)

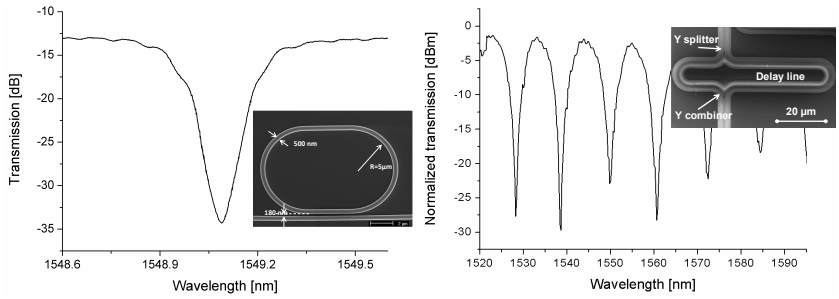
Figure 3.37: (a) Transmission spectrum of a photonic crystal membrane of 400 nm pitch and 220 nm hole diameter and (b) propagation loss of the same.

Reference	Waveguide loss	Cladding	Fabrication Technology
IBM [20]	3 dB/cm	Air	e-beam
Univ. St. Andrews [19]	14.2 dB/cm	Air	193 nm lithography
Univ. St. Andrews	4.1 dB/cm	Air	e-beam
NTT [21]	10 dB/cm	Air	e-beam
NTT [21]	15 dB/cm	SiO_2	e-beam
COM, Tech. Univ. Denmark [22]	40		e-beam
Ghent Univ.-imec [23]	7.5 dB/mm	Air	248 nm lithography
This work	13.72 dB/mm	Air	193 nm lithography

Table 3.4: Propagation loss of Photonic crystal waveguides from the literature.

plers) to avoid loss in the wire section. It is necessary to form a membrance to avoid TE/TM mode coupling in the W1 waveguides, which eventually results in propagation loss. Hence PhC membrane was fabricated as shown in section 3.4.

Figure 3.37 depicts the loss characterization results of a W1 waveguide. Figure 3.37a shows the transmission spectrum for different lengths of the W1 waveguide. The spectrum clearly shows the transmission band of the PhC waveguide. The propagation loss is measured in the transmission band (at 1581 nm) by linear regression of transmitted power for different W1 waveguide lengths, which measured a loss of 13.72$\pm$0.4 dB/mm. The measured propagation loss is an order of magnitude higher than the demonstrated loss with same fabrication technology [19]. We suspect that such a large loss is a consequence of two factors, firstly, the sidewalls of the holes are not perfectly vertical and secondly, recess Si at the bottom of the holes. These two imperfections in fabrication can seriously affect the propagation loss of a PhC waveguides.



(a) (b)

Figure 3.38: Transmission spectrum of (b) a ring resonator and (b) a mach-zhender interferometer. Inset shows the SEM image of the devices.

3.5.4 Wavelength selective devices

Various wavelength selective devices have been fabricated with good wavelength response and performance [24]. Here, as a technology demonstrator, we present two basic wavelength filters; racetrack ring notch filter and Mach-Zehnder interferometer. A racetrack-ring notch filter was implemented by coupling a racetrack ring with a bus waveguide. The design width of the ring and bus waveguide was 500 nm and the gap was 180 nm. Since the bend loss is low, a bend radius of 5 μm is chosen as the bend radius of the rings. Figure 3.38a shows one of the fabricated filters and its transmission response. In this case, a quality factor of 15,000 was achieved with an average free spectral range of 15 nm.

In addition to ring filters, Mach-Zehnder interferometers (MZI) were implemented in the same layer. The MZI was implemented by two Y-splitters and introducing a delay length of 50μm in one of the two arms. Figure 3.38b shows one of the fabricated MZI's and its transmission response. We obtain an average free spectral range ($\Delta\lambda$)of 10nm. From the spectral response of the MZI we extract a group index of 4.8 ($n_g = \lambda_{min}\lambda_{max}/\Delta L\Delta\lambda$). A balanced power splitting by the Y-splitter yields an average extinction ratio of 27dB and an on-chip insertion loss of 3dB.

These characterizations demonstrate that the high resolution patterning using 193 nm optical lithography and dry etching process in a 200 mm CMOS pilot line can deliver devices with good performance figures, such as the propagation loss, insertion loss and quality factor.

3.6 Propagation loss reduction

Propagation loss of a photonic wire is considered as one of the key figures of merit in silicon photonic integrated circuits. In general, loss of optical power in the waveguides is caused by one or more of the following; absorption, scattering and

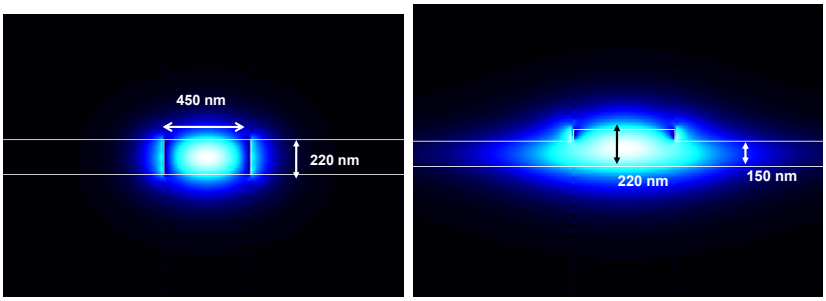
coupling to radiation/lossy modes. Absorption loss is mainly related to bulk and surface absorption of light due to defects, such as unbound Si atoms. The bulk defect appears as a result of poor material quality while the surface defects arise due to pattern definition and fabrication processes such as CMP. SOI wafers are manufactured in a variety of ways [25–29]. During the fabrication process, the Si is subjected to different chemical and high energy physical processes, which could create material defects. A low defect fabrication process is always preferred for photonic applications. Among these techniques smartcut SOI wafers are widely used for Si photonics, which has been widely accepted as highly transparent in infrared wavelengths with very low absorption loss. On the other hand, surface defects, both on the top surface and on the sidewalls can lead to absorption loss [30]. It has been shown that by surface treatment and encapsulating the defects low loss can be achieved [31].

The other loss mechanism is scattering from roughness on the sidewalls of the waveguides, which is mainly caused by the pattern definition process. The roughness in the photoresist is transferred into Si through dry etching with additional roughness from the etch process itself. Even though the roughness can be reduced by process optimizations, there are limitations on the achievable smoothness. In addition to the sidewall roughness, the scattering from the roughness on the top surface of the device also contributes to the propagation loss. However, the degree of its influence depends on the operating polarization, for instance, TE is less influenced by surface roughness while TM is most affected by it. Finally, coupling loss arises from the circuit and waveguide design. Any perturbation in the waveguides, such as a mismatch in waveguide dimensions and bend waveguides can lead to mode coupling to higher order lossy modes. The effect of waveguide crosssection on the bend loss presented in section 3.5.2 is an example of a coupling loss mechanism.

Since the SOI wafers are purchased from a commercial vendor the material absorption depends on the wafer manufacturing and quality control process of the vendor. The scattering and coupling loss, however, can be reduced by the device and fabrication process designer. Efforts have been made to reduce the propagation loss in two ways. Firstly, by changing the waveguide geometry to avoid scattering loss from the waveguide crossection [32–34] and secondly, by using post-fabrication treatments [35–37] and circuit design [38].

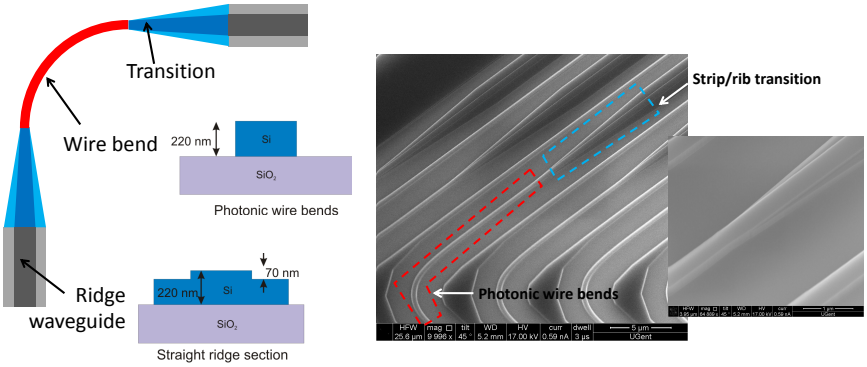
3.6.1 Low-loss waveguide geometry

Reducing the overlap between the mode and the rough sidewalls of the waveguide will reduce the propagation loss. In a photonic wire waveguide (450×220 nm^2), a large amount of field is concentrated on the edges of the waveguide sidewalls (Fig. 3.39a), while the overlap is small for a shallow etch waveguide (Fig. 3.39b). Using shallow etched rib waveguide the scattering loss can be reduced to a greater extent allowing low-loss waveguides [33]. However, due to low optical confinement circuits with sharp micro-bends cannot be designed. An ideal option is to use low-loss rib waveguides for straight section and high-confinement wires as bent waveguide



(a) (b)

Figure 3.39: Modal overlap of TE_{00} with (a) Photonic wire and (b) shallow etch waveguide.



(a) (b)

Figure 3.40: (a) Schematic and (b) scanning electron microscope image of a hybrid rib/wire waveguide.

resulting in a hybrid waveguide. The transition of rib to strip consists of a linear tapering of the deep-etched waveguide, with a slower tapering of the shallow-etch waveguide core. Figure 3.40 depicts a section of the hybrid waveguide fabrication using a 220 nm etch photonic wire and a 70 nm etch rib waveguide. The hybrid waveguide was designed with a rib width of 700 nm and wire width of 450 nm connected by a 15 μm long linear taper. The photonic wire waveguide was bent with a bending radius of 5 μm, which makes a compact waveguide circuit. During fabrication, the exposure dose for photonic wire waveguides was varied over the wafer resulting in waveguides of different widths.

We characterized the propagation and bend loss of the hybrid waveguide by measuring the transmitted power through 4-16 cm long spiral waveguides with 34-456 number of wire bends. Figure 3.41a shows the transmission plotted against the

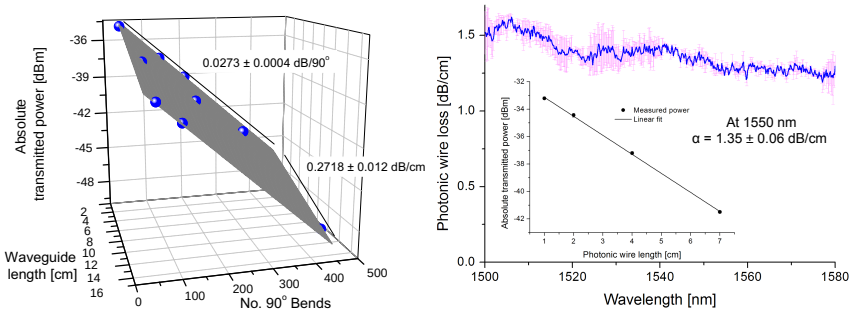


Figure 3.41: (a) Propagation and bend loss of hybrid waveguide circuit and (b) Propagation loss of photonic wire (450×220 nm^2).

Wire width[nm]	Ridge waveguide loss [dB/cm]	Total bend loss [dB/90^o]
470	0.2718±0.012	0.027±0.0004
460	0.286±0.019	0.032±0.001
420	0.33±0.05	0.068±0.002

Table 3.5: Propagation loss and bend loss of 700 nm wide Rib waveguide with wire bends.

shallow-rib waveguide length and number of bends. The waveguide and bend loss is extracted by fitting a 2D-plane to the 9 measured data points. From the fitting, we extracted a propagation loss of 0.2718±0.012 dB/cm propagation loss for the straight shallow rib waveguide and a bend loss 0.0273±0.0004 dB per 90^{o}bend. This bend loss includes all contributions from the bent waveguide itself as well as the transition sections. To our knowledge, this is the lowest loss reported for an etched single-mode waveguide in a thin SOI substrate. In the same layer, we also implemented high-confinement photonic wire waveguide, which measured a propagation loss of 1.36±0.06 dB/cm.

As mentioned earlier, we varied the exposure dose over the wafer for the patterning of the strip waveguides, so we end up with a variation in wire widths. Table 3.5 summarizes the propagation and bend loss for different wire waveguide widths. It can be clearly seen that the bend loss increases with a decrease in photonic wire width, which can be attributed to a decrease in modal confinement with the wire. This in turn increases the radiation loss in the bends, but most likely also the transition loss in the taper. As the shallow-ridge waveguide width was kept constant, the propagation loss did not change significantly.

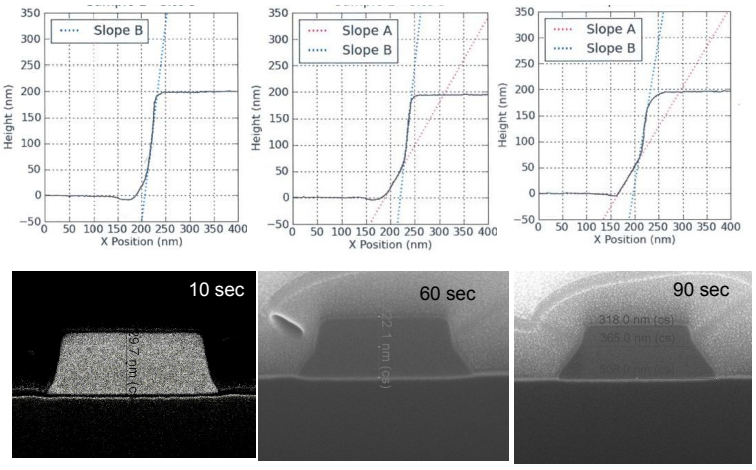
3.6.2 Directional etch and smoothing

In principle, patterns in Si can be defined by using anisotropic wet etching. By taking advantage of the crystal planes, patterns with atomic level smoothness can be defined. In crystalline Si the density of arrangement of atoms results in varying etch rates. Wet chemicals, such as potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH) and ethylenediamine-pyrocatechol(EDP) etch crystalline Si preferentially along a crystal plane. Since the etch process removes atoms from a particular crystal plane atomic layer smoothness can be achieved.

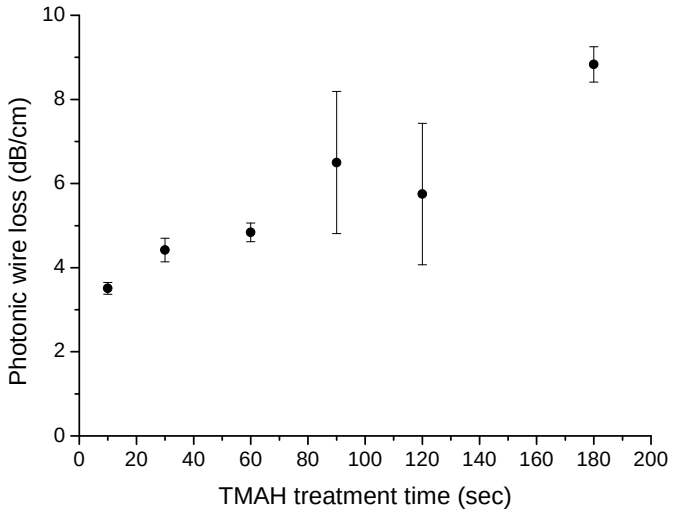
In our study, we used TMAH at room temperature to smoothen photonic wires defined in $<100>$ plane with $<110>$ plane as its sidewalls. Since $<110>$ has high etch rate in comparison to $<100>$ plane, lateral etching reveals the dense $<111>$ plane with a sidewall angle of $\approx 55^o$ (Fig. 3.42a). We observed an etch rate of $\approx$ 50 nm/min for $<110>$ plane and $<$10 nm/min for $<100>$ plane. After treatment, the sidewall roughness was measured using a special sidewall atomic force microscope, which measured a roughness of 2-2.5 nm for all the treated wires. However, the profile of the photonic wire is deformed to a large-angle trapezoid. As already discussed in section 3.5.2, photonic wires with large sidewall angles are susceptible to mode conversion loss. Figure 3.42b shows the photonic wire loss as a function of treatment time. Despite roughness reduction a clear increase in the propagation loss with treatment was observed. This can be due to two reasons, decrease in photonic wire width in combination with waveguide profile change. Decrease in the waveguide width decreases the intensity of optical power in the sidewalls (weakly guiding), which should reduce scattering loss. However, we observe an increase in propagation loss. This can be attributed to loss measurement spirals waveguides, where the wires are bent at 20 μm radius to form spirals. In this scenario, the radiation loss for narrow wires (long treatment time) in the bend is much larger than the relatively wide wires. In addition, since the crystal planes are different in the bend a smooth bend is not possible. Hence it can be arguably concluded that the bends in the photonic wires are the primary cause for the loss in addition to waveguide width.

3.6.3 Si reflow

Reflow of waveguide pattern is a standard roughness reduction technique in polymer waveguides. Since the glass transition temperature of polymers is low they can be melted at relatively low temperatures ($<300^o$C). Si on the other hand, requires temperatures over 1412 ^{o}C for plastic deformation at atmospheric pressure. However, in a hydrogen (H) environment Si can be melted at 800-900 ^{o}C which is about 50 $\%$ below the melting point [39]. During the reflow process Si atoms migrate from peak and valley points on the surface to form energetically stable smooth surface. The migration of the atoms depends on the crystal orientation, atoms can be moved from one plane to the other without losing the volume. As a consequence, the migrating of Si atoms can changes the profile of the existing feature. The migration of atoms can be controlled by the process conditions, such

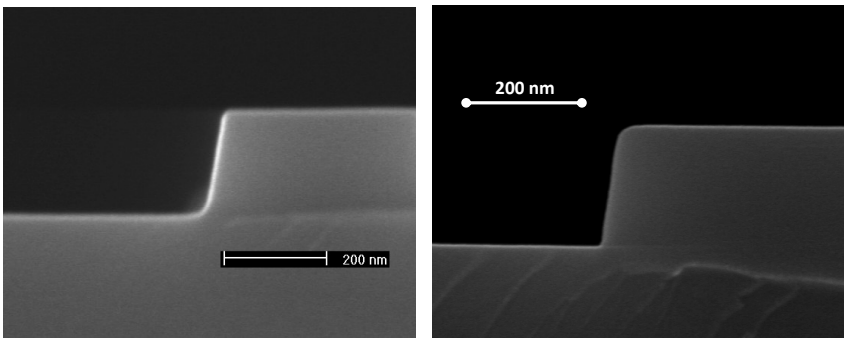


(a)



(b)

Figure 3.42: Effect of TMAH treatment on (a) the profile of photonic wires, profile extracted from the sidewall AFM characterization and cross-section SEM and (b) propagation loss of the photonic wire.



(a) (b)

Figure 3.43: Photonic wire (a) as fabricated and (b) after H anneal at 850^{o}C/756 Torr.

as temperature and pressure.

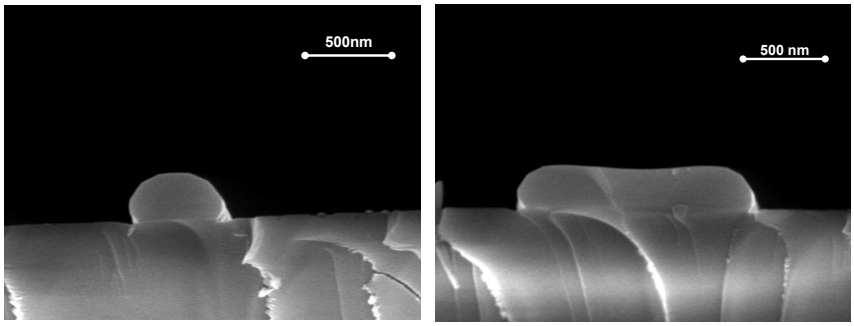
In our study photonic wires were annealed in H enviroment at 850 ^{o}C for 2 minutes at atmospheric pressure. Figure 3.43 shows the effect of H anneal on the waveguide profile. The annealing time was kept low to avoid any profile deformation, however, corner rounding already starts to appear (Fig. 3.43b). After H anneal the propagation loss of a photonic wire was reduced from 3.92 dB/cm to 2.69 dB/cm, which is an improvement of 30 $\%$. Another advantage of the H anneal process is its selectivity, similar to epitaxy. Surface covered with SiO_2 will be unaffected by the annealing process allowing controlled reflow of structures.

We have also processed photonic wires at a higher temperature (1000 ^{o}C) and low pressure (10 Torr). As mentioned earlier a directional migration is clearly observed in figure 3.44 revealing different crystal planes in the photonic wire deforming a trapezoid into a nearly circular waveguide. The shape transformation depends on the starting waveguide cross-section. A high aspect ratio (height/width) feature would result in a circular form while a low aspect ratio feature would result in a toroid like profile (Fig. 3.44b).

Surface roughness smoothening by Si reflow is an attractive technique. Smoothing can be done selectively by using SiO_2 masking. However, the aspect ratio dependent profile change should be carefully considered while applying this technique to preserve profile integrity. Novel innovative device configurations can be made using this approach, such as high-Q Si toroid, and spheres. Negligible Si loss and easy integration with CMOS process are an added advantage of this approach.

3.6.4 SCROD treatment

Cleaning a Si surface using wet chemicals is a standard process in CMOS. Standard cleaning procedure involves particle and organic contamination removal. Both processes involve oxidation. Organic clean is achieved by oxidizing the contam-



(a) (b)

Figure 3.44: Profile transformation of (a) low and (b) high aspect ratio photonic wire as a consequence of H anneal at 1000^{o}C/10 Torr.

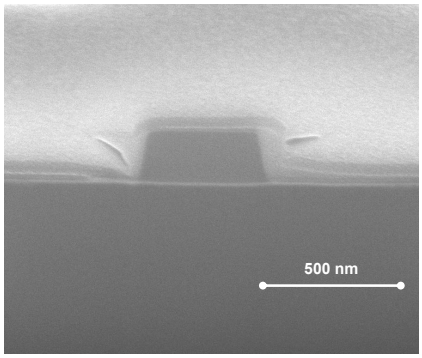


Figure 3.45: Cross-section of a photonic wire after 10 cycle SCROD clean, showing no undercut of BOx.

inant while Si oxidation is used for particle removal. A self-limiting oxidation and subsequent oxide removal lifts off particles from the Si surface resulting in an oxide-covered Si surface. Ammonium peroxide ($NH_4OH : H_2O_2$) or APM is the most prevalent cleaning chemical mixture used for particle removal. It is also referred to as SC-1 mixture. Successive oxidation can results in roughness reduction depending on the starting roughness. It has been shown that by using SC-1 in combination with oxide etching hydrofluoric acid the propagation loss of a photonic wire can be reduced by 65 $\%$ [36]. Even though the sidewall roughness of the photonic wires was reduced the process induced additional roughness on the top surface.

In this work, we use a similar technique but with a different approach. We use Spin Cleaning with Repetitive use of Ozonated water and Dilute hydrofluoric acid, also known as SCROD. In this approach, ozonated water is sprayed on to the wafer, which forms a thin chemical oxide, which is then removed by spraying dilute

hydrofluoric acid. This sequence can be repeated a number of times to achieve desired surface quality. Figure 3.45 shows the cross-section of a photonic wire after 10 cycles of SCROD clean. Since the etch rate of the exposed BOx is higher than the chemical oxide, we did not observe undercut of BOx (Fig. 3.45). After treating with SCROD, the propagation loss of photonic wires was characterized and compared with the untreated reference. We have found that by using 10 cycles SCROD clean the propagation loss has been reduced from 5.29 to 3.38 dB/cm, which is 64 $\%$ reduction in propagation loss. Increasing the number of cycles did not reduce the loss further indicating a saturation of surface modification reaction.

Since SCROD is one of the cleaning techniques used in a standard CMOS process it can easily be integrated in the fabrication process flow. Unlike Si reflow and anisotropic etch, the process preserves dimensional and profile integrity.

3.6.5 SiO_2 smoothening and passivation

As mentioned earlier oxide growth reduces surface roughness in Si. The thickness of SiO_2 formed using a wet chemical process is limited to few 10's of angstroms, hence high temperature process is required for thicker layer growth. In addition to roughness reduction, SiO_2 passivates the surface defect in combination with passivation anneal in hydrogen (H) atmosphere. The oxide layer acts as capping layer for passivation H atoms in the defects providing stable passivation. By using such a approach the scattering loss and surface absorption loss can be addressed together.

We used dry thermal oxidation to grow 5 nm of SiO_2 on a photonic wire at 950^{o}C in oxygen. The SiO_2 layer consumes $\approx$50 $\%$ of Si, hence only 5 nm of the lateral dimension and 2.5 nm of the thickness is consumed. After SiO_2 growth, the wafer is annealed in forming gas (10$\%H$/90$\%N$) at 450 ^{o}C for 30 minutes. The annealed photonic wires were then characterized for propagation loss and compared with the as fabricated reference photonic wires. Optical characterization reveals that by dry oxidation and forming gas anneal the propagation loss is reduced by 25 $\%$, from 3.2 dB/cm to 2.4 dB/cm. The reduction in the loss is a consequence of the reduction in sidewall roughness and passivation.

3.7 Conclusion

In this chapter, we presented the high resolution fabrication technology for silicon photonic devices using advanced CMOS technology. 193 nm optical lithography and inductively coupled plasma dry etching process were developed to achieve high resolution and uniformity. Both processes were optimised to achieve a uniformity of $<$1 $\%$ of actual dimension for photonic wires and $<$2 $\%$ for photonic crystals. We have explored the suitable lithography condition to achieve overlapping process windows for fabrication of photonic wires and photonic crystals with single illumination without compromising uniformity. Low proximity effect

(4 nm) in photonic crystal waveguides was achieved by using appropriate optical lithography settings. A tunable sidewall angle was demonstrated by changing the dry etch process chemistry. Two different etch depth were developed for fiber couplers (70nm) and photonic wires (220nm). Using the developed process we have demonstrated photonic wire low as low as 2.7$\pm$0.1 dB/cm and bend loss of 0.009, 0.015 and 0.028 dB/90^{o}bend for bend radius of 5, 3 and 2 μm respectively. The propagation loss of a W1 photonic crystal waveguide was measured to be 13.72$\pm$0.4 dB/cm. In addition, we have also fabricated and characterized two wavelength selective devices, ring resonator and mach-zehnder interferometer.

In order to reduce the propagation loss of a photonic wire, we explored post treatment schemes to reduce scattering and surface absorption loss. Four schemes was explored; anisotropic wet etch, Si reflow, successive wet oxidation and oxide removal, and thermal oxidation. Since an anisotropic wet etch resulted in profile transformation the propagation loss increased after treatment. However, other schemes gave an improvement of 30, 64 and 25 $\%$ for H annealing, SCROD, and SiO_2 smooting and passivation respectively.

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4

Uniformity of Silicon Photonic Devices

One of the major issues in using a high index contrast platform such as SOI for photonic devices is its sensitivity to dimensional variations. Deviations in the width or the height of the devices will cause a proportional shift in the spectral response of these devices. These variations affect standalone devices such as rings, where they result in a shift of the resonance frequency, but also discrete parts of larger devices such as the delay arms in an arrayed waveguide grating, where they typically result in increased crosstalk. Variations in device dimensions (width or height) down to mono-layers of atoms can be measured from the spectral response. By taking advantage of the thermo-optic effect in silicon, thermal tuning can be employed to compensate for nonuniformity, but the power required for tuning is proportional to the as-fabricated device nonuniformity [1]. To reduce power consumption for tuning high device uniformity is an absolute necessity.

Even though most of the silicon photonic devices are fabricated with e-beam lithography, there is some literature addressing reproducibility issues. Barwicz et al in [2] demonstrated spectral matching of two rings in a second order ring filter with high accuracy (26 pm) using e-beam lithography. The reliability of high resolution e-beam resist on the device response was recently presented in [3]. Xia et al in [4] used e-beam lithography to fabricate optical buffers using multiple notch ring resonators, showing a spectral non-uniformity of 0.46 nm. Though these papers directly or indirectly address the issue of uniformity, there are no studies yet addressing the issue in a holistic way.

Reproducibility of devices within a chip, chip-to-chip, and wafer-to-wafer depends on various factors, but fabrication imperfection is one of the main causes

of variation. Though the device design can be adapted to accommodate fabrication tolerances (design for manufacturability), in order to make fabrication tolerant devices the fabrication process limitations should be studied first.

This chapter addresses the non-uniformity issues related to fabrication and circuit design. First, we briefly illustrate the effect of dimensional non-uniformity on integrated optical devices. A detailed introduction on different types of non-uniformity and the respective sources is presented. The uniformity of the fabrication process presented in chapter 3 and its effect on wavelength selective devices along with circuit design are also presented. Finally, two proposals are made, one for closed loop device design for tolerant devices and secondly for a litho-centric adaptive fabrication process for better process uniformity.

4.1 Effect of variability on Silicon photonic devices

The high refractive index of the SOI waveguide platform can be exploited for making waveguides with very high modal confinement and micrometer scale bends, shrinking the size of integrated circuits by several orders of magnitude. However, at the same time this results in a very high sensitivity to fabrication variations making it difficult to achieve good uniformity within a device, from device-to-device, and from chip-to-chip.

$$\frac{d\lambda}{\lambda} \approx \frac{dn_{eff}}{n_{eff}} \tag{4.1}$$

The spectral response of any photonic wire-based optical device depends on the effective index (n_{eff}) of the photonic wire, which is for a given waveguide structure fully determined by its width and height (Eq. 4.1). Therefore, any change in the latter two parameters will change the effective index of the photonic wires and as a consequence the spectral response of the device will shift accordingly. In case of deposited materials, such as amorphous silicon, the material composition uniformity affects the effective index in addition to the device cross-section.

Using a film mode matching method the change in the effective index as a function of the dimensions was calculated, for a waveguide with nominal dimensions of 500 nm (width) by 220 nm (height). Figure 4.1 show the change in n_{eff} of TE_0 mode as a function of width and height respectively. Also the sensitivities $\frac{dn_{eff}}{dW}$ and $\frac{dn_{eff}}{dh}$ are shown. From $\frac{dn_{eff}}{dW}$ we can clearly see that around a width of 400 nm n_{eff} is very sensitive, while at larger waveguide widths the sensitivity is reduced. This is a consequence of the high confinement (fill factor) of the optical mode at a width of 400 nm. At the nominal waveguide dimensions, n_{eff} changes by 0.0013/nm and 0.0036/nm for a change in the waveguide width and height [5], corresponding to a ≈1 nm/nm (width), and ≈2 nm/nm (thickness) shift in the resonance wavelength of the devices. However, to accurately determine the resulting resonance wavelength shift for a device, the width and height changes in any device should be integrated over the length of the device. Hence it is important to note that for uniformity, the average width and height of the devices should be

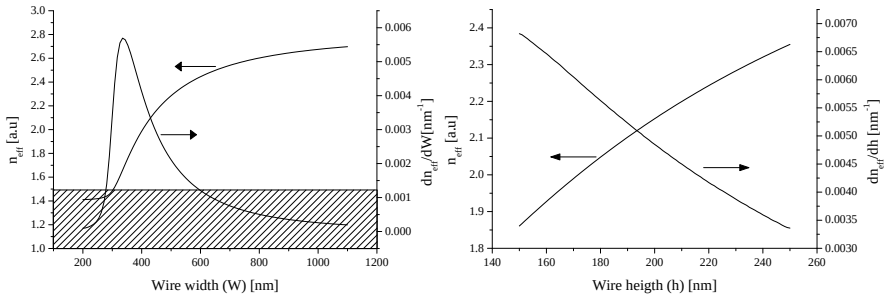


Figure 4.1: (a) Sensitivity of effective index of the TE_0 mode to photonic wire width at 1550 nm. The height of the wire is 220 nm and (b)Sensitivity of effective index of the TE_0 mode to photonic wire height at 1550 nm. The width of the wire is 500 nm

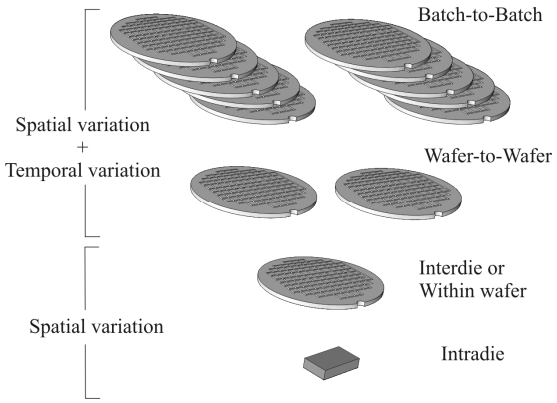


Figure 4.2: Spatial and temporal variations.

matched over the length-scale of a typical device, rather than the absolute local width and height of the devices.

4.2 Classiffication of variability

The variations in spectral response between devices may originate from two types of sources: environmental and physical factors. Environmental factors such as, temperature of the chip, input power, etc... affect the devices during operation. Physical factors during manufacturing result in structural variations that are essentially permanent. The distribution of the variation could be randomly or systematically distributed over time and space. An important factor in controlling such

variation is to isolate the systematic, repeatable or deterministic contributions to the variations.

The permanent structural nonuniformity in devices is obviously influenced by the fabrication process employed in making them. The variation in the process manifests itself across time and space. Temporal process variation is often related to drift in consumables, changes in the incoming wafers or process conditions over time. For example, the ageing of photoresist often changes the viscosity and contrast, thereby directly affecting the printed dimensions. Temporal variation is of critical concern in a mass manufacturing environment and results in nonuniformity from wafer to wafer and batch to batch. Besides temporal variation, spatial variation over the wafer also plays an important role in non-uniformity during the fabrication process.

At the wafer level we can separate sources of physical or structural variation into two categories: intra-die and inter-die(or within wafer) nonuniformity. The magnitude and distribution of variations within a die can be different from those between dies (die-to-die). Fig.4.2 illustrates these variations at different levels.

Fabrication of photonic devices goes through two types of processing steps: (a) wafer level processes such as deposition, resist/bottom anti-reflection layer thickness, CMP, baking and etching, and (b) die level processes such as optical lithography. The wafer level variation is often referred to as global variation and die level is referred to as local variation. Nonuniformity in wafer level processes can result in a shift of the average linewidth from die-to-die. Die level processes and in particular optical lithography can introduce additionaly nonuniformity. The uniformity in scanning a die depends, amongst others, on the mask quality, pattern density in the mask and projection optics in the tool.

4.2.1 Inter-die non-uniformity

Nonuniformity between dies, which are fabricated on the same wafer, or on different wafers is referred to as inter-die nonuniformity. Inter-die nonuniformity generally is caused by the fabrication tool and process design. Inter-die nonuniformity often has a specific signature on the wafer. A CMP process for example creates a radially varying thickness from the centre to the edge of the wafer. Since the dies are spatially distributed over the wafer, the inter-die uniformity will be affected by thickness variation of Si, BARC, and photoresist over the wafer and plasma non-uniformity during the dry etch process. Knowledge of inter-die variation is essential to clearly identify different sources of non-uniformity and it is relatively easy to extract the sources of inter-die non-uniformity compared to intra-die nonuniformity.

4.2.2 Intra-die non-uniformity

Intra-die non-uniformity is the deviation occurring spatially within a die. Contrary to inter-die variation, which affects all the structures on a die equally, intra-die nonuniformity affects individual structures on the same die, resulting in mismatch

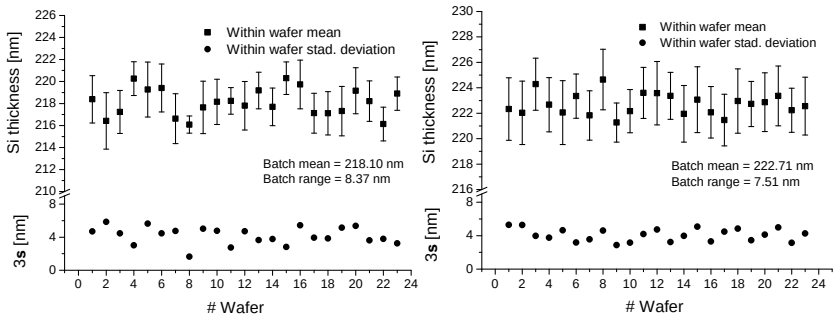


Figure 4.3: Within a batch and batch-to-batch Si thickness non-uniformity (a) Batch 1 and (b) Batch 2. The thickness of silicon was measured using spectroscopic ellipsometry.

between identical devices on a die (or even within a single device). Since each die is a replica of every other, in most cases, the fingerprint intra variation within one die can be seen in all other dies. Intra-die nonuniformity can manifest itself on different length scales. With a die size of 8×12 mm^2, the variation in the lithography and dry etch process can affect linewidth on a μm length scale, while the Si thickness variation affects the device on a mm length scale. For instance, during optical lithography, the non-uniformity in the energy along the scanning slit can create a systematic intra-die variation [6]. Furthermore, local device density variation can have non-uniformity due to dry etching [7, 8].

Unlike the wafer level processes, it is easy to extract the systematic variation in a given die. Even though, it is obvious to observe such systematic variation it is often difficult to clearly understand the source of such variation. Therefore, any attempt to control the variations should start with complete information about the mask (resolution, layout, pattern density, etc), local and global variations.

4.2.3 Batch-to-Batch (BtB) and Wafer-to-wafer (WtW) non-uniformity

In a production environment, process stability over time is critical for reliability. Large volumes of wafers are processed in batches, a batch can be a single wafer or a collection of wafers. The number of wafers per batch depends on the protocols used in different production lines. These batches are not necessarily processed at the same time leading to batch-to-batch(BtB) and wafer-to-wafer (WtW) non-uniformity. In addition to intra- and inter-die uniformity, BtB and WtW uniformity is as a serious concern in a high volume production environment. For instance, figure 4.3 shows the thickness variation of the top Si layer of two batches of SOI wafer. It is evident that WtW and BtB mean thickness and non-uniformity are fairly unrelated. The BtB and WtW uniformity as mentioned earlier strongly relies

on the process design and maintenance, hence monitoring and correcting each step in the fabrication process is vital for process reliability (Section 4.6).

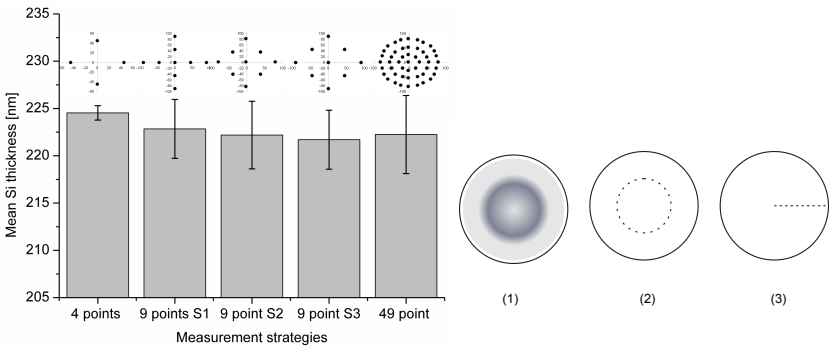
4.2.4 Critical Dimension Metrology

The two physical dimensions that define a photonic integrated device are the height (or thickness) and lateral dimension(linewidth , hole diameter and trench width). In a standard CMOS fabrication line, spectroscopic ellipsometry and critical dimension - scanning electron microscopy(CD-SEM)[1] are used to characterize thickness and linewidth , respectively. With an appropriate optical model (refractive index-n and extinction coefficient-k) the thickness of the layers can be measured accurately using ellipsometry. Recently scatterometry is widely used as a metrology tool to simultaniously extract linewidth and height of a two dimension structure. This technique is superior to CD-SEM in two aspects; speed and accuracy. However, the process has to be only used for one dimension periodic structures, such as, line gratings and not for photonic crystals [9, 10] . In this work, we did not use scatterometry for dimensional measurements.

Over a 200 mm wafer, using automatic measurement techniques a larger number of locations can be measured quickly without manual intervention. However, for a full batch of wafers it still requires a considerable amount of time. Hence an appropriate number of measurement locations which represents the full wafer statistics should be used. For a process which has radial variation, the measurement location should represent the wafer variation in order to extract the real variation. For instance, figure 4.4b(1) shows a process which has radial distribution. A circular measurement scheme (Fig. 4.4b(2)) will underestimate while a radial scheme can over-estimate. Hence a combination of circular and radial must be employed to extract the real variation. Figure 4.4a shows a comparison between the number of measurement points and their location on the wafer statistics, in this case average Si thickness over a 200 mm SOI wafer. The scheme designated as 9pointS2 measures 9 locations and gives a close estimate to a 49 point wafer statistics. Hence by using fewer measurement points and at the same time choosing an appropriate site scheme the full wafer statistics can be extracted.

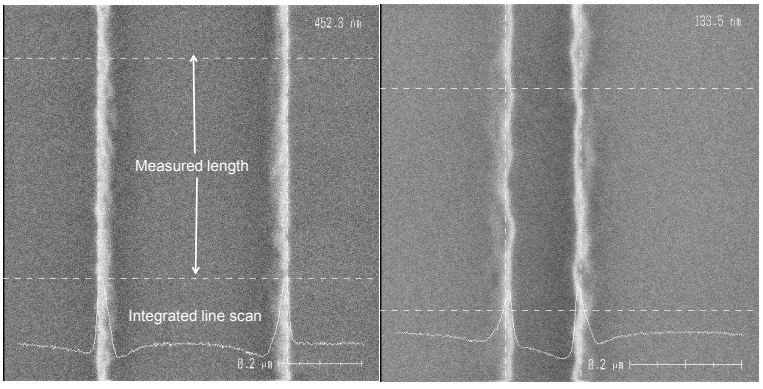
As mentioned earlier the lateral dimension of a feature is measured using a CD-SEM. The linewidth is measured using an in-built image processing algorithm, which measures the CD from the image contrast along the edge of the structure. Figure 4.5 shows a SEM image of a photonic wire and a trench, where the linewidth and trench width are extracted from integrating the line scan across the width of the feature over a length of $\approx$1000 nm. A threshold on the integrated contrast is defined to extract the lateral dimension of the feature. An appropriate measurement algorithm is set up by correlating the CD-SEM measurement with cross-section SEM characterization. Since the measurement algorithm is sensitive

[1] In CMOS fabrication process, CD refers to the critical dimension of the structure in a particular circuit. For instance, in a wire based circuit the waveguide width is the CD of the circuit. Likewise in a photonic crystal circuit the hole diameter and pitch are the CD of the circuit. Typically, CD-SEM refers to dimension of measurement of lateral dimension of the feature from top of the device.



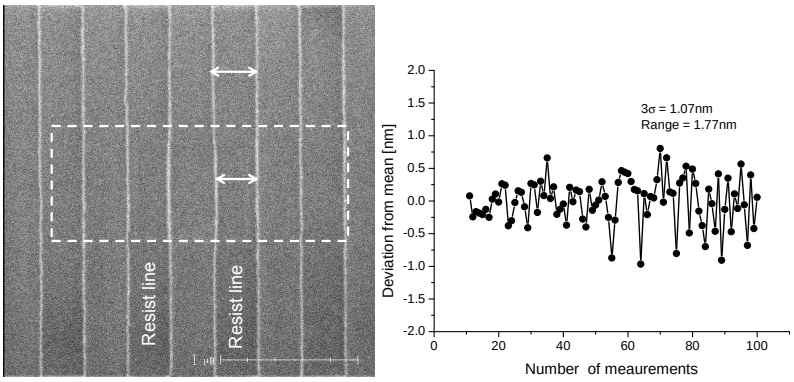
(a) (b)

Figure 4.4: (a) Different thickness measurement schemes and its consenquence on the average Si thickness. and (b) Two possible addressing schemes (2) and (3) for radial variation over the wafer as in (1).



(a) (b)

Figure 4.5: Linewidth measurment from CD-SEM (a) Photonic wire and (b) Trench.



(a) (b)

Figure 4.6: (a)Photoresist shrinkage due to electron beam exposure and (b) Reproducibility of linewidth of a photonic wire in silicon.

to sidewall angle of the feature separate algorithms were used for patterns in photoresist and Si. The pattern in photoresist have vertical sidewalls compared to the pattern in Si.

The CD-SEM characterization influences the examined device. Photoresist shrinkage due to electron beam exposure is an intrinsic issue with advanced photo resists [11]. Figure 4.6 shows photoresist shrinkage, which was intentionally exposed for few seconds with an electron beam. It is impossible to completely avoid photoresist shrinkage while measuring. However, it can be reduced through appropriate measurement schemes. A simple approach to reduce shrinkage is to reduce the exposure time of the electron beam by using an automatic focusing scheme.

In addition to absolute dimensional measurement, repeatability is important for reliable measurements. Even though repeatability is one of the tool specifications, it has to be qualified for a particular application. In our case, a measurement accuracy of $\pm$ 4.5 nm is acceptable to characterize the non-uniformity of a 450 nm photonic wire. Figure 4.6a shows the repeatability of a linewidth measurement on a 450 nm photonic wire in Si. The measurement algorithm shows an accuracy of 1.77 nm with a 3σ of 1.07 nm, which is well within our requirement. The absolute value and repeatability of measurement also depends on the resolution or magnification. Therefore, we used the same magnification for all the linewidth and hole diameter measurements throughout this work.

4.3 Fabrication process characterization

During the fabrication process, each step is a potential source of non-uniformity. Assuming uniform material properties over a 200 mm wafer, the thickness and linewidth are the two primary factors that influence the device non-uniformity. In the following section, the thickness and linewidth uniformity of the fabication

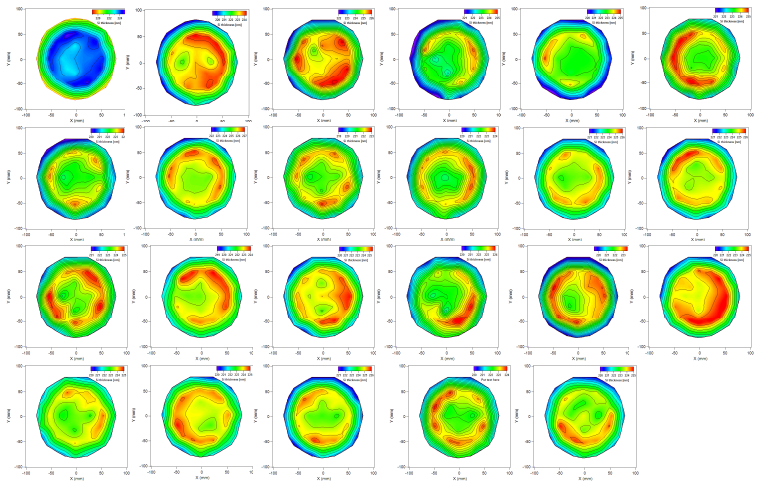


Figure 4.7: Thickness uniformity of silicon from a batch of 23 SOI wafers.

processes are presented.

4.3.1 Layer thickness variability

The three critical thicknesses that need to be monitored and controlled are the Si thickness in the SOI wafer and the photoresist and BARC thickness during optical lithography. Before optical lithography the thickness of the Si layer in a 200 mm SOI wafer was measured using ellipsometry. Within a wafer, a radial thickness variation (Fig.4.7) is observed, which is typical for a process involving a CMP process [12]. For a typical wafer, we observe a thickness range (T_{max}-T_{min}) of 3 nm radially from the centre to the edge of the wafer and a full wafer range of 7.1 nm. Furthermore, within a shorter distance scale of 10 mm, the thickness varies as much as 1 nm, which will cause observable device non-uniformity within a die. The average thickness and its non-uniformity can vary from WtW and BtB. Figure 4.7 shows such variation from a batch of 23 wafers where the finger print radial thickness variation is observed for all the wafers. Table 4.1 summarizes within wafer, WtW and BtB thickness statistics of SOI wafers from the same wafer vendor. The BtB non-uniformity was measured from 5 batches of wafers. In order to avoid spurious data points we used an edge exclusion of 10 mm for all of our thickness measurements. The edge of the wafer is mostly unusual for a variety of reasons. Some of them are, high non-uniformity, contamination due to wafer handling and non availability of enough space for a full chip.

The thickness of the BARC and photoresist used in the lithography process influences both the absolute linewidth and the linewidth uniformity. The thickness of these layers was also measured using ellipsometry. To simplify the complexity of the model used for ellipsometry, the uniformity of the BARC and photoresist lay-

	Within wafer	Wafer-to-Wafer	Batch-to-Batch
Wafer mean (nm)	219.1	218.10	221.25
Wafer stand. dev. (nm)	2	1.26	2.14
Wafer range (nm)	7.1	4.22	5.27
Wafer stand. dev. ($\%$)	0.9	0.58	0.97
Wafer range ($\%$)	3.2	1.93	2.38

Table 4.1: Summary of Si thickness metrology after 10mm edge exclusion.

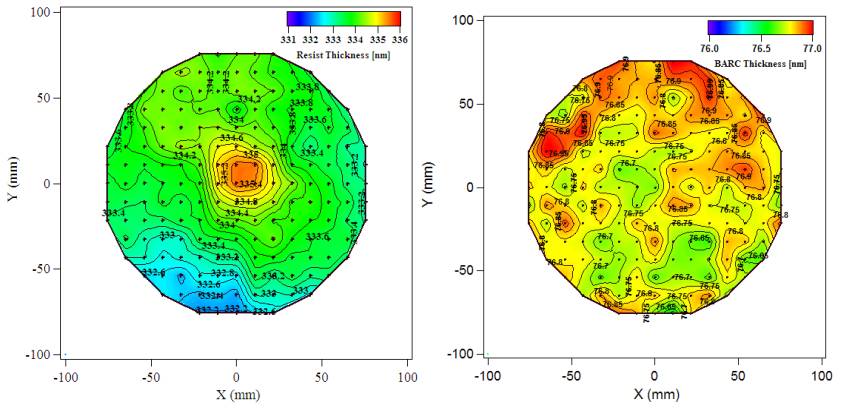
	BARC	Photoresist
Wafer mean (nm)	76.8	333.7
Wafer stand. dev. (nm)	0.09	0.7
Wafer range (nm)	0.5	3.4
Wafer stand. dev. ($\%$)	0.1	0.2
Wafer range ($\%$)	0.5	3.4

Table 4.2: Summary of Photoresist and BARC thickness metrology after 10mm edge exclusion.

ers was characterized by coating them on a bare silicon wafer. Table 4.2 summarizes the thickness characterization of the two layers. The BARC and photoresist thickness is controlled down to sub-nanometer non-uniformity, which is crucial in achieving a reproducible lithography process. Figure 4.8a & b illustrates the thickness variation of 330 nm photoresist and 77 nm BARC layer respectively. Over a 200 mm wafer, we observe photoresist thickness variation of 3.4 nm, while the BARC layer variation is 0.5 nm. This thickness variation will result in photoresist linewidth variation of $<$ 0.3 nm (Chapter 3), which is less than the measurement limit of the CD-SEM but will be noticeable in optical measurements. The achieved uniformity is well within in the target uniformity of ± 1 $\%$ within a 200 mm wafer.

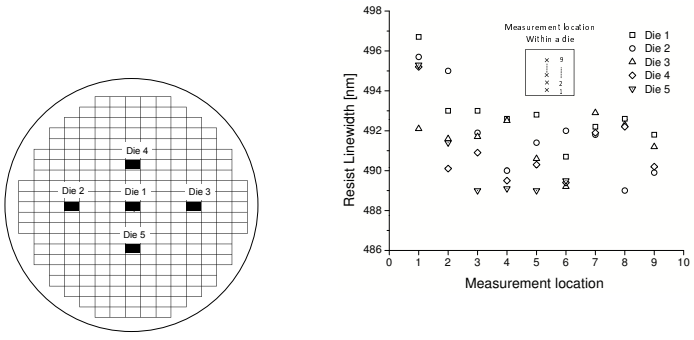
4.3.2 Linewidth variability

The linewidth of the photonic wire after lithography and after dry etch was measured using CD-SEM inspection. The uniformity was characterized by measuring a 450 nm photonic wire measured at the same location from die-to-die. The linewidth measurement was automated, which reduces the measurement errors. Fig.4.10a and Fig. 4.10b show the linewidth uniformity over a 200 mm wafer. We achieved a linewidth uniformity of 0.45$\%$ after the lithography process and 0.76$\%$ after the etch process respectively (standard deviation over the wafer). Table 4.3 summarizes the measurement statistics. The average linewidth of the photonic



(a) (b)

Figure 4.8: Thickness uniformity of (a) Photoresist and (b) Bottom anti-reflective coating (BARC) .



(a) (b)

Figure 4.9: Intra die photoresist linewidth uniformity after optical lithography (a) location of the dies on the wafer (b) linewidth within a die.

	Linewidth	
	After Lithography	After Etch
Wafer mean (nm)	450.9	469.8
Wafer stand. dev. (nm)	2.01	2.59
Wafer range (nm)	5.5	7.5
Wafer stand. dev. ($\%$)	0.45	0.76
Wafer range ($\%$)	1.22	1.61

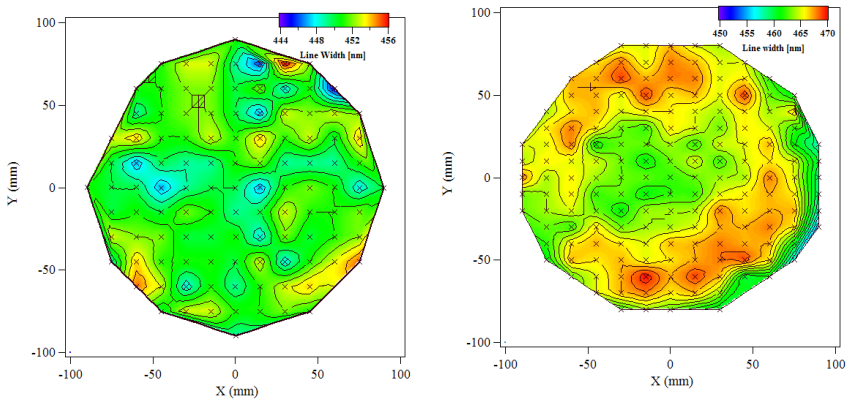
Table 4.3: Linewidth statistics of a photonic wire(450nm) after optical lithography and dry etch Target linewidth = 450 nm.

wire increases by 19 nm after dry etch, due to the sloped sidewalls of the photonic wires. This increase in linewidth can be compensated for by adapting the exposure dose such that following lithography the linewidth is reduced by 19 nm.

The linewidth measured in the resist pattern (Fig.4.10a) does not show any systematic variation over the wafer, which implies that there is no observable systematic variation from die-to-die (or within wafer) coming from optical lithography. The linewidth uniformity is a consequence of highly uniform photoresist and BARC thickness over the wafer. After the dry etch process (Fig. 4.10b) we see a donut shaped variation, typical for a plasma process and this is caused by a variation of reactive species in the plasma. The final resulting linewidth variation over the wafer of 0.76$\%$ meets our specification of $<1\%$.

Since we are using a step-and-scan based lithography process, local variations in the lens system, mask or scanning system will result in a reproducible variation within a die. These variations can be deduced from measuring photonic wires at multiple locations within a die, and comparing it to similar measurements from neighbouring dies. Figure 4.9 depicts intra die linewidth variation from 5 dies after the lithography process. We can clearly see that for all the dies, the linewidth of the photonic wires at the bottom of the die (numbered 1-3) is on average larger than that for the other wires. This variation can be attributed to a systematic error, e.g. in the mask, which is replicated in every die. We also observed a good correlation between this linewidth variation and the device response (see section 4.2.2). As all dies are replicas, after dry etch the lithographic finger print will be preserved, but with a shift in the mean linewidth. This shift in the mean linewidth is due to plasma non-uniformity during the dry etch process. In addition to within wafer and within die uniformity, wafer-to-wafer reproducibility shows good process stability. Figure 4.11 shows an average CD variation of a photonic wire from wafer-to-wafer.

The top down CD-SEM linewidth measurement of photonic wires over a 200 mm wafer gives a good indication of the uniformity. However, it does not reflect the absolute device uniformity. As discussed earlier, the photonic device response depends on the average linewidth variation over the length of a device and not on the absolute linewidth. With the CMOS characterization tools and



(a) (b)

Figure 4.10: Linewidth uniformity over a 200 mm wafer after (a) optical lithography (photoresist) and (b) dry etch (silicon wires).

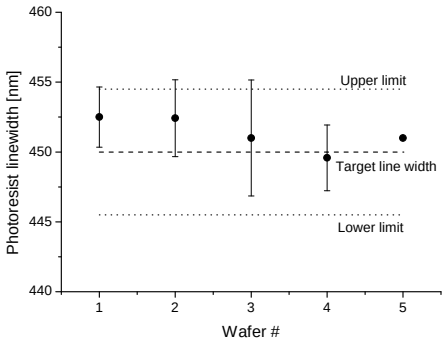


Figure 4.11: Wafer-to-Wafer linewidth uniformity.

algorithms available at the moment it is not possible to accurately measure the average linewidth over a distance of few 10's of micrometers and therefore, optical characterization is the only way to characterize actual device uniformity. This is described in the following section.

4.4 Wavelength selective device non-uniformity

To characterise the process uniformity, we designed a number of suitable test devices and circuits. Since almost all Si photonic devices are sensitive to dimensional variation we have a wide variety of components to choose from. We used the following devices to study the short and long range device non-uniformities; all-

Layout	Test device	Purpose
Layout-1	Race-track ring notch filter, Mach-Zehander interferometer	Intra & Inter die uniformity
Layout-2	1×8 arrayed waveguide gratings	Intra die uniformity
Layout-3	1×8 racetrack ring (de)multiplexer	Intra & Inter die uniformity
Layout-4	1×4 racetrack ring (de)multiplexer	Within Wafer uniformity

Table 4.4: Details of different layout used to study device non-uniformity.

pass racetrack ring resonators (RTR), 1×1 mach-Zehnder interferometers (MZI), 1×8 racetrack ring (de)multiplexers, 1×4 racetrack ring drop (de)multiplexers and 1×8 arrayed waveguide gratings (AWG). These are all interferometric devices and variations in the spectral response directly reflect any variation in the dimensions (width and height) of the photonic wire.

Layout-1 for short and long range non-uniformity of compact devices

The devices were arranged in such a way that both short and long distance non-uniformity could be studied. RTR's and MZI's were placed in pairs of two on two locations of the die (Fig.4.12top). The distance between two devices in a pair was 25 μm and representative for short-range uniformity. The distance between the two pairs was 1700 μm, which is suitable for long-range uniformity assessment. The RTR's were designed with a ring radius of 4 μm, a coupling length of 4 μm, and a coupling gap of 180 nm. The 1X1 MZI's had a delay length of 50 μm in one of the arms and used two Y junctions for splitting and combining the light.

Layout-2 for short and long range non-uniformity of larger devices

Unlike RTR's and MZI's, relatively large devices such as AWG's and planar curved gratings suffer from both long and short range non-uniformities within a single device. We used AWG's as test structures to study these influences. The AWG's were arranged in an array of rows and columns, with each AWG having a closest neighbour at 250 μm, while the farthest distance between two arrays was 4500 μm (Fig. 4.12bottom). In total 18 devices cover an area of 0.7×6 mm^2 in each die. The 8-channel AWG's were designed to have a channel spacing of 400 Ghz. They have a footprint of 200×35 μm^2 each. The relatively large footprint of the array of AWG's enables us to study the effects of long length scale variation within a die.

Layout-3 for intra-die exposure slit non-uniformity

Identical 1×8 ring (de)multiplexers were placed in six locations over the die to study the non-uniformity within a die. Intra-die variation sources include device density as a result of circuit design (Layout-4) and lithography variations, such as

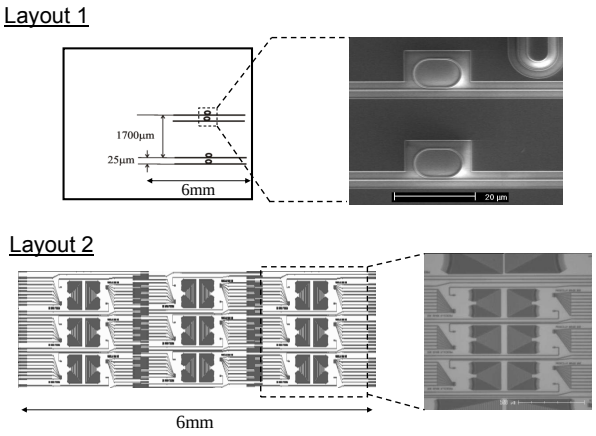


Figure 4.12: Within die non-uniformity test device Layout-1 and -2.

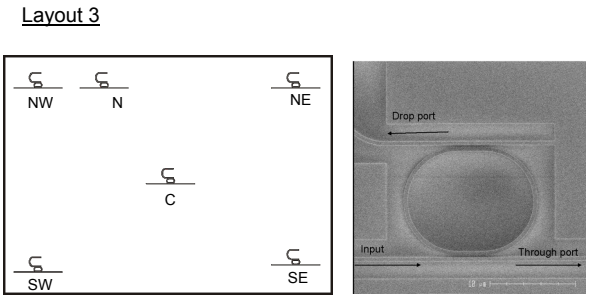


Figure 4.13: Within die non-uniformity test device Layout-3.

exposure dose variation due to slit non-uniformity in the mask. During fabrication the slit moves either from top-to-bottom or bottom-to-top of the die, assuming the bottom of the die is toward the wafer notch. Any intensity variation in the slit or the speed of slit motion will directly affect the illumination dose and thus the pattern dimension.

A ring based (de)multiplexer is used as a test device formed by a racetack ring resonators with a bus and drop waveguide. The resonators were designed with a ring radius of 4 μm and a waveguide width of 450 nm. The coupling gap and length of all the resonators was kept constant at 200 nm and 2000 nm respectively. The location of each (de)multiplexer is chosen in such a way to extract the non-uniformity caused by exposure slit non-uniformity within in a die. Figure 4.13 illustrates the device placement and gives a SEM image of one of the fabricated devices.

Layout-4 for device density non-uniformity

Density of devices in the mask plays an important role in device uniformity. Non-uniform density of devices in the mask can create local pattern density fluctuations resulting in a non-uniform fabrication process, in particular through etch loading and stray light during lithography. The etch loading depends on the pattern density and the proximity of the neighbouring device. The pattern density can be easily modified by adding optically isolated dummy structures. Three layouts were used to study the effect of pattern density on the device response and its uniformity (Fig. 4.14).

In layout-4a, dummy devices are placed around a RTR notch filter as shown schematically in figure 4.14. The distance between the active and the dummy ring was varied between 10-40 μm, in addition, rings without any dummies were also implemented for comparison. The dummy rings were optically isolated from the active ring and bus waveguide to avoid a spurious response. This layout allows us to study the minimum distance required between the devices.

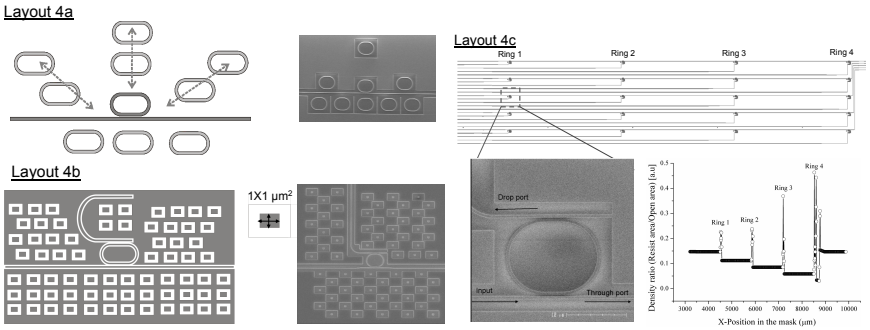
In order to have a controlled loading, the pattern density should be tunable. We used square tile dummies as shown in figure 4.14, where the gap between inner and outer square can be used to control the loading. The inner square dimension was fixed at 1×1 μm while the gap was varied. Tiles were implemented in two configurations, firstly, the loading is tuned around an active ring resonator by changing the density. Secondly, the density is kept constant and the distance between the ring and the tiles was changed.

In addition to the dummy controlled density as mentioned above, we have also used five identical 1×4 ring (de)multiplexer arranged in such a way that they naturally create a density variation on each ring filter. The resonance wavelength of each ring was de-tuned by increasing the radius of the rings. The radius of the rings was designed to be 5000, 5010, 5020 and 5030 nm, while the coupling and length were kept at 180 nm and 2000 nm respectively. Figure 4.14b illustrates the implementation of the circuit and the density variation for each ring. It can be seen that the presence of access waveguides increases the density [2] from ring-1 to ring-4. The density around ring-4 changes erratically creating an abrupt density change, which is expected to have higher non-uniformity in comparison to ring-1.

Fabrication and optical characterization

The devices mentioned above were fabricated in a 200 mm SOI wafer (220 nm Si/2000 nm SiO_2). Fabrication was carried out using 193 nm optical lithography and dry etching process as described in chapter 3. In addition, devices were also fabricated using 248 nm optical lithography and dry etch to compare the effect of illumination wavelength and etch process on the uniformity of wavelength selective devices [13] . After fabrication, the wafer was diced into individual dies and optically characterized. Optical characterization was carried out by injecting a TE polarized light from a tunable laser or a superluminescent light emitting diode and

[2] less photoresist area.



(a) (b)

Figure 4.14: Test structures for density study.

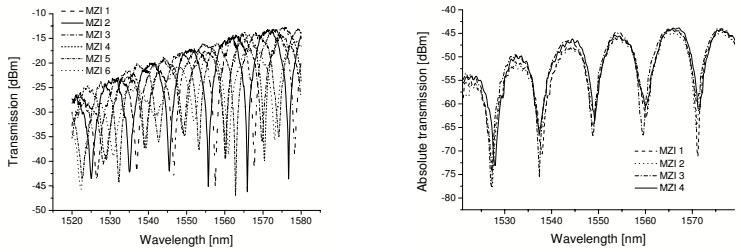
the output response is measured using either a photodiode or a spectrum analyser. The dies were secured on a vacuum chuck, which is thermally stabilized to avoid the influence of ambient temperature changes on the devices. The collected wavelength response is then analysed to extract the non-uniformity of the devices. In some cases, the output is collected through an infrared-camera, which allows parallel measurement of a number of devices. Details of the infrared-camera setup can be found in the doctoral dissertation of Dr. Katrien De Vos [14].

4.4.1 Intra-Die device non-uniformity

In general, within a die, the devices can be placed from a few tens of nanometres (coupled devices) to a few hundreds of micrometers away from each other. Table 4.5 summarizes the results for the intra-die uniformity, measured from 13 different dies, organised as shown in Layout-1 (Fig. 4.12). For MZI devices, which are located close together (25 μm) we measured an average variation of 0.2 nm for the resonance wavelength and a minimum variation of 20 pm (Fig. 4.16). Distantly spaced devices show a variation of 0.6 nm. For RTR's we respectively measured a variation of 0.15 nm and 0.55 nm.

Compared to RTR's and MZI's, AWG's are larger in size (few 10's of μm), which makes them more vulnerable to different sources of variations. Within a die, we have measured an average non-uniformity of 0.57 nm. From the spectral measurement of 17 AWG's as organized in Layout-2 (Fig. 4.12), we observe a strong correlation between the peak wavelength shift and the position of the devices (Fig.4.17). A possible origin for this rather systematic variation could be the shift in the Si layer thickness or mask error. The AWG's were spread over a length 6 mm in the die and as shown above, the silicon layer thickness can vary by over 0.5 nm over this distance. However, intra-die measurements over multiple dies shows a systematic trend, which points towards mask error rather than Si thickness variation.

The influence of the fabrication process on the device non-uniformity is de-



(a) (b)

Figure 4.15: (a) Intra die uniformity of Mach-Zehnder interferometer fabricated using (a) 248 nm optical lithography and (b) 193 nm optical lithography .

picted in figure 4.15, which shows the intra-die uniformity of MZIs fabricated using 193 and 248 nm optical lithography and dry etch. Though we have used an identical mask the non-uniformity is significantly higher for the 248 nm lithography process in comparison to the results obtained with the 193 nm lithography process. We have found an average wavelength shift of 0.7 nm and 7.3 nm for the short and distantly placed devices respectively. Reducing the illumination wavelength of the optical lithography system from 248 nm to 193 nm hence considerably enhances the process uniformity.

Layout-3 was particularly designed to extract exposure slit non-uniformity during the illumination process in lithography. Figure 4.18a shows the mean corrected resonance wavelength ($\lambda_{M-res} = \lambda_{mean} - \lambda_{res}$) deviation of the ring resonators with respect to their location within a die. The λ_{M-res} shift clearly indicates a position dependency, a red shift from west-to-east of the die. This trend is inconsistent from die to die. Figure 4.18b shows the λ_{M-res} shift trend from 5 different die's along the horizontal axis of the wafer (with notch facing south). Within a die, the blue shift becomes a red shift when moving from west-to-east of the wafer. The λ_{M-res} shift when overlapped with the linewidth variation from west to east of the wafer, a correlation of trend between them indicates an influence of global etch variation on the intra die variation. Without information of global variation the observed variation from layout-3 can be easily concluded as variation related to lithography or mask. Thus in order to extract intra-die non-uniformity it is important to isolate the global wafer scale variation.

4.4.2 Inter-Die device non-uniformity

Inter-die or die-to-die uniformity is the device uniformity between nominally identical chips within a wafer. As already discussed in section 4.2.1 inter-die uniformity is influenced by process design and wafer non-uniformity. We characterised

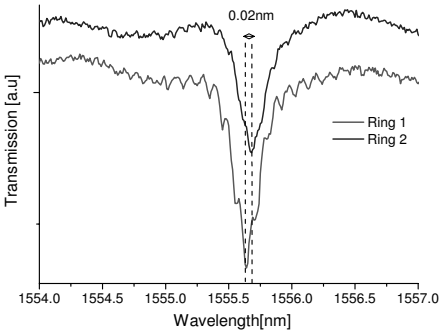


Figure 4.16: Spectral response of two racetrack ring resonators spaced 25 μm apart.

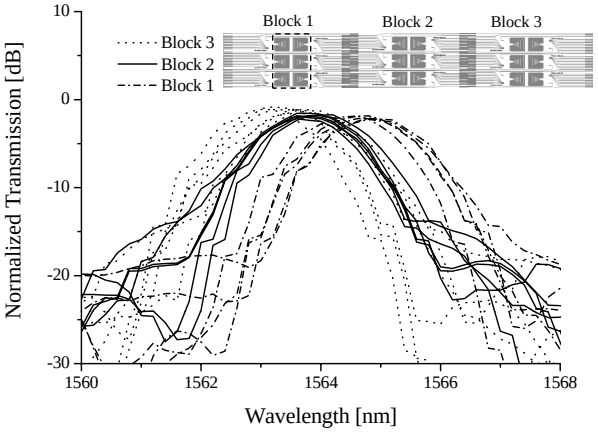
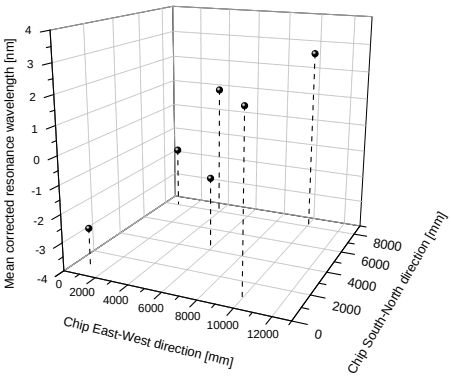
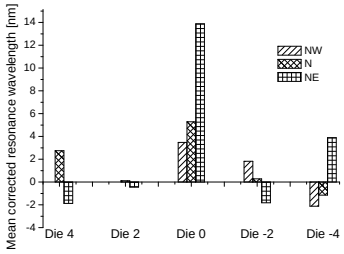


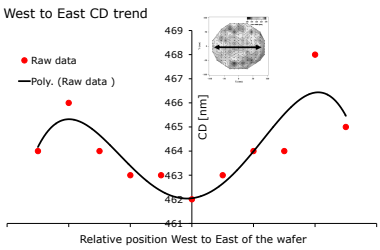
Figure 4.17: Transmission of one of the 8 channels of 17 AWG's on the same die fabricated using 193 nm optical lithography.



(a)



(b)



(c)

Figure 4.18: (a) Mean corrected wavelength shift of ring resonators (a) within a chip and (b) from chip to chip. (c) Linewidth variation of a photonic wire along the east-west direction of a 200 mm wafer.

Distance between	Mean standard deviation of $\lambda_{res}[nm]$		
device	ring resonator	MZI	AWG
25μm	0.15	0.2	-
275μm	-	-	0.54
770μm	-	-	0.52
1700μm	0.55	0.6	-

Table 4.5: Within Die/Chip device uniformity.

	Device		
	MZI	RTR	AWG
Range ($\lambda_{res_{max}}$ - $\lambda_{res_{min}}$) [nm]	2.95	3.04	1.8
Standard deviation (σ) [nm]	0.84	1.08	0.53

Table 4.6: Inter-die device uniformity.

inter-die non-uniformity by measuring 36 MZI's and RTR's from 13 different dies and 53 AWG's from 3 dies. From these measurements, we observe a standard deviation $\leq$1 nm of the resonance wavelength for all the devices (Table 4.6).

Figure 4.19a depicts the spectral response of 12 MZI's from 3 dies, which shows good uniformity. The die-to-die resonance shift of the MZI and AWG is shown in Fig.4.19b and 4.19c respectively. It can be clearly seen that all dies shows a fingerprint variation, but with a shift in the mean peak wavelength, which is in agreement with our initial argument in section 4.2.1. This shift in the wavelength as a function of device location within a die is mainly caused by mask error or non-uniformity in illumination. The shift in the mean wavelength from die-to-die is mainly caused by wafer level variation, such as Si thickness and dry etch non-uniformity. Because both show a radial varying pattern over the wafer, it is difficult to separate between both effects however. Hence special fabrication procedures, such as, rotation and shifting of the wafer would be required to discriminate between the influence of silicon layer thickness variation and plasma variation over the wafer.

4.4.3 Effect of pattern density on device non-uniformity

The effect of density of devices is studied using three different layouts as shown in figure 4.14. Firstly, figure 4.20 shows the wavelength shift as a function of distance between the ring resonator and the nearest dummy ring. We can clearly see that dummy rings as far as 15 μm could influence the device response. As the dummy rings move further, the response comes back to an isolated resonator response showing the dummy rings' influence on the resonator. The wavelength response of

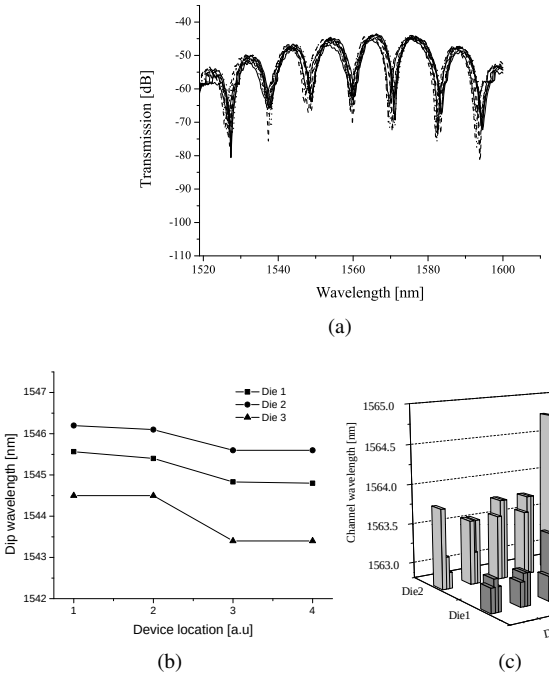


Figure 4.19: Inter die uniformity of 12 mach-Zehnder interferometer from 3 normally idential dies from a wafer (a) (a) Transmission spectrum and (b) Die-to-die resonance wavelength trend. (c) Die-to-die uniformity of AWG's within a wafer

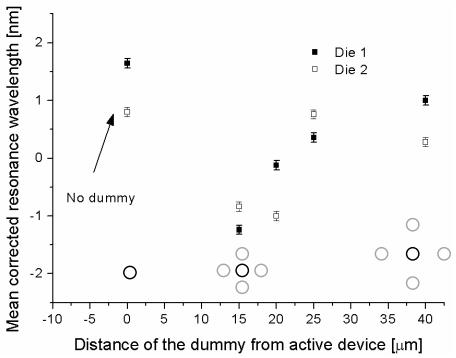


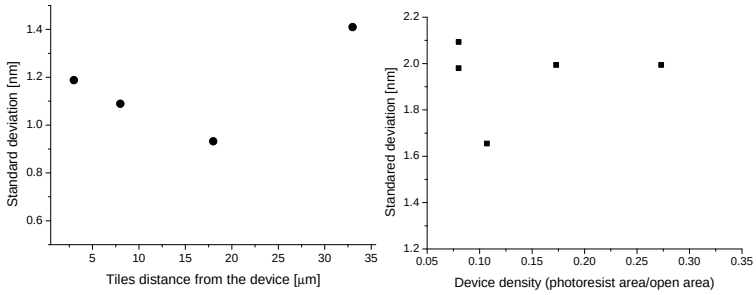
Figure 4.20: Effect of device density on absolute wavelength response of a ring resonator.

the resonators shifts towards lower wavelengths suggesting a decrease in linewidth of the resonator. Etch loading is one of the main causes of such a change in the linewidth. It is well known that the etch rate decreased with an increase in device density due to depletion of etch radicals [8, 15] . As shown in chapter 3, the amount of etch products is directly related to sidewall angle (also linewidth) variations. Hence, depletion of etch radicals in a non-uniform density environment can result in higher device non-uniformity. In order to achieve good device uniformity within in a die and a wafer, the depletion of etch radicals should be controlled. This control can be achieved through standard density control structures, such as tiles.

Figure 4.21 shows the uniformity of a ring resonator as a function of pattern density and distance of the pattern around a ring resonator. The non-uniformity was measured for 36 ring resonators from 3 dies.

We observe a slight improvement with respect to the proximity of the tiles, in the layout-4a. The tiles, which are located $\approx$15 μm from the resonator showed marginal improvement while other distances did not show improvement. This could be related to diffusion length of the etch radicals on the surface. At an optimum distance, the tiles can distribute the etch radicals evenly, resulting in a uniform environment around the device. When the tiles are moved close to the device, the presence of tiles could disturb the radical density arriving on to the device resulting in higher non-uniformity. On the other hand, the tiles that are far from the device fail to have an influence on the environment in a short-length scale (within a die).

Figure 4.22 shows within wafer device non-uniformity of 4 ring resonators with varying environment as shown in figure 4.14b. We measured 220 ring resonators from 11 dies distributed over a 200 mm wafer to extract WiW non-uniformity. In order to measure a large number of devices, in this case, we used the infrared camera setup to characterise a die at a time. Figure 4.22a shows the spectral response of 55 ring resonators from 11 dies. The bunching of spectra in figure 4.22a shows intra-die non-uniformity, which correlates well with the intra-die statistics in table 4.5. We observe within wafer standard deviation as low as 1 nm and a range



(a) (b)

Figure 4.21: Effect of device density and distance on uniformity of the ring resonator.

σ : standard deviation, R *: Range (λ_{max}-λ_{min})*

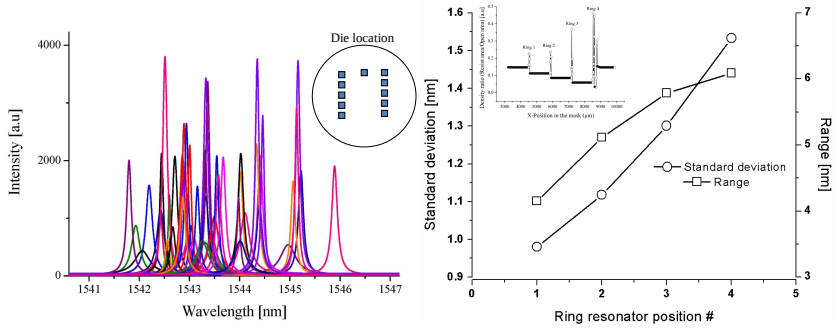
	Within chip		Within wafer	
Device	Mean σ nm	R nm	Mean σ nm	R nm
Ring1	0.3	0.89	1	4.2
Ring2	0.4	1.02	1.1	5.1
Ring3	0.4	1.08	1.3	5.9
Ring4	0.6	1.03	1.5	6.1

Table 4.7: Within wafer device uniformity statistics of 4 ring resonators with varying device density.

of 4.2 nm. It can be clearly seen that the uniformity degrades with an increase in photoresist area from ring 1 to ring 4 (Fig. 4.22). In addition to a reduction in the open area, the density changes erratically, which also contributes to an increase in non-uniformity of ring 4. The measured non-uniformity is a combination of Si thickness, lithography and dry etch non-uniformity over the wafer. In order to discriminate these variations, a large number of device measurements is required over the wafer. Since optical measurements can take few 10's of minutes per die, manual measurements can be laborious. Hence, parallel measurement techniques such as a camera based system or an automatic scanning system are an ideal solution. Even though the number of measurement points presented here forms $<10\%$ of the total sample points, it is representative of the global variation as the measured dies covers different locations in a 200 mm wafer.

4.5 Designing fabrication tolerant devices

In addition to high resolution fabrication processes, designing fabrication tolerant devices is key to achieve reliable photonic integrated circuits. As mentioned



(a) (b)

Figure 4.22: (a) Spectral response of 55 ring resonators from 11 dies over a 200 mm wafer. (b) Non-uniformity of the ring resonators with varying density environment.

earlier in section 4.1 each process step is a potential cause for non-uniformity, which can be either systematic or random. One of the good design practices is to acknowledge these variations during device and circuit design. In most cases, the effect of fabrication imperfection is ignored in the design phase leading to non-optimal device performance. In semiconductor industry, design for manufacturability (DFM) is a widely accepted method to increase device performance and yield, where circuits are designed by taking fabrication non-uniformity and distribution into account.

Design for manufacturability

Design for manufacturability (DFM) can be defined as a process of designing devices considering all the processes exerted on the device, including fabrication and operation [16, 17]. DFM is a widely used technique in microelectronics circuits, where device yield and reliability are one of the main criteria. Figure 4.23 illustrates a simple process flow to obtain an optimised design using a DFM technique, where the process and layout behaviours are considered while carrying out the device design [18]. The spatial and temporal process variation along with the layout-dependent process behavior is fed back to the designer, which helps to optimise device parameters for robust device design. The spatial and temporal variation contains the inherent process variation details. The layout-dependent process behavior contains details about the process performance as a function of density variation of the mask. DFM can be applied in the optimisation process at a different level of complexity. Wim Bogaerts et al [19] developed a closed-loop design flow which incorporated partial device fabrication and re-design of the device. This model can be further developed by adding process variability.

In addition to device design, circuit design is equally important. The placement of devices creates variation in device density resulting in non-uniformity. It

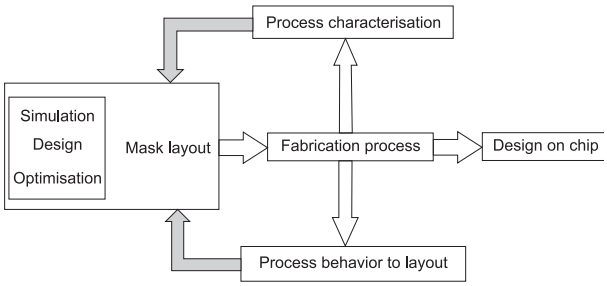


Figure 4.23: Design and fabrication process flow for design optimization.

has been clearly demonstrated in section 4.4.3 that density and distance of the devices influence absolute dimension and uniformity of the devices. Hence, while designing a photonic circuit placement of devices and density should be considered.

Optimised waveguide geometry

The dimensional tolerance of a photonic device depends on the modal confinement in the waveguide cross-section of the device. Hence optimising the cross-section for dimensionally tolerant devices is the first step in DFM for Si photonic devices. Miloš Popovic in his doctoral dissertation showed that the cross-section of the waveguide can be designed to achieve highly tolerant Si photonic devices [20]. The optimum cross-section depends on the operating polarization of the device. The optimisation was done on the bases of the confinement of the fundamental mode in the waveguide volume. He found that a cross-sectional aspect ratio (width:height) of 6:1 and 2:1 are optimal for a tolerant device cross-section for TE and TM polarization respectively.

Another way to overcome confinement and bend loss issue is to use a combination of waveguide geometries. Combining broad PhW in the straight section and narrow PhW in the bend section can allow bends with small bending radius. This approach also helps to reduce propagation process, since broad waveguides yield low propagation loss in the straight section (chapter 3). Dr. Pieter Dumon in this doctoral research found that such implementation yielded better phase error performance in arrayed waveguide grating [5].

4.6 Adaptive process flow

Though we managed to control the nonuniformity and reduce it below a nanometer, such results are only sustainable by using an adaptive process flow. During the fabrication process each process step is a potential source of nonuniformity, hence controlling each step is vital. For photonics device fabrication the tolerances are

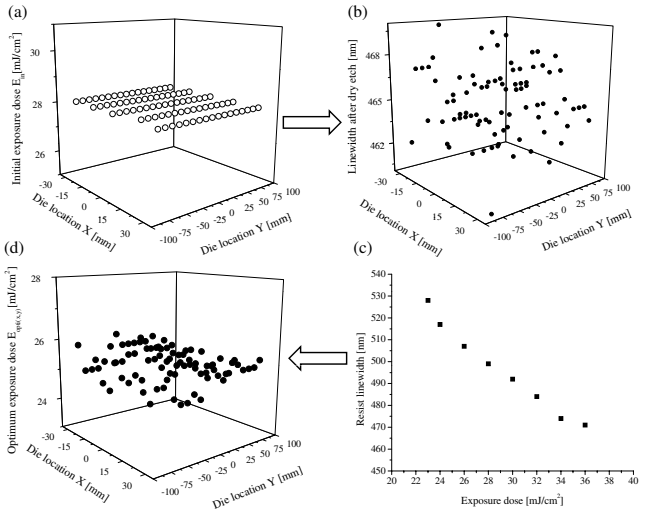


Figure 4.24: Exposure dose compensation for dry etch nonuniformity.

tighter (<1%) than for CMOS (<5-10%), and therefore the monitoring process has to be adapted to these more stringent device specifications.

Figure 4.24 illustrates a simple uniformity control through exposure dose optimization during the optical lithography process. Figure 4.24b shows the die-to-die linewidth variation after dry etch when fabricated with a uniform exposure dose as shown in figure 4.24a. The etch non-uniformity can be controlled by tuning the exposure dose of each die. Using the dose-to-target data (Fig. 4.24c) the exposure dose can be adjusted to compensate the dry etch non-uniformity with a dose map $E_{opti(x,y)}$ as shown in figure 4.24d.

The adaptive process control presented can be further extended to compensate for Si thickness non-uniformity over a 200 mm SOI wafer. Figure 4.25 shows the proposed fabrication flow. Since the lithography process is a die-per-die process, it could be adapted "on-the-fly". The dashed line in Figure 4.25 shows the flow of process monitor data, which can be used during device fabrication to tune the process for maximal uniformity. The first step in the fabrication process should be mapping the Si thickness and its variation over the incoming wafers. From the obtained data and based on input from the designer, the linewidth optimised to match the required device response can be determined for each location on the wafer. From this data and the linewidth dose-to-target graph (Fig. 4.24c) we can then determine the initial exposure dose ($E_{in(x,y)}$). The latter can then be exported to the lithography process while keeping all other settings (defocus, numerical aperture etc) unchanged.

First a send-ahead wafer is exposed with an exposure dose matrix and ($E_{in(x,y)}$) is tuned to the optimum dose ($E_{opti(x,y)}$) if needed. As described earlier, the dry

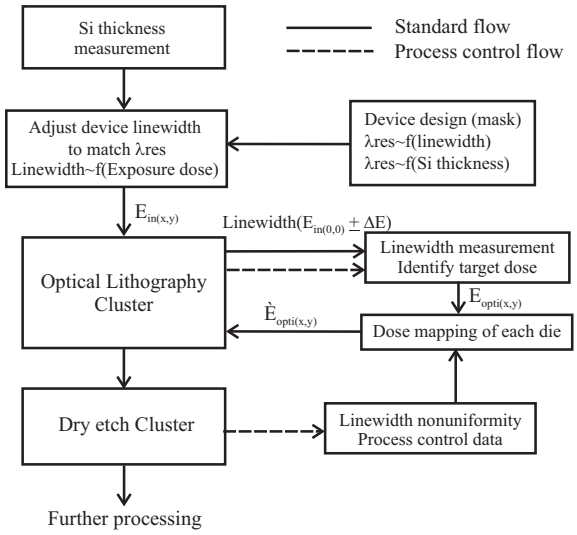


Figure 4.25: Proposed process flow model to improve device uniformity in a production environment.

etch nonuniformity can be controlled by further tuning the optimized exposure dose for each die($\grave{E}_{opti(x,y)}$).

4.7 Conclusion

In this chapter, the uniformity of the fabrication process and devices was explored. The fabrication process that was presented in chapter 3 was characterized for uniformity over a 200 mm wafer. We demonstrate good linewidth uniformity after optical lithography and dry etching. We achieved a uniformity of <1 % after each process step. The achieved process uniformity was tested with wavelength selective devices. Intra-die and inter-die measurements showed a standard deviation of <1 nm of the resonance peak, while over 200 mm wafer it was 1.5 nm. The effect of distance and density of the neighbouring devices on the absolute dimension and uniformity was also studied by using appropriate test circuits. We have found that devices as close as 10 μm can influence each other's absolute dimensions. However, the uniformity of the photonic devices on the density was not conclusive. The test structures used in the study captures both thickness and linewidth variation collectively. However, by using devices, which are sensitive to only one of the variations, the source of non-uniformities can be discriminated qualitatively.

In addition to the non-uniformity study, we propose an adaptive process control for correcting systematic non-uniformity, such as the dry etch process through

optical lithography. Further more, a data flow scheme between the device designer and the fabrication is also presented, which can be used for designing fabrication tolerant silicon photonic devices.

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5

Fabrication technology for advanced photonic device integration

5.1 Introduction

In general, wafer based device technology limits device geometry, and layer stacks over the complete wafer. Also silicon-on-insulator based silicon nano-photonic devices face a similar challenge. Even though standardization of layer stacks and thickness can bring unification in research efforts towards commercialisation of the technology, it limits freedom to explore different device geometries. In order to fabricate novel devices with high performance and functionality, a flexible layer stack is desirable. For instance, a tunable local thickness variation of the waveguide along the propagation direction can be interesting for many applications, such as for dispersion engineering, polarization rotation and splitters [1–3].

Deposited silicon, such as amorphous or polycrystalline Si can be used to overcome the limitation mentioned above. However, there are also limitations regarding these deposited materials. Firstly, amorphous Si cannot be doped and processed at high temperatures and the high propagation loss of polycrystalline Si makes it a less attractive option for photonic devices. Hence a combination of crystalline Si and either of the deposited or epitaxial Si could be an ideal option for building advanced devices.

A grating fiber-chip coupler is a prime example of a device where the conventional SOI wafer stack limits the efficiency. To overcome this problem G. Roelkens et al proposed a grating fiber coupler with silicon overlay to achieve an efficiency of 80 $\%$ between a single mode optical fiber and a silicon nano-photonic circuit [4].

The proposed grating coupler requires locally thicker Si as shown in figure 5.1b. In this chapter, we explore a more flexible and CMOS compatible fabrication process for advanced photonic devices. As a technology demonstrator, we considered high efficiency fiber couplers with overlay along with the photonic wires and wavelength selective devices in conventional SOI wafer as a test device. The fabrication technology presented here can also be exploited for other devices, such as polarization rotators [1].

5.2 Design of high efficiency fiber coupler

The efficiency of the grating couplers depends on the directionality of the diffracted power and the mode matching between the grating and the optical fiber. In a conventional grating couplers [5], an equivalent amount of power is scattered out-of-plane upwards to the optical fiber and downwards to the substrate. In order to increase the efficiency most of the light should be directed towards the optical fiber, which requires directional diffraction. The directionality can be achieved in two ways, either using an additional reflector at the bottom of the grating couplers [6–8] or by making the grating coupler intrinsically directional [4]. By modelling the Si thickness and grating design it was found that a thickness of 380 nm yields a coupling efficiency of $\approx$80 $\%$ between a single mode optical fiber and a photonic wire (500$\times$220 nm). The designed grating has a period of 520 nm with 35 $\%$ fill-factor and an etch depth of 220 nm. For a 220 nm thick waveguide, the optimum fiber coupler width is 15 μm, while the length was $\approx$20 μm. Figure 5.1 shows a schematic of a standard and high efficiency fiber coupler. Since the fiber couplers require an additional layer of Si, it is referred to as the raised fiber coupler (RFC). For more details on the design procedures we refer to [9]. The high efficiency fiber couplers were designed by Ir. D.Vermeulen.

5.3 Fabrication of high efficiency fiber couplers

The proposed high efficiency RFC can be fabricated in three different ways. Figure 5.2 illustrates the fabrication process routes through which RFC can be realized. All the process routes start with a 200 mm SOI wafer with 220 nm of Si on top of a 2000 nm BOx. In route-A and -B, the overlay islands are added through selective epitaxial growth and a deposition process respectively. On the other hand, in route-C a blanket layer of overlay is deposited all-over the wafer followed by patterning of islands containing the RFC grating, while the unwanted overlay is removed elsewhere. These three fabrication routes have both advantages and disadvantages, they might be appropriate for certain type of devices and not for others. In the following section, the fabrication routes and their suitability for fabricating high efficiency raised fiber couplers is discussed.

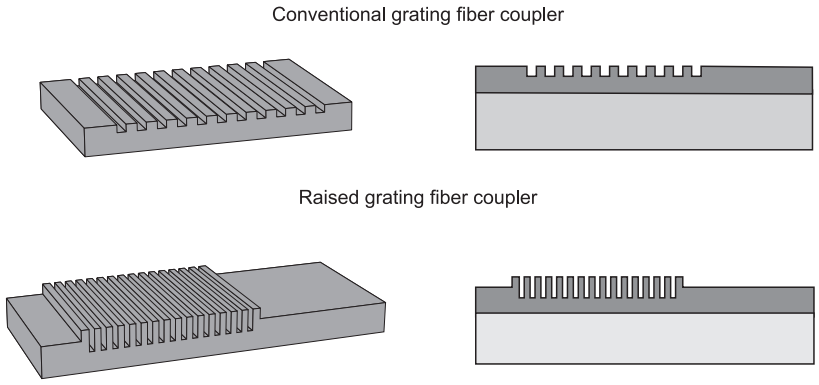


Figure 5.1: Schematic of a standard fiber-chip coupler in a conventional SOI wafer stack and raised fiber coupler with an overlay for highly efficient fiber-chip coupling.

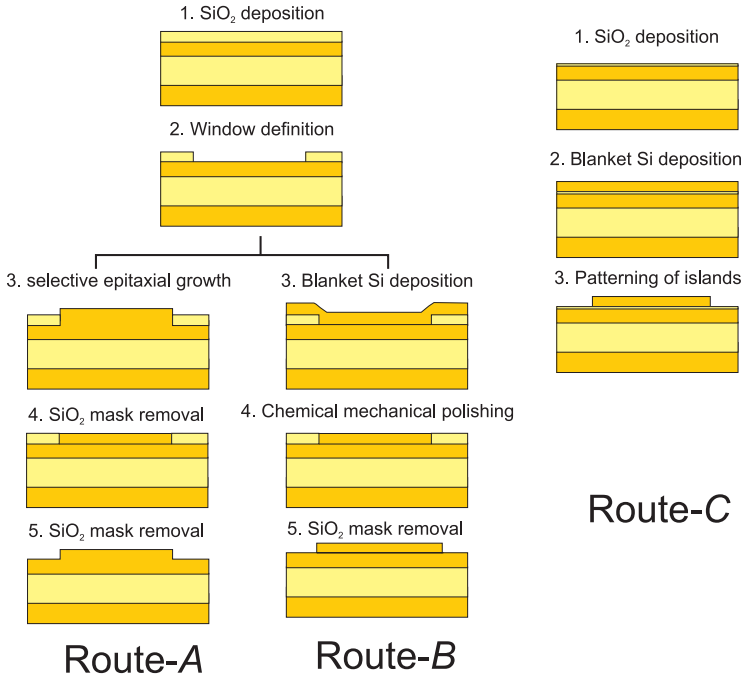
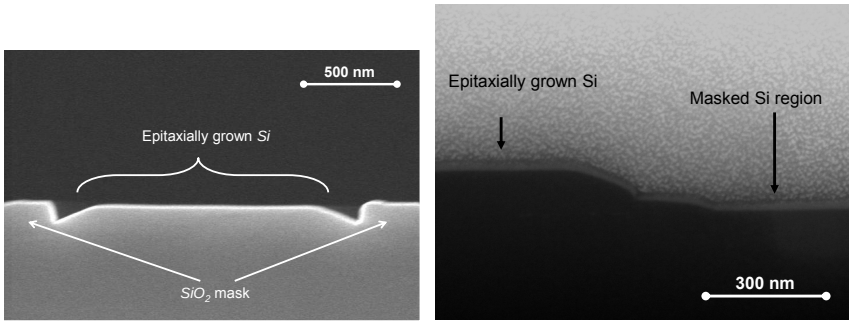


Figure 5.2: Possible fabrication route to locally add features to a convential SOI wafer.



(a) (b)

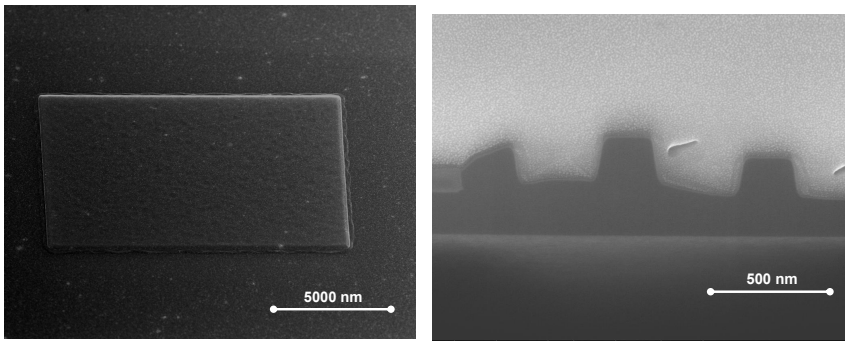
Figure 5.3: (b)Selective epitaxial Si growth in an oxide window showing preferential growing in <100> plane and (b) cross-section of a Si island formed inside the oxide window.

Fabrication Route-A

Firstly, let us discuss route-A where overlay islands are grown using selective Si epitaxy using chemical vapour depositon at high temperatures ($>800^oC$) (Fig. 5.2). In order to selectively grow Si the rest of the wafer surface is covered with SiO_2 and island of windows are opened exposing the underlying Si surface. The thickness and the profile of the grown Si can be controlled by the height of the SiO_2 layer defining the window. In practice, the height of the window is chosen slightly higher than the required thickness of Si. Figure 5.3 shows the selectively grown Si in a SiO_2 window. Due to a higher growth rate along the $<100>$ plane ($\perp$ to the wafer surface), the $<111>$ plane, appears as a wedge on the edges of the window. This can be resolved by over growth and subsequent chemical mechanical polishing (CMP). Figure 5.4a shows a Si island after SiO_2 mask removal and with the RFC etched into the grown Si. The variation in the grown Si thickness can be clearly seen in figure 5.4b. This variation could seriously degrade the efficiency. While an overgrowth and polishing can help, this limits the flexibility of device dimensions due to dishing effects in the CMP process (See next section). In [10] a similar approch was used to realize a RFC with a a moderate coupling efficiency of 50 $\%$.

Fabrication Route-B

Similar to route-A, in route-B the overlay is formed by filling a SiO_2 window with deposited amorphous silicon ($\alpha - Si$) (Fig. 5.2). Since deposition is not a selective process, the deposited $\alpha - Si$ covers the whole wafer surface. And by using a CMP process it is then removed from unwanted regions. This technique of filling and planarization is also called as damascene process, which is used in CMOS fabrication for via and metal line fabrication. In this approach, CMP is the most



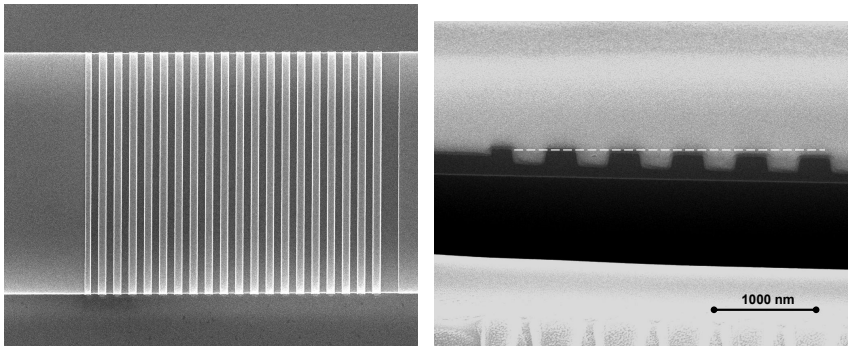
(a) (b)

Figure 5.4: (a) Island of crystalline Si grown selectively on Si surface and (b) Effect of thicknes non-uniformity in grown Si on RFC pattern.

critical step and a careful control of the polishing selectively between Si and SiO_2 is required. We used a two step CMP process: first, a non-selective CMP and then a selective polish is applied. In order to achieve an overlay thickness of 160 nm, 350 nm of amorphous Si was deposited into a 160 nm deep SiO_2 window trench. Twice the required thickness of Si was deposited in order to reduce the topography generated by the window. First, a non-selective polish is applied to remove the topography followed by a SiO_2 selective polish, which acts as an end-point for the polish process. Figure 5.5 shows a RFC fabricated using this process. Closer observation shows dishing at the centre of the overlay due to the CMP process. Even though the process was carefully designed, a thickness variation of ≈40 nm was observed as a consequence of dishing. This is due to an unfavourable size of the RFC windows (15×20 μm), which does not suit the CMP design rules. Further optimisation of the CMP process reduced the dishing to 10 nm, however, resulting in large non-uniformity over the wafer. Hence a compromise has to be found between the target and the uniformity. For devices, such as photonic wires (≈450 nm) this approach can be used with less complexity. It has been demonstrated that such a process can be used for fabricating low-loss photonic wires [11].

Fabrication Route-C

Unlike route-A and -B, a subtraction patterning approach is used in route-C (Fig. 5.2). The process starts with a crystalline SOI wafer with 220 nm of crystalline Si ($C-Si$) on top of a 2000 nm of BOx layer. Figure 5.6 and 5.7 illustrates the deposition steps to form the substrate and RFC fabrication respectively. In order to achieve a total Si thickness of 380 nm (Fig. 5.2), we deposited 160 nm of $\alpha - Si$ using a low pressure chemical vapour deposition process on top of a thin 5 nm thermally grown SiO_2 layer. This SiO_2 will act as a protective layer for the underlying $C - Si$. On top of $\alpha - Si$, 10 nm of SiO_2 and 70 nm of SiN were



(a) (b)

Figure 5.5: (a) Top-down image of the RFC fabricated in $\alpha - Si$ overlay (b) cross-section of RFC fabricated using route-B showing dishing after CMP, dotted line showing where the overlay should have been.

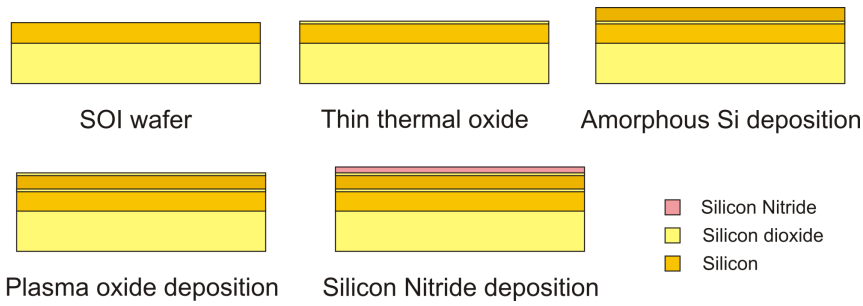


Figure 5.6: Substrate formation by layer deposition.

deposited using a plasma process. The final SiN layer will be used as a stop layer for the planarization process to obtain a flat surface for further processing, which is not presented here.

All the patterning was done using 193 nm optical lithography and dry etch process. After layer deposition, the patterning is done in the following sequence, RFC grating, RFC window/overlay removal, shallow etch grating/waveguides and finally, waveguides are defined. The details about the pattering process are presented in the following sections.

5.3.1 Raised Fiber Coupler Grating patterning

After substrate fabrication, the RFC grating is defined using 193 nm optical lithography and a dry etch process. During optical lithography the reflectivity from the substrate has to be reduced by using the appropriate thickness of anti-reflective

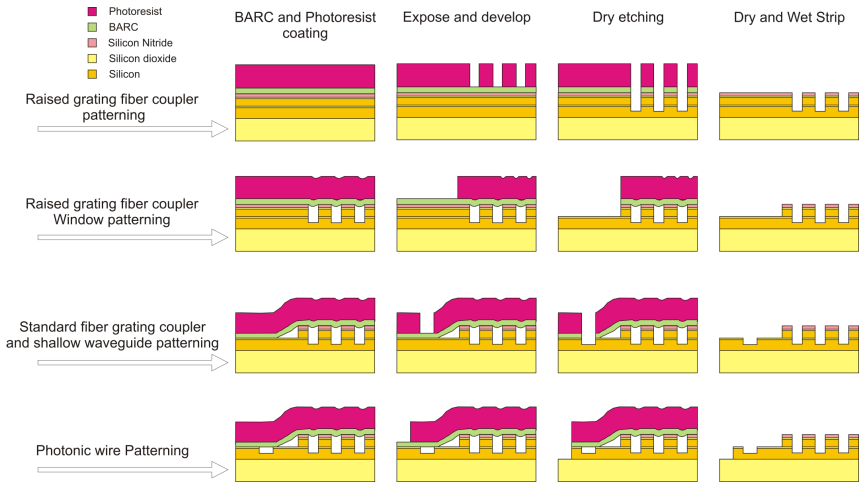
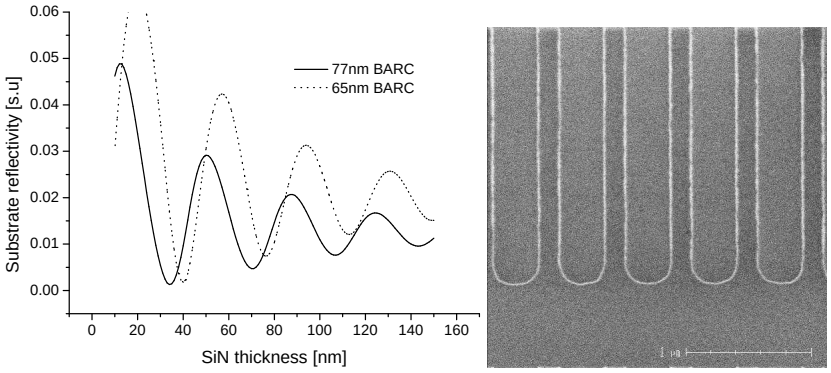


Figure 5.7: Fabircation process overview for advanced photonic integrated circuit.

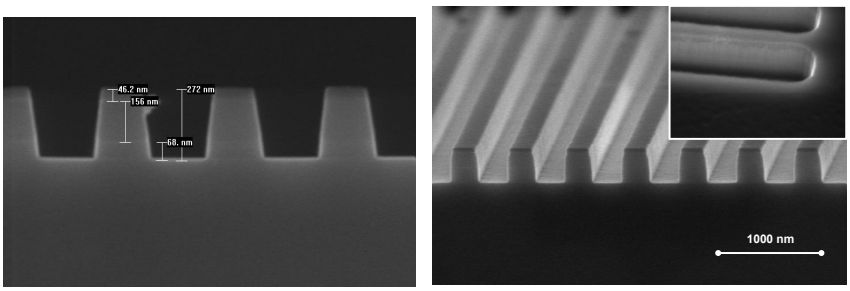
coating. As mentioned in chapter 3, the photoresist and bottom anti-reflective coating (BARC) thickness are vital for pattern fidelity and uniformity. Figure 5.8a shows the simulated substrate refection for a BARC thickness of 77 and 65 nm. For a 70 nm thick SiN, 77 nm of BARC gave the minimum reflection and hence was identified as the optimal BARC thickness. The photoresist thickness was fixed at 330 nm. The illumination was done with a conventional source with a spatial coherence (σ) of 0.5 and a numerical aperture (NA) of 0.63. For a grating pitch of 520 nm and trench width of 320 nm, we have achieved a moderate depth-of-focus of 170 nm at 4% exposure latitude. Figure 5.8c shows the top-down SEM image of a RFC in the photoresist after exposure and development.

The pattern in the photoresist is then transferred into the stack by dry etching. The grating trenches were defined by etched 315 nm deep into the substrate using selective and non-selective halogen based etch processes. The total etch depth of 315 nm includes 70 nm of SiN/10nm SiO_2/160nm $\alpha - Si$/5 nm SiO_2/70 nm Si. The etch process was done with sequence of steps for each layer. The top SiN and SiO_2 layer is first etched followed by 160 nm of overlay $\alpha - Si$ and 70 nm into $C - Si$ into the SOI wafer. Figure 5.9 shows the SEM image of one of the fabricated RFC gratings after the dry etch and photoresist strip process. The grating teeth showed a sidewall angle of $\approx 7.6^o$. This is due to the strong polymerisation on the sidewalls, which could be controlled by the etch chemistry (see chapter 4). However, the passivation helps to achieve a smooth sidewall as shown in figure 5.9b(inset).



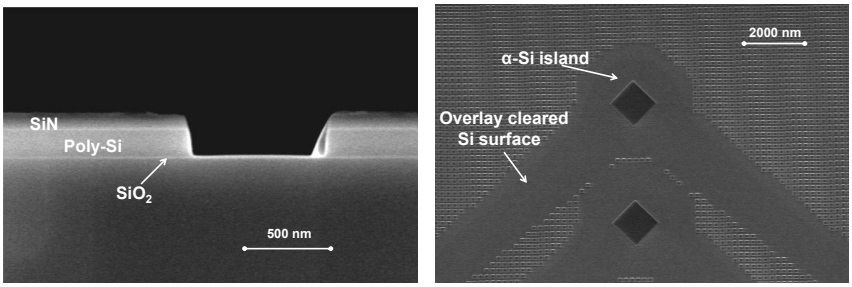
(a) (b)

Figure 5.8: (a)Substrate reflection as a function of BARC thickness and (c) Raised fiber coupler grating pattern in the photoresist.



(a) (b)

Figure 5.9: Raised fiber coupler grating pattern after dry etch (a) cross-section (b) perspective view and sidewall roughness.



(a) (b)

Figure 5.10: Fiber coupler window pattern after dry etch (a) cross-section showing highly selective overlay etch process stopping on thin oxide layer (b) image showing cleared overlay region for waveguide pattern.

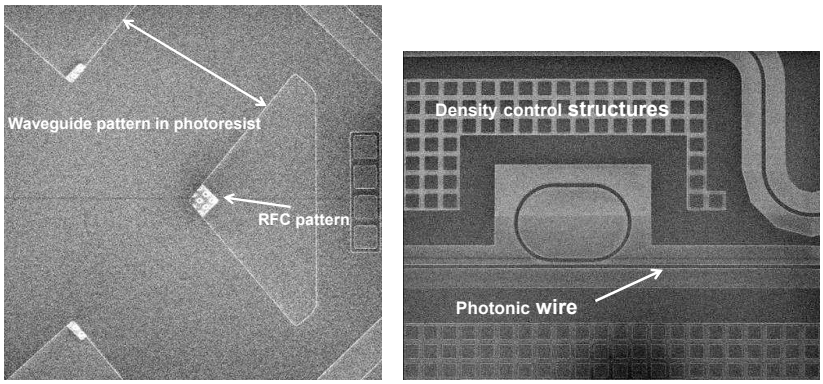
5.3.2 Fiber Coupler Window Patterning

Following the RFC grating patterning, the overlay of $\alpha - Si$ is removed from the regions other than RFC gratings by using dry etching (Fig. 5.7). Removal of the un-wanted overlay $\alpha - Si$ is one of the most critical steps in the process flow. Since all the photonic devices will be processed in the SOI wafer underneath, the top surface should be protected from dry etch damage. A 5 nm thin SiO_2 layer is used as an etch stop layer between the overlay $\alpha - Si$ and $C - Si$. During dry etch the overlay in the RFC grating is protected with photoresist islands on top of the grating structure. After defining the islands, the overlay $\alpha - Si$ is dry etched from the unprotected regions. The etch process was designed to selectively etch the overlay and stop on the thin SiO_2 layer. Figure 5.10a shows the selective etch stop on a 5 nm oxide layer. Figure 5.10b shows the top-down image of the area cleared for the photonic circuit patterning on the $C - Si$.

5.3.3 Shallow Etch Patterning

After exposing the underlying $C - Si$, the photonic circuits can be defined in it. Since the circuits will be fabricated on a wafer with a topography of ≈240 nm a sufficient depth-of-focus and exposure latitude is required. Grating fiber couplers with a period of 630 nm and a 50 $\%$ fill-factor are taken as the target device. In the same layer shallow etched devices, such as waveguide crossings and multi-mode interference splitters can also be defined. The photoresist thickness and BARC thickness was fixed at 330 and 77 nm respectively. Using a NA and σ of 0.63 and 0.85 respectively, we have achieved a depth-of-focus of 250 nm at 4$\%$ exposure latitude for a dimensional tolerance of ± 1 $\%$ (Chapter 4).

The pattern in the photoresist is transferred by etching 70 nm deep into the $C - Si$. The etch process that was defined in chapter 3 is also used here. Since a 5 nm SiO_2 was still present, the etch duration was increased to achieve 70 nm etch



(a) (b)

Figure 5.11: Waveguide pattern in photoresist after optical lithography (a) on top of RFC region and (b) in the $\alpha - Si$ overlayer cleared region.

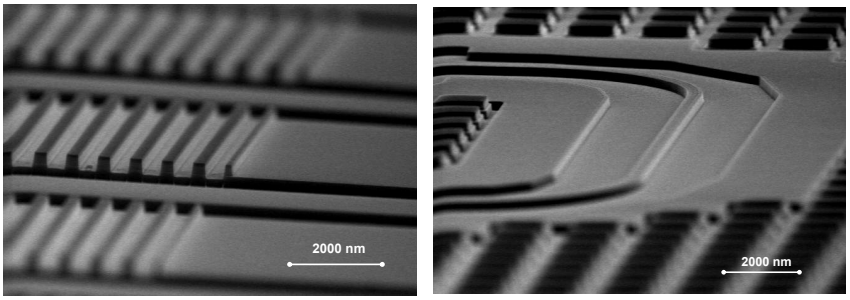
depth in $C - Si$. It should be noted that the etch process is non-selective between Si and SiO_2, hence any thickness non-uniformity of the SiO_2 will affect the etch depth in $C - Si$. After dry etching, the remaining photoresist is cleaned using a plasma and wet chemical process. The cleaned wafers are then transferred for waveguide patterning.

5.3.4 Waveguide Patterning

Waveguide definition is the last patterning process in the fabrication flow. All the devices such as resonators, arrayed waveguide gratings and planar waveguide gratings which require 220 nm of etch depth into $C-Si$ are defined in this layer. In addition to uniformity, the propagation loss in the waveguide is considered as the most important specification for this layer. In order to achieve low-loss photonic wires, the etch process should be able to deliver low sidewall roughness.

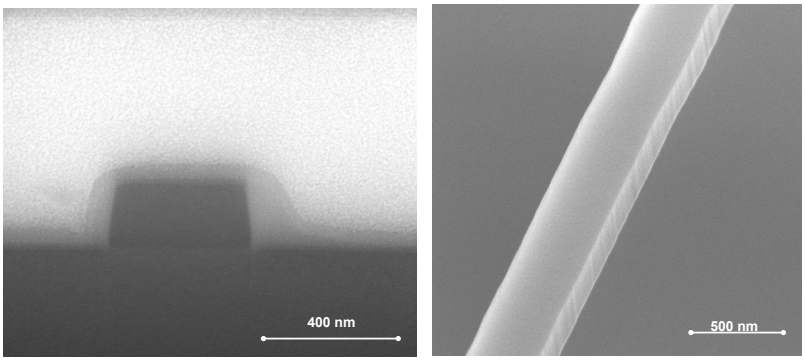
The waveguide patterns were defined in a 330 nm photoresist using 193nm optical lithography. The lithography process was designed to achieve a tolerance of ± 1 % for a 450 nm photonic wire with a depth-of-focus of 200 nm at an exposure latitude of 5.4 %. Figure 5.11 shows the waveguide pattern in the photoresist after lithography. The photonic wires were defined where the $a - Si$ has been removed (Fig. 5.10) as shown in figure 5.11b, which also shows the density control structures. After lithography the wafers are then transferred for dry etching.

For etching the 220 nm deep $C - Si$ we used the process descriped in chapter 3. Figure 5.12 shows the waveguide pattern along with the RFC grating structure in the overlay $\alpha - Si$. Figure 5.13 shows the cross-section of a photonic wire and the sidewall, which shows a very smooth surface. After dry etching the wafers were cleaned to remove the remaining photoresist followed by a short dip in the buffered hydrofluoric acid to remove the thin thermal oxide layer on top of the



(a) (b)

Figure 5.12: (a) Raised fiber coupler pattern with $\alpha - Si$ overlay and (b) photonic wire waveguide in $C - Si$.



(a) (b)

Figure 5.13: (a) Cross-section of a photonic wire and (b) smooth sidewall.

waveguides.

5.4 Optical characterization

The fabricated devices were optically characterized by transmission measurements. All the characterization was carried out using a vertical fiber coupler setup as described in chapter 3.

5.4.1 Raised Fiber Coupler Efficiency

The efficiency measurement structure was implemented by using two identical fiber couplers at the input and output connected by a wide photonic wire (15 μm). The length of the waveguide was kept short to avoid the influence of propaga-

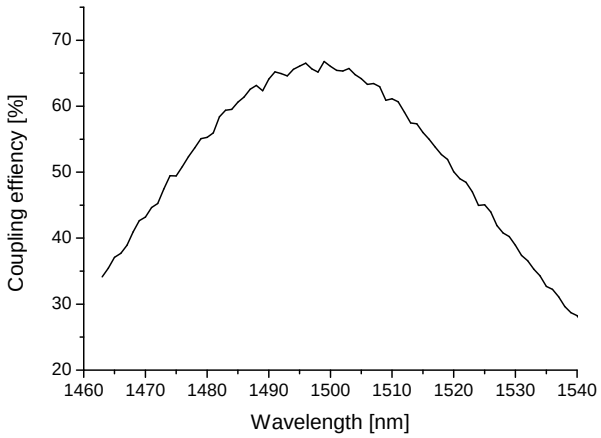


Figure 5.14: Light coupling efficiency of a raised fiber coupler and photonic wire a fiber incident angle of 13°.[courtesy D. Vermeulen]

tion loss on the fiber coupler efficiency. By normalizing the transmission through the fiber coupler with loss in the measurement setup, we have found a coupling efficiency of 70 $\%$ per coupler with a 3dB bandwidth of 80 nm. The achieved efficiency is the highest reported thus far for a fiber-chip coupler fabricated using CMOS front-end fabrication process.

5.4.2 Photonic wire Propagation Loss

The propagation loss of the photonic wire was measured by using the cut-back method. We used photonic wire lengths varying between 0.5 to 15 cm, which are spiraled with a bend radius of 20 μm. Since the chosen bend radius was large the influence of the bend loss on the straight propagation loss is negligible. The light was coupled in and out the photonic wires using a shallow etch grating coupler in $C - Si$ [5].

Figure 5.15 shows the propagation loss spectrum and the inset shows the propagation loss at 1550 nm. For a 500 nm wide photonic wire waveguide we have measured a propagation loss of 1.77$\pm$0.05 dB/cm. There are two possible reasons for this improvement. Firstly, smooth sidewalls which reduces scattering loss and secondly, reduction in the surface absorption by thin oxide layer and wet chemical process [12].

5.4.3 Wavelength Selective Devices

In addition to photonic wires, we have implemented a mach-zehnder interferometer (MZI) as a wavelength selective test device. It was implemented by using two Y-splitters and a delay length of 50 μm was introduced in one of the arms. Figure 5.16 shows the transmission spectrum of one of the fabricated MZI. We obtained

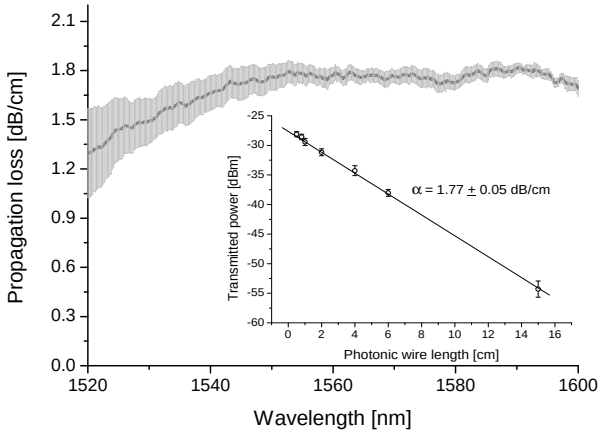


Figure 5.15: Propagation loss of a photonic wire of 500 nm wide and 220 nm high and inset showing linear regression of transmitted power at 1550 nm.

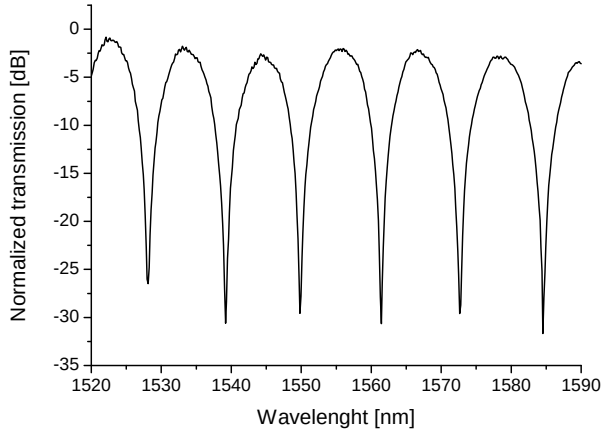


Figure 5.16: Normalized transmission spectrum of a mach-zehnder. interferometer.

an average free spectral range of 10 nm. From the spectral response, we extracted an average group index (n_g) of 4.8. The device characteristics clearly demonstrate the technology viability for fabrication of any type of wavelength selective device with the fabrication technology presented in this chapter.

5.5 Conclusion

In this chapter, an advanced fabrication process for flexible device geometries has been outlined. High efficiency fiber-chip couplers with overlay were studied. Three possible fabrication routes has been proposed and investigated for their

suitability. Selective epitaxial growth and damascene process were found to be unsuitable for this application while layer deposition and etching was found to be the most reliable way for fabricating photonic devices with a flexible cross-section geometry, such as the raised grating fiber-chip coupler. Using such a fabrication process, low-loss photonic wires, wavelength selective devices and high efficiency fiber-chip light couplers have been demonstrated.

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6

Deposited silicon for Photonic integrated circuits

6.1 Introduction

Silicon photonics usually means photonic devices fabricated in crystalline silicon-on-insulator (SOI) material technology. The superior material quality, transparency and high refractive index contrast (Δn=2, Si/SiO_2) make crystalline silicon an attractive platform for compact integrated circuits. Silicon alloys (SiN and $SiON$) have been developed as an alternative to low index contrast planar lightwave circuits with a moderate refractive index contrast (0.55-0.8). The development of compact components in silicon, such as photonic wires, ring resonators and arrayed waveguide gratings inspired integration with microelectronics. Advancement in silicon photonics as a matured technology can be exploited for many applications, one such application is electronic-photonic integration. Both fields can benefit through this integration, for instance, a low cost optical communication technology and high-speed integrated circuits [1]. In order to overcome the communication bottleneck in high-performance integrated circuits, optical lines may help. Three possible electronic-photonic integration schemes have been proposed in the past years: front-end: photonic circuit at the transistor level, back-end: photonic circuit on top of the metal levels and 3D-integration: photonic circuit on top of electronic chip or otherwise. Unlike front-end and 3D integration schemes, back-end integration requires a deposited waveguide material. Ideally this material has low-loss and high index contrast and should be possible to deposit at low temperatures. In addition to integration, this technology can serve as an alternative

to crystalline silicon.

In recent years various functionalities have been demonstrated using deposited silicon. The two main material variations studied are amorphous and polycrystalline silicon. With these, functionalities such as an electro-optic modulator [2, 3] , all-optical modulators [4], high speed nonlinear effects [5], multilayer photonic circuits [6], and wavelength selective devices [7] have been demonstrated. The choice of material depends on the thermal budget of the fabrication process. Amorphous silicon is deposited at low temperatures ($<450^{o}$C), which is suitable for back-end and other low temperature integration schemes. However, amorphous silicon cannot withstand high temperature. In those cases polycrystalline silicon can be the material of choice. Apart from the passive functions, such as waveguides and wavelength selective devices, deposited polycrystalline silicon would be particularly interesting for high speed modulators due to the relatively short carrier life time [3].

In this chapter, we explore three types of deposited material; silicon dioxide as a cladding material, and amorphous and polycrystalline silicon as waveguide material for photonic integrated circuits. The deposition process, material properties and optical transparency of all the materials are presented.

6.2 Silicon dioxide

Silicon dioxide (SiO_2) is one of the most commonly used materials in a wide range of applications both in daily life and in electronics. The excellent electrical insulating properties of SiO_2 made planar processing possible in electronic circuit manufacturing. Since SiO_2 is transparent for a wide range of optical wavelengths, it is also widely used as waveguide and cladding material in integrated photonic circuits. Low index contrast planar lightwave circuits are formed by doping SiO_2 channel waveguides [8]. In high index contrast material technologies, such as silicon nitride (SiN) and silicon (Si), SiO_2 is the most commonly used cladding material, since it provides good environmental protection without reducing the index contrast significantly.

Even though SiO_2 is transparent for a wide wavelength range, telecom wavelength bands are the most interesting for silicon integrated circuits. SiO_2 can be desposited in a variety of ways and, the optical and material properties depend on the deposition technique and process conditions. Hence, in this section, SiO_2 films deposited using different techniques and their properties are studied.

6.2.1 Deposition techniques

Chemical vapour deposition (CVD) is the most commonly used technique for SiO_2 deposition. Thermal CVD, Plasma CVD and high density plasma CVD are the three widely used CVD methods. Different techniques yield different process and material quality. The two primary precursors used for SiO_2 deposition are silane (SiH_4) and tetra-ethyl-otho-silicate (TEOS) with N_2O, oxygen or ozone.

Deposition method	Precursor Gas	Process temperature
Low pressure chemical vapour deposition (LPCVD)	TEOS/O_2	670^{o}C
Plasma ehanhanced chemical vapour deposition (PECVD)	SiH_4/N_2O	400^{o}C
High density plasma - chemical vapour depsition (HDP)	$SiH_4/O_2/Ar$	400^{o}C

Table 6.1: Different SiO_2 deposition methods.

The primary goal of the deposition process is to oxidize the precursor gas and to form a solid reaction product (SiO_2) on the wafer surface.

In this work, we explored SiO_2 deposited using three types of CVD process: Low pressure CVD (LPCVD), plasma enhanced CVD (PECVD) and high density plasma CVD (HDP).

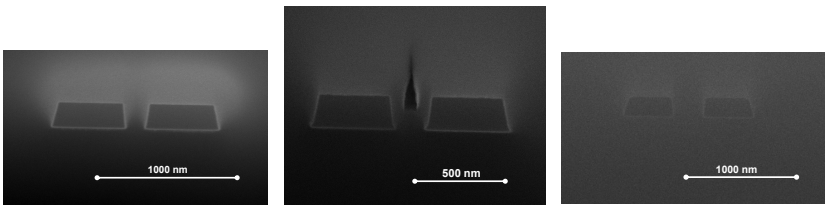
6.2.2 Design of experiment

Our experiment was limited to three types of SiO_2 deposited with the methods mentioned in the previous section. Table 6.1 illustrates different deposition methods and gases used in our experiment. Two types of wafers were deposited with SiO_2: one with circuit patterns in SOI wafer and the other is a flat unpatterned blanket on a silicon wafer. The blanket layer was used to characterize the material composition through fourier transform infrared spectroscopy and for surface roughness characterisation using an atomic force microscope (AFM). Filling and optical absorption were characterized on the patterned wafers using cross-section scanning electron microscope (XSEM) and optical transmission measurements, respectively.

6.2.3 Material characterization

6.2.3.1 Conformality and Filling

Conformality can be defined as retention of the topography when deposited over a patterned surface. Conformal deposition is important while filling a structure with high aspect ratio, such as narrow slots and photonic crystal holes. Figure 6.1 shows the gap filling capability of different deposition processes. It is well known that the LPCVD process can yield conformal deposition, since the deposition species can diffuse readily into trenches and holes. Figure 6.1a shows complete filling of a directional coupler by using a LPCVD process. On the other hand, a PECVD process has created a key-hole in the coupler gap (Fig.6.1b). This is a typical characteristic of a plasma process, which has less conformality. The wide acceptance angle at the top corner of the trench and high sticking coefficient of the deposited species enables higher growth rate resulting in bridging and the formation of a key-hole void in the trench. This filling is unacceptable for photonic devices as they



(a) LPCVD oxide (b) Plasma oxide (c) High density plasma oxide

Figure 6.1: (Cross-section scanning electron micrograph of a directional coupler filled with SiO_2.

will create undesirable device performance, such as scattering and non-optimal coupling.

The issue of conformal deposition in a plasma process is resolved by using a HDP process, where a cycle of deposition and sputtering etching action ensure better film coverage. The deposition process is executed as a combination of deposition and etching. The enhanced deposition at the top corner is abated by sputter etching. Figure 6.1c shows a result of such a process. By controlling the deposition and sputtering process, structures with different aspect ratios can be filled. Even though HDP process has an excellent gap filling property, it creates triangular topography of SiO_2 on top of the patterns [9], which can be removed by a chemical mechanical polishing process (see section 6.2.3.3).

6.2.3.2 Material Composition

The material composition of the deposited material strongly depends on the precursor, deposition technique and process conditions. Fourier Transform InfraRed (FTIR) spectroscopy is one of the simple ways to identify the constituents in a thin film. Table 6.2 shows the different vibration modes in SiO_2. Figure 6.2 shows the FTIR spectrum of LPCVD-TEOS, PECVD and HDP SiO_2. The dominant vibration modes of $Si-O$ are clearly visible at 460, 1085 and 1140 cm^{-1} from all the oxides. However, closer examination of the difference spectra[1] shows clear differences between them (Fig. 6.3). They indicate the presence of $-OH$ mode in LPCVD-TEOS, while no traces were observed in HDP and PECVD oxides (Fig. 6.3a). The presence of $-OH$ would result in absorption loss (section 6.2.3.4. There are two reasons for the presence of $-OH$ in the film, firstly, incorporation of H during deposition process and secondly, moisture absorption due to a low material density. In either case, it can be removed by annealing at a high temperature. Despite annealing at 850^{o}C the $-OH$ was still present with lower intensity (Fig. 6.3b). This suggest that $-OH$ is incorporated as a consequence of moisture absorption and not during deposition.

[1]Difference spectra is nothing but the derivative of the FTIR absorption spectra. It helps to bring out small peaks and variations.

Bond configuration	Peak frequencies (cm^{-1})	ref
$Si-O$ rocking	460-70	[10]
$Si-O$ bending	820	[11]
$Si-O-Si$ stretching	1085	[12, 13]
$Si-O$ asymmetric stretching	1140	[12, 13]
$Si-Si$ oxygen vacancies	612	[10]
$Si-OH$	3674	[14]
$H-OH$	3300, 1630	[14] [15]
$Si-H$ stretching	2000	[16]
$Si-H_2$ asymmetric stretching	2090	[16]
$Si-H_3$ symmetric stretching	2090	[16]

Table 6.2: Infrared absorption of various $Si-O$ and $Si-OH$ vibration modes.

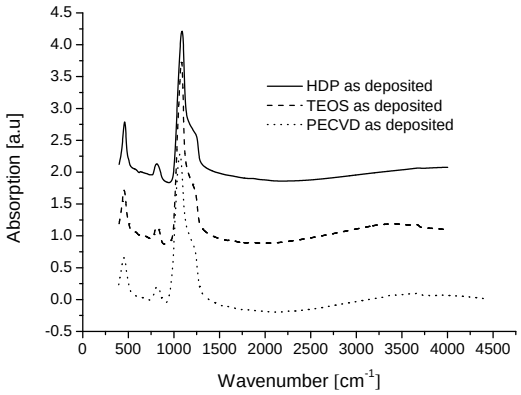


Figure 6.2: FTIR spectrum of desposited silicon dioxide showing $Si-O$ modes at 460, 1085 and 1140 cm^{-1}.

The presence of $-OH$ in the film can result in absorption of light in the telecom wavelength band (1550 nm), which is confirmed by optical measurements in section 6.2.3.4. Hence, while selecting the type of oxide for cladding, the presence of $-OH$ should be kept in check. From FTIR characterization, HDP and PECVD oxide qualifies as a suitable cladding layer.

6.2.3.3 Surface roughness and planarization

A smooth surface is crucial for building a high performance deposited silicon-on-insulator technology. Roughness present in the oxide layer can propagate through layers deposited on top of it resulting in scattering loss. Figure 6.4 shows the surface roughness on a HDP oxide surface before and after chemical mechanical polishing (CMP). After polishing the surface roughness(rms) was reduced from 0.7 nm to 0.12 nm. In the figure 6.4 after polished image shows stripes which,

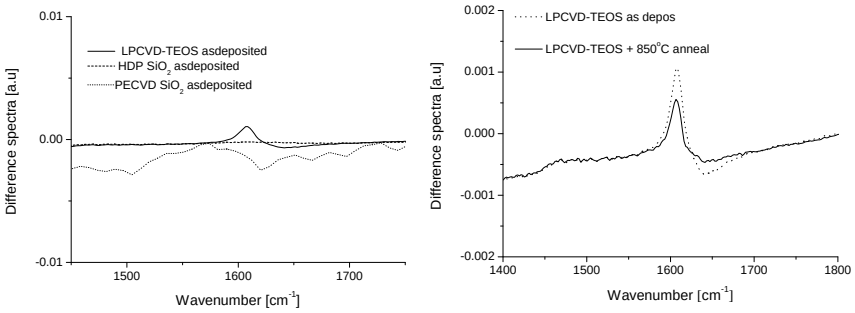


Figure 6.3: (a)FTIR difference spectrum showing $-OH$ peak at ≈1600 cm^{-1} and (b) Thermal annealing of LPCVD-TEOS reduces $-OH$ intensity.

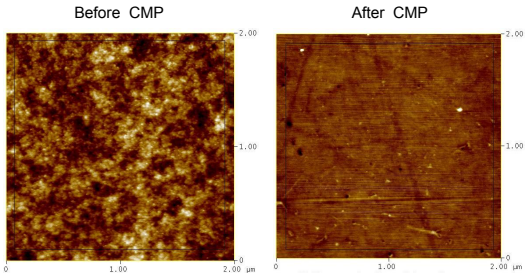
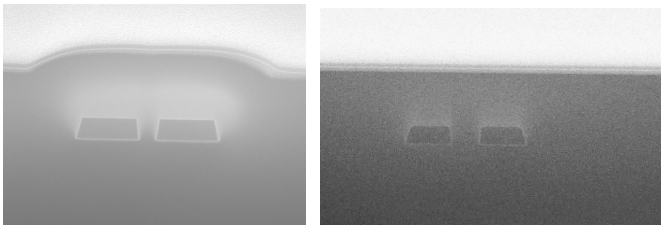


Figure 6.4: Surface roughness of HDP silicon dioxide before and after chemical mechanical polishing.

can be either due to sample handling damage or CMP damage, which measured a maximum height of 5 nm. Irrespective of the deposition method and technique, surface roughness can be reduced to atomic layer smoothness with the help of an appropriate CMP process.

In addition to smoothening, CMP can be used to planarize topographies generated after oxide filling. Figure 6.5 shows the effect of planarizing CMP on a surface with a topography. Planarization becomes more important for multilayer photonic circuits, where a flat wafer surface is required for building functional photonic devices and circuits.

Both smoothening and planarization are achieved by removing material from the wafer surface. Hence, during the deposition process the thickness loss should be compensated for by additional deposition.



(a) Before CMP (b) After CMP

Figure 6.5: Planarization of topography created after cladding deposition.

6.2.3.4 Optical absorption

Absorption of light is the most important material metric for photonic applications. Absorption in the cladding is assessed by comparing the propagation loss of a photonic wire fabricated in crystalline Si with and without cladding layer. After fabricating the wires, some of the wafers were covered with LPCVD-TEOS, HDP and PECVD oxides. Wafers deposited with LPCVD-TEOS were annealed at 850^{o}C in order to reduce the $-OH$ content in the film.

The propagation loss difference was measured by using a cut-back method for photonic wires with and without oxide cladding. Photonic wires cladded with LPCVD-TEOS yielded a 1.7 dB/cm higher loss, which can be attributed to the presence of $-OH$ bonds. HDP and PECVD oxides showed a very small change in the loss within the error margin, they measured -0.1 and 0.2 dB/cm respectively suggesting low absorption in the 1550 nm range.

6.2.4 Summary

Silicon dioxide deposited by three CVD (LPCVD, PECVD and HDP) deposition methods was investigated. SiO_2 deposited using the PECVD and HDP deposition process yield low absorption, while LPCVD-TEOS resulted in higher absorption due to $-OH$ bonds incorporated in the film. Furthermore, the high deposition and anneal temperature restricts LPCVD-TEOS to front-end integration. With low deposition temperature and lower absorption PECVD and HDP oxides can be used both in front and back-end of the line. However, the poor filling capability of PECVD oxide limits its usage to unpatterned wafer surfaces. Overall, the HDP oxide emerges as the most suitable for both bottom and top cladding materials.

6.3 Amorphous silicon

Amorphous silicon ($\alpha - Si$) is a widely used material in many thin film applications. In particular, the applications include photovoltaic cells, thin-film-transistors (TFT) and photocopiers. Amorphous silicon as waveguide material was

first demonstrated by Cocorull et al in 1996 [17]. Since then tremendous progress has been made in material and device technology. As mentioned earlier in section 6.1, low absorption is one of the primary requirements for silicon photonics. Unlike crystalline Si, where atoms are regularly arranged on a periodic lattice, amorphous Si has short range order, which results in dangling bonds, distorted bond configurations and voids. These defects are inherent in an amorphous material. However, by understanding the nature of these defects, an optimised process can deliver low defect levels and eventually low propagation loss.

Amorphous silicon can be deposited either by using chemical vapour depsoition (CVD) or physical vapour deposition (PVD). The physical processes, such as thermal evaporation or sputtering yield poor material quality. In a CVD process, a Si containing precursor gas is transformed into a solid layer by chemical reaction. The two most widely used CVD techniques are LPCVD and PECVD. Over the years, both these techniques have been explored to obtain a low-loss $\alpha - Si$ material. Various groups showed that PECVD is the most suitable technique to achieve low-loss deposited $\alpha - Si$ [7, 18–20]. The main reason is the ability to deposit layers with a low defect density. This is achieved by adding hydrogen (H) in the Si network resulting in passivation of dangling bonds [21, 22]. Hydrogenated amorphous Si ($\alpha - Si : H$) has been studied in the context of photovoltaic research, where improvements in the device performance with hydrogen incorporation were clearly observed.

6.3.1 Deposition process

$\alpha - Si : H$ thin films for photonics are commonly prepared using monosilane (SiH_4) as precursor gas with or without dilution gases such as H_2, He, Ar, and Xe. In the plasma, the precursor gas is dissociated into different reactive species, including silyl(SiH_3), silylene(SiH_2), silylidine (SiH), etc., depending on the energy state. These excited species react among themselves and with the feed gas to form a steady state condition to sustain the plasma. The addition of a dilution gas such as He ensures that the dissociated species do not react in the gas phase, which would create particles and result in a poor film morphology and quality. The film formation is influenced by the density of the dissociated species, which in turn is governed by the deposition process parameters such as, gas ratio, power, temperature, etc.

It has been shown by Matsuda et al [23, 24] that SiH_3 is one of the dominant species in the plasma and also one of the major contributors for the film growth. By adsorbing these species on the surface of the wafer a solid film can be formed from the gaseous species. Initially, the wafer surface is covered with $-H$. When the Si containing radicals arrive onto the H rich surface it reacts with H, which is then released from the surface (Eq. 6.1 and 6.2) resulting in a dangling bond ($Si-$). This dangling bond serves as a growth point for further film formation. However, not all of these dangling bonds are further used, hence leaving residual defects. Thus, it is impossible to prepare films without defects (i.e. dangling bonds). The chemical reactions involved in the growth process are very complex.

However, general reaction models can be derived for basic understanding. The reaction route described by Eq. 6.1 and Eq.6.2 is one of the possible film forming surface and gas phase reactions.

$$\equiv Si - H + SiH_3 \rightarrow \equiv Si - + SiH_4 \tag{6.1}$$

$$\equiv Si - + SiH_3 \rightarrow \equiv Si - SiH_3 \tag{6.2}$$

6.3.1.1 Role of hydrogen

Hydrogen plays a vital role in defect passivation of $\alpha - Si : H$. Due to its small radius, hydrogen can diffuse through the film relatively easily. The incorporation of H in the amorphous network has two implications; firstly, weak $Si - Si$ bonds can be broken by H resulting in an ordered network, which could reduce defect density in the film. Secondly, a large amount of hydrogen results in clustering and void formation. Hence, it is necessary to incorporate the right amount of hydrogen in the film to avoid the degrading effect of H.

Despite its passivation property, H is also responsible for the instability of $\alpha - Si : H$ films at high temperatures (>400^{o}C). Since H can be mobilized at high temperature, desorption of H from the film occurs. The loss of H creates dangling bond defect sites. At even higher temperatures (>600^{o}C) recrystallization occurs forming polycrystalline silicon, which is known to have high optical loss. This is one of the primary reasons why $\alpha - Si : H$ is restricted to the CMOS back-end (<450^{o}C).

Desorption of H can be exploited positively by controlling the H evolution and thereby modifying the material properties, such as the material density. In section 6.4, we present a method of trimming photonic devices using such a technique.

6.3.1.2 Optical absorption and scattering defects

Defects are the main cause of optical loss in deposited Si. As mentioned earlier adding hydrogen in the Si network can help to reduce the defects, but still a number of defects are still present. The two primary causes for loss are absorption and scattering. Absorption loss is primarily caused by bond configuration and dangling bond defects. These defects have characteristic energy levels and charge states. Since the energies are distributed over a broad spectrum, it is often difficult to distinctly distinguish defects in $\alpha - Si$. Hence these defects are collectively handled as absorption defects. Absorption defects generate defect states within the band gap. A linear relation of dangling bond density to the optical absorption is observed in $\alpha - Si : H$ [25]. Optical absorption occurs when a neutral defect state in the bandgap is transformed on to a charged state either by accepting an electron from the valance band or by passing an electron into the conduction band. A typical bandgap of $\alpha - Si : H$ is $\approx$1.6-1.9 eV [20] depending on the H content. A similar argument is also applicable for polycrystalline Si.

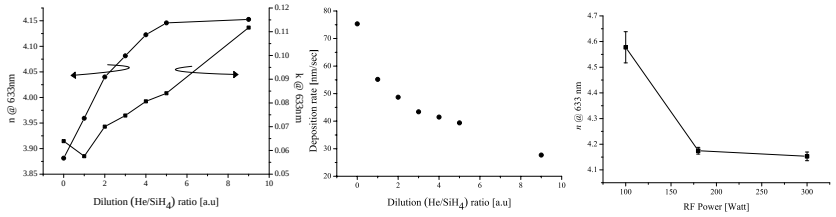
Parameter	Range	Nominal setting
RF power	100-300 Watts	180 Watts
Spacing	500 mils (12.25 mm)	500 mils
Pressure	1.5-5 Torr	2.6 Torr
Temperature	300^{o}C	300^{o}C
Silane (SiH_4) flow	100-300 sccm	100 sccm
Helium (He) flow	0-2500 sccm	900 sccm

Table 6.3: Experimental conditions for $\alpha - Si : H$ deposition.

In addition to absorption, scattering loss is also a major concern for photonics application. Scattering of light occurs when the properties of the material, mainly the density (refractive index), abruptly changes along the light propagation direction. Even though H plays a vital role in defect passivation, clusters of H result in microscopic voids. These voids are undesirable, as they represent a local change in density. These clusters have to be controlled through the deposition process. For instance, the density of higher order silyl and silylene ($(Si - H_{2,3})_n$) which is known to create voids of H clusters has to be reduced. Beside H voids, local crystallinity can also result in scattering. In polycrystalline Si, this is one of the primary causes for the loss due to crystal grains and their boundaries. In $\alpha - Si : H$, however, the effect is microscopic. These microscopic crystals created during the deposition process are not larger than 5 nm. These defects cannot be cured after deposition hence the deposition process has to be tuned in order to avoid such evolution.

6.3.2 Design of experiment

$\alpha - Si : H$ was deposited in a 200 mm industrial PECVD deposition tool manufactured by Applied materials®. The deposition chamber is a part of a deposition cluster with load-locks. The plasma source consists of two aluminium electrodes separated by a gap set to 12.25 mm. The upper electrode is connected to a radio frequency power supply operating at (13.56 MHz), while the bottom electrode is grounded. SiH_4 and helium (He) are used for film deposition. As mentioned earlier there are a number of parameters that can be tuned to control the film growth. We kept the substrate temperature and the distance between the electrodes (spacing) constant, while the feed gas ratio, pressure, and power were tuned. Table 6.3 summarizes the experimental conditions of the deposition process used in our experiments.



(a) (b) (c)

Figure 6.6: Influence of dilution of SiH_4 on (a) the refraction index($n\&k$) at 633 nm and (b) the Deposition rate of α-Si:H. (c) Influence of plasma power on the refractive index of α-Si:H

6.3.3 Material characterization

6.3.3.1 Refractive index : Spectroscopic ellipsometry

The film thickness and the refractive index of the deposited material were characterized using spectroscopic ellipsometry (SE). Figure 6.6a and Fig. 6.6b illustrate the effect of dilution of the precursor (SiH_4) on the refractive index and deposition rate of the deposited films respectively. The refractive index of the film increases with increase in the dilution, which induces an increase in film density, while the deposition rate decreases. We also observe that the refractive index decreases with increase in power (Fig. 6.6c).

The change in the film density can be related to the deposition rate and surface reaction [26]. Although the growth process itself is a complex sequence of random events on the wafer surface, a simple but realistic explanation can be given. The deposition rate increases with an increase in the radical density in the plasma. This can happen either at higher plasma powers or at lower dilution. During the growth process, the radicals from the plasma arrive on the wafer surface at a certain rate called radical arrival rate R_a, which is determined by the deposition condition. Upon arrival on the surface, these radicals diffuse to identify a reactive growth site, the distance they travel on the surface is called diffusion length and the rate at which they react is called the surface reaction rate (R_{sr}). If R_{sr} is higher than R_a, the radical gets sufficient time to find a growth centre resulting in a dense film, for instance, higher dilution of the precursor decreases R_a there by forming a film with higher density or refractive index. As mentioned earlier, we can clearly observe this in figure 6.6a. On the other hand, a higher R_{ar} would result in a less dense or low refractive index film.

6.3.3.2 Material composition : Fourier transform infrared spectroscopy

The composition of the deposited film is studied through the Fourier Transform Infrared spectroscopy (FTIR) absorbance spectrum between 400-4000 cm^{-1}. The background corrected spectrum is studied for the $Si-H$ bond configurations, as

Bond configuration	Peak frequencies (cm^{-1})	ref
$Si-H$ wagging	640	[16], [27]
$Si-H_2$ rocking	620	[16]
$Si-H_3$ symmetric bending	840	[16] [28]
$Si-H_3$ asymmetric	890	[16] [28]
$Si-H_2$ symmetric bending	890	[16] [28]
$Si-H$ stretching	2000	[16]
$Si-H_2$ asymetric stretching	2090	[16]
$Si-H_3$ symetric stretching	2090	[16]

Table 6.4: Infrared absorption of various $Si-H_n$ vibration modes.

they are an important constituent of the film. The characteristic vibration modes of different $Si-H$ bonds occur at distinct frequencies, which are summarized in Table 6.4. Although H is a vital element for preparing low-loss α-Si films higher concentrations lead to undesirable cluster formation, which can result in void formation. These clusters can be easily identified from the IR frequency peaks in the spectrum as presented in Table 6.4.

Effect of dilution

Figures 6.7a and 6.7b depict the absorbance spectra at 2000 and 640 cm^{-1} for samples with different dilution. In fig. 6.7a it can be clearly seen that the peak shifts from 2090 cm^{-1} (polyhydride) to 2000 cm^{-1} (monohydride) for higher dilution. This is a clear indication that the total amount of H incorporated in the film decreases with an increase in dilution. Further more reduction in the 640 cm^{-1} $Si-H$ peak also suggests the same (Fig.6.7b). Excessive hydrogen in the film creates voids, which is called microstructure (R). The latter is often quantified by the ratio of mono- and polyhydrides absorbance peaks [29],

$$R = \frac{\int I_{2090}}{\int I_{2000} + \int I_{2090}}. \tag{6.3}$$

Where I_{2000} and I_{2090} are the integrated intensities of the peaks at 2000 and 2090 cm^{-1} respectively. Figure 6.8 shows the microstructure R obtained from the spectrum, which clearly indicates the reduction in the voids with increasing dilution. The microstructure is an indication of the film density and can be correlated with the refractive index of the film. We indeed observe an excellent agreement between these two quantities when comparing Fig. 6.6 and 6.8.

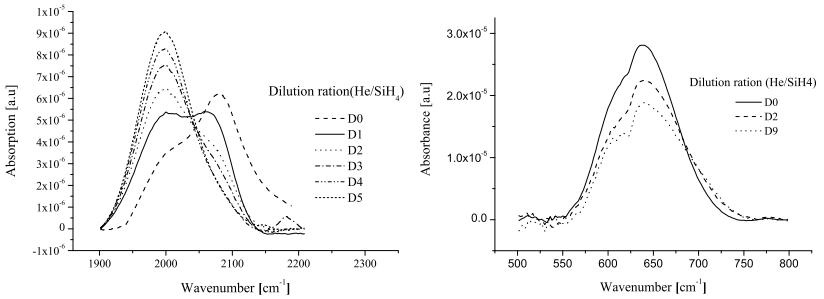


Figure 6.7: (a) Infrared absorption due to $SiH_{x=1,2,3}$ at 2000 and 2090 cm^{-1}, at different precursor dilutions. and (b)Infrared absorption due to SiH at 640 cm^{-1}, at different precursor dilutions.

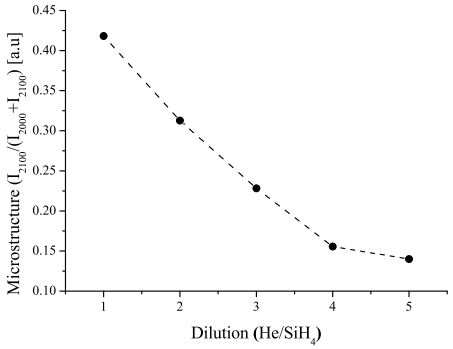
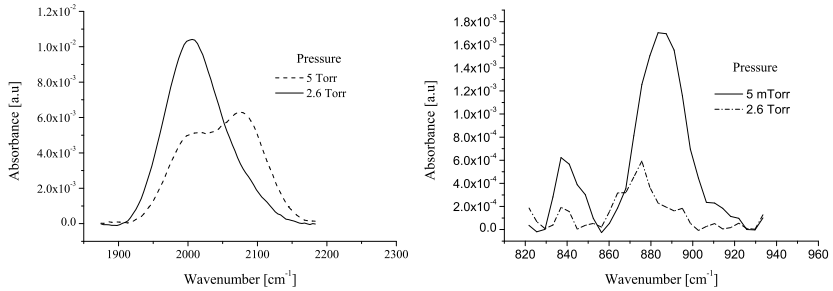


Figure 6.8: Microstructure evaluation as a function of precursor dilution.



(a) (b)

Figure 6.9: (a) Influence of pressure on the infrared absorption due to mono- and polyhybrids of SiH_x at 2000 and 2090 cm^{-1} respectively and (b)Influence of pressure on the infrared absorption due to SiH_2 chains at 840 and 890 cm^{-1}.

Effect of pressure

The effect of the pressure on the deposited film was studied while keeping other plasma parameters constant: precursor dilution at He/SiH_4=9, spacing at 500 mils, power at 100 Watt and temperature at 300^{o}C. The pressure was varied over the range of 1.5-5 Torr. At the lowest pressure (1.5 Torr) the plasma failed to ignite, hence no deposition was possible at this pressure.

Figure 6.9a depicts the absorbance spectrum in the 2000-2090 cm^{-1} band. At higher pressure the absorbance at 2090 cm^{-1} indicates formation of clustered SiH and $SiH_{x=2,3}$. However this peak disappears at low pressure, which can be attributed to a decrease in the radical density in the plasma at lower pressure. This can be explained as follows: at a constant gas flow, when the pressure is increased the mean free path of the gas molecules is reduced. This leads to a chain reaction between the precursor (SiH_4) and dissociated radicals (e.g. SiH_2) forming $(Si-H_{2,3})_n$ like networks [30]. This is verified from the absorption peak around 840 and 890 cm^{-1} (Fig. 6.9b), which corresponds to clustered $Si-H_3$ and $Si-H_2$ respectively. The peak at 840 and 890 cm^{-1} diminishes when the pressure is decreased, which clearly indicates that at lower pressure the $(Si-H_{2,3})_n$ chain formation is arrested, resulting in the formation of a void free and dense film.

Effect of power

The power applied to create the plasma is an important deposition parameter, which facilitates dissociation of the precursor gas. To study the effect of applied power on the film composition the applied power is changed between 100-300 Watts, while the other parameters were kept constant at their nominal value as indicated in table 6.3.

We observe an increase in the $Si-H$ monohydride peak (2000 cm^{-1}) with an increase in applied power (Fig.6.10a), while no polyhydride peak (2090 cm^{-1})

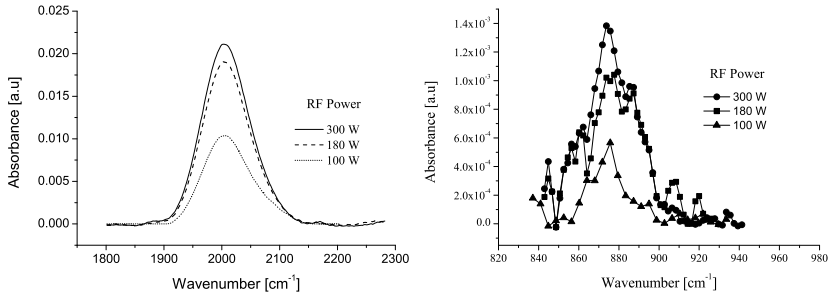


Figure 6.10: (a) Influence of plasma power on the infrared absorption due to mono- and polyhybrid of SiH_x at 2000 and 2090 cm^{-1} respectively and (b)Influence of plasma power on the infrared absorption due to clustered $Si-H_3$ and $Si-H_2$ at 840 and 890 cm^{-1} respectively.

was observed. However, the clustered $Si-H_2$ peak at 890 cm^{-1} appears at higher power and diminishes when the power is reduced (Fig.6.10b). Due to the existence of a higher radical density at high plasma power the chain reaction leads to $(SiH_2)_n$ formation, which is reduced at lower plasma power. From the literature, we have found that better quality $\alpha - Si:H$ is often achieved at low plasma power [7, 18]. We believe the reduction in $(SiH_2)_n$ is one of the reasons for this.

6.3.3.3 Crystallinity : X-ray diffraction and transmission electron microscopy

The crystalline nature of the deposited film was studied with glancing angle (1^o) X-ray diffraction (XRD). The measurements were compared with the ones obtained from SE and FTIR presented in sections 6.3.3.1 and 6.3.3.2 respectively.

Figure 6.11 shows the crystallinity of films deposited with different silane dilutions. Two peaks can be distinguished in the spectrum. The broad peak around $\approx 52^\circ$ corresponds to scattering of the Si lattice from the substrate due to thermal vibration. The peak at 28° corresponds to the $Si < 111 >$ crystal in the deposited film. This peak smears out and disappears with an increase of the precursor dilution, which indicates that the film evolves from a microcrystalline phase(at low dilution) to an amorphous phase (at higher dilution). The crystallinity of the film is also a good indication of the film density: we observe an excellent agreement between SE (Fig.6.6) and XRD characterization. Low crystallinity corresponds to high refractive index. In addition, the microstructure (Fig.6.8) of the films also correlates with the crystallinity of the film.

The amorphous nature of the film was also confirmed by using a transmission electron microscopy (TEM) and selected-area diffraction (SAD). Even though a weak $< 111 >$ peak was observed in the XRD spectrum, we were unable to observe the atomic order from SAD and TEM. Figure 6.12 shows the result from the films deposited with a dilution (He/SiH_4 of 9 and 2). A circular ring in

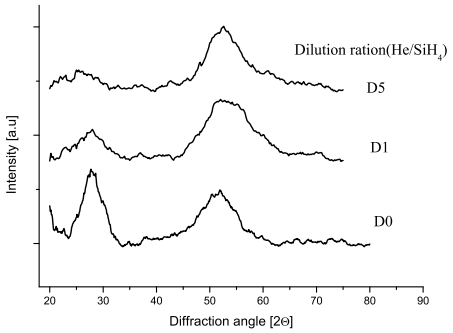


Figure 6.11: X-ray diffraction spectrum of α-Si:H films deposited with different silane dilutions. D0, D01 and D05 represent dilutions 0, 1 and 5 respectively.

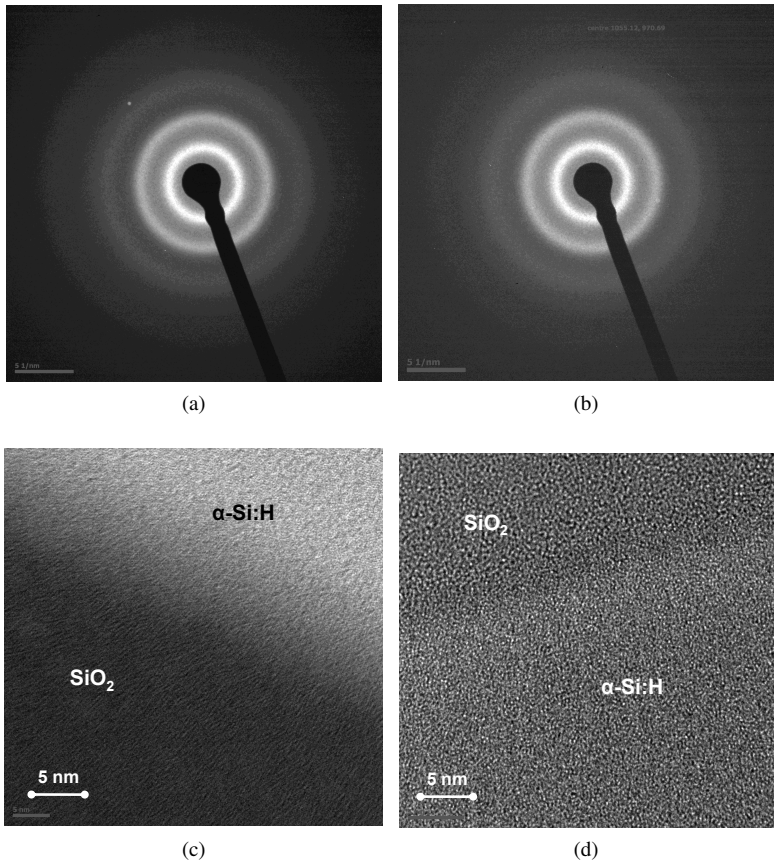


Figure 6.12: SAD of a film deposited with a dilution of (a) 9 and (b) 2, and (c) and (b) shows the corresponding TEM image of the film and its interface with SiO_2.

the SAD image (Fig. 6.12a&b) without distinct diffraction pattern indicate the amorphous nature of the film. In addition to bulk SAD, the interface between the SiO_2 and α-Si:H also shows amorphous behavior. Figure 6.12c&d show the amorphous nature of the interface and bulk of the film.

6.3.3.4 Stress

The two main reasons for having stress in a thin film are molecular interactions and differential thermal expansion coefficients (TEC). The stress (σ) induces wafer bow and therefore can be determined from the wafer curvature. The stress induced by a given layer is calculated from measuring the wafer radius before and after the deposition. This also allows to determine if the stress is either tensile or compressive. Equation 6.4 relates stress and the wafer parameters.

$$\sigma = \frac{1}{6}\frac{Y}{1-\nu}\frac{t_s^2}{t_f}\left[\frac{1}{R_f} - \frac{1}{R_s}\right]. \tag{6.4}$$

Where t_s is the thickness of the silicon substrate, t_f is the thickness of the deposited film, R_s and R_f are the wafer radius before and after deposition respectively, ν is the poisson's ratio of the wafer and Y is the young's modulus of the substrate.

Figures 6.13a and 6.13b show the effect of dilution and plasma power on the stress in the deposited $\alpha - Si : H$ film. We observe that the stress is mostly compressive, and it increases with increase in dilution and on the contrary, decreases with increase in the plasma power. The stress changes from tensile to compressive when the feed gas dilution is increased from 0 to 25. This transition can be explained from the changing diffusion length of the radicals on the surface. As mentioned earlier (in section 6.3.3.1) at higher radical arrival rate (R_{ar}), the diffusion length is restricted, and this results in a columnar structure. Due to an inter-molecular attraction between the Si atoms in the columns, neighbouring columns induce a tensile stress. On the other hand, at higher dilution (or lower R_{ar}) the densely packed Si atoms repel each other resulting in a compressive stress (Fig.6.13b).

From FTIR and XRD characterization, we observe that higher dilution and lower power yield films with low microstructure, which is important to achieve low-loss waveguides. Although stress in itself does not affect the propagation loss, the wafer bow (Fig. 6.13a and 6.13b) of the films deposited at low power and high dilution is unacceptable for further processing. E.g. during the lithography process, the focus over a wafer with bow will vary resulting in a large variation in the linewidth [31]. For larger bow, the substrate holder used in the lithography tool will reject the wafer. Hence we had to limit our feed gas dilution and power to ≤ 9 and $\geq$180 Watts respectively.

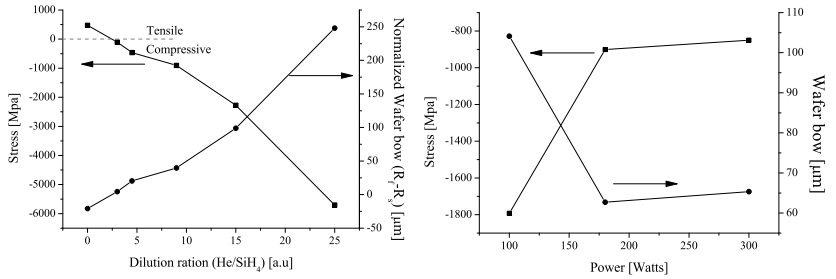


Figure 6.13: (a) Influence of plasma power on the infrared absorption due to mono- and polyhybrid of SiH_x at 2000 and 2090 cm^{-1} respectively and (b)Influence of plasma power on the infrared absorption due to clustered $Si-H_3$ and $Si-H_2$ at 840 and 890 cm^{-1} respectively.

6.3.3.5 Surface morphology : Atomic force microscope

The surface roughness of the film deposited with the optimized deposition condition (180Watts, 2.6 Torr, precursor dilution 9) was characterized using atomic force microscopy (AFM). The surface roughness of deposited films is often influenced by substrate roughness, and therefore, we prepared all the films on a polished oxide surface with a surface roughness of 0.1 nm rms. We found that the surface roughness of $\alpha - Si : H$ film increases with an increase in the thickness of the film. A roughness of 1.4 and 2.1 nm was measured for a film thickness of 220 and 440 nm respectively (Fig.6.14). As the surface roughness of the film can cause scattering of light eventually resulting in propagation loss, we have used chemical mechanical polishing (CMP) to smoothen the surface. After polishing the surface roughness of the films was 0.23 nm and 0.25 nm for 220 nm and 440 nm thick films respectively. During CMP ≈40 nm of material is consumed, which should be taken into account during the initial deposition process.

6.3.3.6 Optical characterization

The optical propagation losses of the deposited $\alpha - Si : H$ films in the telecommunication wavelength range 1500-1600 nm were characterised by using photonic wire waveguides. The propagation loss of a photonic wire waveguide is mainly caused by three phenomena: scattering of light from the sidewalls of the photonic wire, scattering of light inside the core due to voids/microstructures and absorption in the core. The propagation loss measurement gives the combined effect of these three loss factors. We studied the effect of the precursor gas dilution and the plasma power on the propagation loss of the photonic wires.

The photonic wires were fabricated in 220 nm thick as-deposited $\alpha - Si : H$ on top of 1950 nm of surface polished high-density plasma oxide. Photonic wire

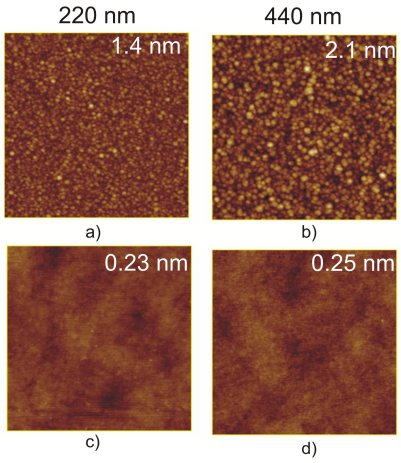


Figure 6.14: Surface roughness before (a,b) and after (a,b) polishing of 220 and 440 nm α-Si:H.

(≈450 nm) patterns with varying length (0.6 - 6 cm) were defined using 193 nm optical lithography and dry etching 3. To compare different materials, we used the same patterning process for all wafers, thereby keeping the effect of the sidewall roughness fixed. As crystalline silicon is a well known low-loss material, we have also fabricated photonic wires in a crystalline Si wafer for comparison.

To characterize the propagation loss of the different materials, light from a broad-band light source is coupled into the waveguide and the output is measured using a spectrum analyzer. We use grating fiber couplers [32] to couple the light in and out the photonic wires. Table 6.5 summarizes the effect of precursor gas dilution and plasma power on the propagation loss. The propagation loss does not change appreciably with decreasing plasma power (180-300 Watts). As mentioned earlier we were unable to pattern the film deposited at 100 Watts due to wafer bow, which restricted us to operation above 100 Watts. On the other hand, higher dilution clearly shows a considerable improvement in the propagation loss, from immeasurably high loss to 3.46 dB/cm. To our knowledge this is the lowest propagation loss reported for photonic wires of this dimension (450 $\times$ 220 nm) fabricated in $\alpha - Si : H$.

The propagation loss shown in table 6.5 is a combination of material loss and sidewall scattering loss. In order to assess the material loss of the best material, shallow etch (70 nm) ridge waveguides with varying length were fabricated in a 220 nm thick $\alpha - Si : H$ layer. The bending radius of the spirals was kept large (70 μm) to avoid radiation loss. By deducing the propagation loss measured for crystalline SOI based photonic wires fabricated using a similar process from the $\alpha - Si : H$ wire loss, we can estimate the bulk material loss to be ≈0.7 dB/cm. The loss measurement shows a propagation loss of 1.37±0.07 dB/cm, wich is

Material	Dilution ratio (He/SiH_4)	Power [Watts]	Wire loss [dB/cm]
$\alpha - Si : H$	9	100	NA
$\alpha - Si : H$	9	180	3.46 ± 0.04
$\alpha - Si : H$	9	300	3.7 ± 0.08
$\alpha - Si : H$	5	180	4.25 ± 0.04
$\alpha - Si : H$	3	180	4.94 ± 0.04
$\alpha - Si : H$	0	180	$veryhigh$
Crystalline Si	-	-	2.8 ± 0.09

Table 6.5: Propagation loss of $\alpha - Si : H$ photonic wires for various precursor gas dilution and pressure, while other parameters were kept constant (wafer temperature=330 °C, Pressure=2.6 Torr, spacing=500 mils).

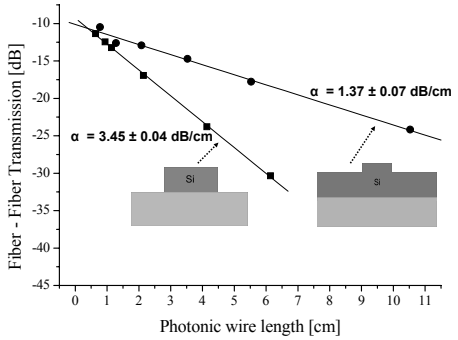


Figure 6.15: Propagation loss of a photonic wire and ridge waveguide fabricated in α-Si:H.

twice the expected material loss (Fig.6.15). The measured ridge waveguide loss can be considered as an upper estimate for the bulk loss since in these waveguides the interaction between propagating mode and sidewall roughness is considerably reduced in comparison to photonic wires.

The propagation loss of $\alpha - Si : H$ photonic wires reported so far spans between 40 and 2.7 dB/cm depending on the cross-section and material quality. The lowest loss of 2.7 dB/cm was demonstrated by using an unconventional waveguide geometry (700×100 nm^2). The loss improvement was achieved by covering the waveguides with a thin layer (10 nm) of plasma treated silicon nitride (SiN). The authors claim that the plasma treatment improves $\alpha - Si : H$ passivation and reduces unwanted $N - H$ bonds from the SiN films.

In this work, by using CMOS fabrication tools and by engineering the deposition process, we demonstrated low-loss photonic wire waveguides and single-mode ridge waveguides with a loss of 3.45 dB/cm and 1.37 dB/cm, respectively. Since the deposition was done at low temperature (300^{o}C) the material is ideal for

Ref	Material Loss [dB/cm]	Wire Loss [dB/cm]	wire dimension [nm]	Top cladding
[7]	1.5	40	500×250	Air
[18]	< 1	6.5	500×200	SiN
[33]	-	2.7	700×100	SiN/SiO_2
	-	12	700×100	SiO_2
	-	6.5	700×100	SiN/SiO_2
[34]	0.5	4.5	500×200	SiO_2
[5]	-	14	400×250	SiO_2
This work	0.7	3.45	480×220	Air
This work	–	3.4	480×220	SiO_2
[19]	-	2	1100×1300, 380 nm *	Air
This work	-	1.37	500×220, 70 nm *	Air

Table 6.6: Propagation loss comparison from the literature.
** indicates ridge waveguides, width×height, etch depth.*

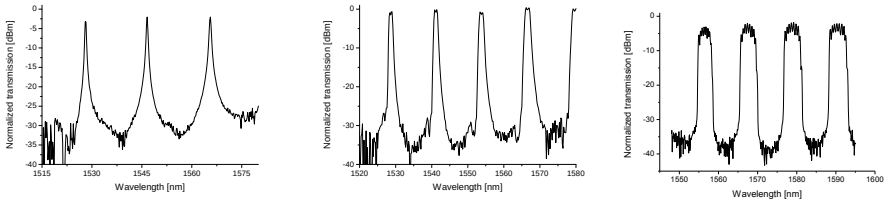
back-end CMOS-photonics integration.

6.3.4 Wavelength selective devices in $\alpha - Si : H$

Fabricating photonic devices in $\alpha - Si : H$ is no different from crystalline Si. In order to assess the performance of wavelength selective devices, we have fabricated ring resonator based filters, planar curved gratings and arrayed waveguide gratings in $\alpha - Si : H$. The devices were fabricated in a 220nm thick $\alpha - Si : H$ deposited on top of 2000 nm surface polished SiO_2. 193 nm optical lithography and dry etch was used for pattern definition [31].

Ring filters: Ring resonator filters were implemented by using single and multiple rings (2^{nd} and 20^{th} order) in racetrack configuration. A compact single ring drop filter was implemented with a ring radius of 3 μm, coupling length of 4 μm and a coupling gap of 200 nm. The width of the photonic wire was kept at 450 nm. Figure 6.16a shows the drop response of a first order ring resonator. A free spectral range of 18.8 nm was achieved as a result of a compact resonator. A quality factor of ≈3515 was observed with a high out-of-band rejection of 30 dB.

The 2^{nd} and 10^{th} order ring filters were implemented as side coupled rings. The two main advantages of higher order filters are the flat-top response and large out-of-band rejection. In order to achieve a flat top response, the 2^{nd} order ring was implemented with varying coupling gap (140 nm, 200 nm, 140 nm) [35], while the coupling length and ring radius were kept at 4 μm and 5 μm respectively. The 10^{th} order ring filter was implemented with a uniform coupling gap of 180 nm with a coupling length of 4.5 μm and a ring radius of 12 μm. Figure 6.16b and 6.16c depict the drop response of the 2^{nd} and 10^{th} order ring filter, which shows a



(a) (b) (c)

Figure 6.16: Drop response of a ring filter of a (a) 1^{st} order, (b) 2^{nd} order and (c) 10^{th} order.

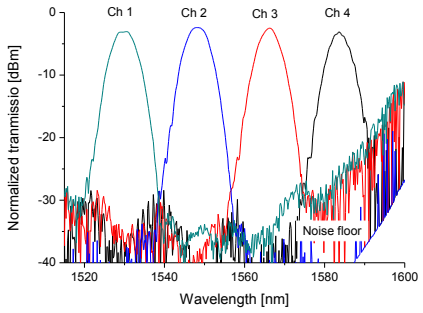


Figure 6.17: Superimposed transmission spectra of 4 channels of a 1×4 planar curved grating with DBR facet. [courtesy device design J. Brouckaert]

free spectral range of 12.7 nm and 11.2 nm and an out-of-band rejection of over 30 dB and 35 dB respectively. A passband ripple of ≈5 dB was observed in the 10^{th} order filter, while only 0.5 dB was observed from the 2^{nd} filter. These ripples can be reduced by design optimizations, for example, varying the coupling between the rings.

Planar concave gratings: Planar concave grating demultiplexer (PCG) is an excellent
device for coarse wavelength division multiplexing [36]. Figure 6.17 depicts the superimposed transmission spectra of 4 channels from a 1×4 PCG with DBR-type facets [37]. The channels were spaced at 17.6 nm with an insertion loss of the four channels were 3.05, 2.39, 2.47 and 3.2 dB and an average cross talk of 30 dB. The observed crosstalk is slightly (≈ 5dB) better than the PCG's in crystalline Si, possibly due to better thickness uniformity over the device. However, due to non-optimal DBR mirrors, the insertion loss was on average 1 dB higher.

Arrayed waveguide gratings: Arrayed waveguide grating demultiplexers (AWG) are one of the most flexible and scalable narrow band filter. Figure 6.18 shows the

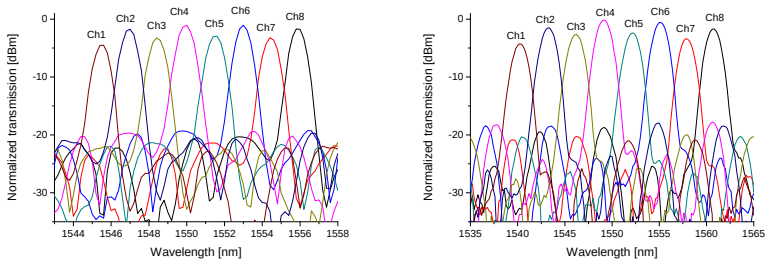


Figure 6.18: Superimposed transmission spectra of a 8-channel arrayed waveguide grating with a channel spacing of (a) 8×200 GHz and (b) 8×400 GHz.

	MZI		2nd order ring demux		PCG		AWG	
	a-Si	C-Si	a-Si	C-Si	a-Si	C-Si	a-Si	C-Si
Insertion loss (<dB)	2	3.5	0.5	0.5	3	3.6	3	3
Crosstalk (≈dB)	-	-	14	11	30	30	18	18
extinction (dB)	>20dB	>20dB	-	-	-	-	-	-

Table 6.7: Performance comparison between devices fabricated in $a-Si:H$ and crystalline Si.

superimposed spectra of 8 channels of a 8 × 200 GHz (1.6 nm) and 8 × 400 GHz (3.2 nm). Both devices exhibit a non-uniform insertion loss from channel to channel. However, the non-uniformity is systematic and the actual reason for this non-uniformity is not clear at this point. The crosstalk levels of the devices are comparable to the devices fabricated in crystalline Si.

Table 6.7 shows the performance comparison between devices fabricated in $a-Si:H$ and crystalline Si. The performance figures, namely, insertion loss, crosstalk and extinction ration does not show a good correlation between two material platform. This clearly shows that the performance of the device fabricated in $a-Si:H$ are comparable to those in crystalline Si.

6.4 Thermal Trimming and Tuning of $\alpha-Si:H$ photonic devices

As mentioned earlier in chapter 4, high refractive index contrast photonic devices are very sensitive to small dimensional changes. These dimensional changes can

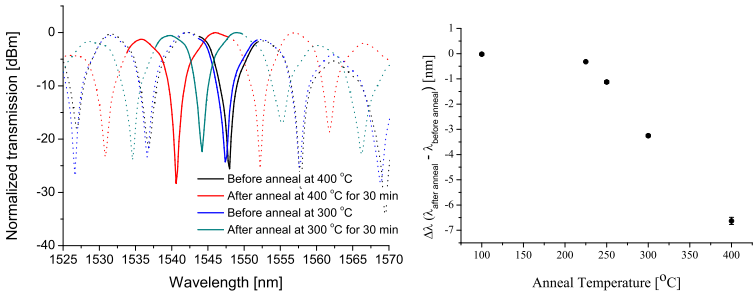
be compensated by post fabrication trimming (permanent) or tuning (temporary) the devices. The primary goal is to change the effective index (n_{eff}) of the device, which determines the device response to obtain a value. The n_{eff} of the device can be modified either by changing the refractive index of the core or the cladding. It has been shown that by using a photosensitive organic cladding material photonic devices in silicon nitride can be trimmed as much as 23.5 nm [38]. Similarly, trimming was achieved by compaction of burried oxide in a SOI based Si photonic device, where an electron beam was used for trimming [39]. On the other hand, there are no reports on trimming of the core refractive index. In this section, a trimming and tuning method using thermal treatment on the photonic devices fabricated in $\alpha - Si : H$ is explored. This technique allows change in the refractive index of the core material, which can be exploited as a compensation for fabrication imperfection of the devices [40].

The properties of $\alpha - Si : H$, such as the refractive index and crystallinity are strongly influenced by the amount of hydrogen (H) incorporated in the film, and can be controlled by process parameters, such as the substrate temperature, the RF power and the gas flow rate. When the film is in thermodynamic equilibrium, the H in an $\alpha - Si : H$ network manifests itself in different configurations ($SiH_{x=1-3}$) and bond energies. If the equilibrium in the film is disturbed optically [41, 42] or thermally [43–45], bond breaking and reorganization of the network occurs. This results in hydrogen desorption and crystallization. Despite considerable material development, there are no reports on the thermal treatment on the optical properties of deposited a-Si:H. It has been shown that at elevated temperatures the chemical nature of $\alpha - Si : H$ is permanently modified as a consequence of H desorption and crystallization [43]. This results in a change in the refractive index of the material, which can be exploited as a trimming technique.

6.4.1 Experiment

The thermal response of a-Si:H was studied by using two types of photonic wire devices: Mach-Zehnder interferometers (MZI) and long spiral waveguides. The Mach-Zehnder interferometer is used to determine refractive index changes by measuring the spectral response of the device. The spiral waveguides are used to characterize material absorption losses, which can be estimated from the waveguide propagation loss. The 1×1 MZI was composed of two connected Y-splitters with a delay length (δL) of 50μm in one of the two arms. The spiral photonic wires of varying length (0.5 cm to 40 cm) were realized using straight and bend waveguides. A large bending radius of 20 μm was used to avoid any bend loss. The cross section of the photonic wire was 450×220 nm, resulting in single mode waveguides.

The photonic devices were fabricated using 193 nm optical lithography and dry etching [31]. Next the wafer was diced into individual samples. Then the devices in the different samples were optically characterized to obtain the reference spectral response and propagation loss. The optical characterization was done by injecting TE polarized broadband (1500-1600 nm) light from a superluminicent



(a) (b)

Figure 6.19: (a) Transmission spectrum of Mach-Zehnder interferometer before and after annealing at 300 and 400 ^{o}C (b) Effect of anneal temperature on spectral shift of Mach-Zehnder interferometer.

light emitting diode (SLED) and measuring the output through an optical spectrum analyser. After reference measurements, each sample was annealed at different temperatures ranging from 100 to 600 ^{o}C for 30 minutes in a nitrogen ambience. To avoid thermal shock, the samples were loaded and unloaded at cleanroom temperature, while the raise and fall temperature was set at 10 ^{o}C/min. Finally, the annealed samples were optically characterized again at room temperature. Some of the unannealed samples were characterized at elevated temperatures to measure the thermo-optic effect. In order to compare the optical response and the material compositional changes FTIR was carried out on un-patterned samples, which experienced similar thermal treatment as the devices.

6.4.2 Trimming action and the cause

Figure 6.19 shows the spectral shift of the MZIs before and after annealing. A blue-shift (towards lower wavelength) is observed with increase in anneal temperature (Fig. 6.19b). The observed spectral shift can be attributed to a reduction in the effective refractive index (n_{eff}) of the photonic wire. Through numerical simulations we have found that 1 nm wavelength shift corresponds to a change of 2.9e-3 in the effective refractive index of the zeroth order guided mode.

The measured wavelength shift follows a linear trend beyond a critical temperature (T_c) of 200 ^{o}C (Fig. 6.19) reaching a maximum shift of -6.6 nm at 400 ^{o}C. Below the critical temperature T_c no wavelength response is observed. Due to the strongly increasing propagation loss, we were unable to measure samples annealed above 400 ^{o}C. However, for temperatures below 400 ^{o}C the loss did not vary beyond 0.2 dB/cm(Fig. 6.21).

The change in the spectral response and the propagation loss can be directly related to a permanent change in the material properties of $\alpha - Si : H$ after annealing. The amount of H in a silicon network affects the properties of the $\alpha - Si : H$ film, including the film density. It is well known that at an elevated

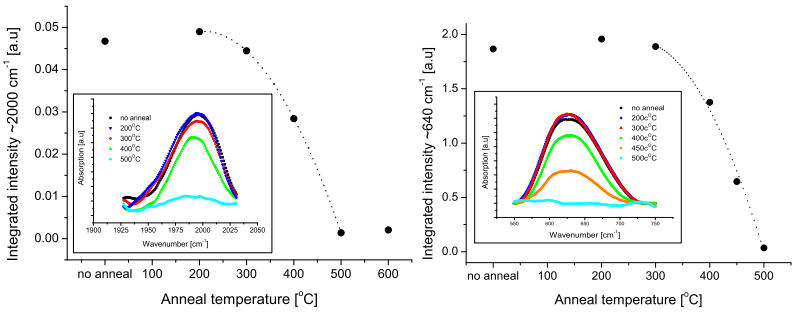


Figure 6.20: Integrated Fourier transformed infra-red peaks at (a) 2000 cm^{-1} and (b) 640 cm^{-1}. The inset shows the corresponding spectrums.

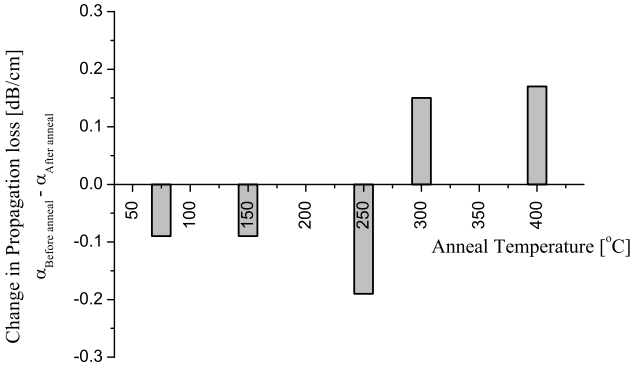


Figure 6.21: Change in propagation loss of photonic wires as a function of anneal temperature.

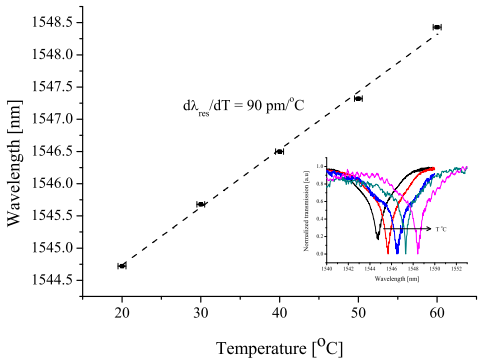
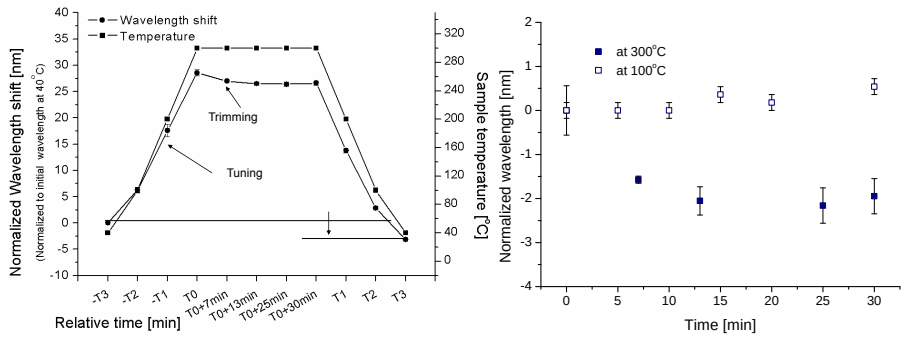


Figure 6.22: Thermo-optic effect of a-Si:H, inset shows the spectral shift of a Mach-Zehnder interferometer at different temperatures.

temperature the mobility of H in the film increases, resulting in desorption of H from the Si network. The two main consequences of H desorption are a decrease in refractive index and creation of Si dangling bonds. As discussed earlier, the three important FTIR phonon mode bands related to the different $Si-H$ bond configurations are located at 640, 2000 and 2100 cm^{-1}. Figure 6.20a and 6.20b show the integrated intensity and the absorption spectra for $Si-H$ monohydride at 2000 and 640 cm^{-1}. It is obvious from these figures that the intensity of the 2000 and 640 cm^{-1} peaks starts to decrease beyond the critical temperature T$_c$. This clearly indicates that the observed wavelength shift is a result of H desorption. As mentioned earlier, Si dangling bonds are created due to the loss of H. As a consequence, the propagation loss is expected to increase due to absorption. Despite this, we did not observe a considerable change in the propagation loss up to 400 ^{o}C (Fig. 6.21). This suggests a reorganizing mechanism in the network below 400 ^{o}C, which reduces the dangling bond density. Beyond 400 ^{o}C loss of most H atoms (Fig. 6.20a and 6.20b) results in a high dangling bond density and a very high propagation loss.

The critical temperature (T$_c$) clearly demarks two regions; a chemically stable ($<$T$_c$) and an unstable ($>$T$_c$) operating region. These two regions can be used to carry out a post-fabrication compensation of fabrication inaccuracies. It is clear from our experiments that above T$_c$ the devices can be trimmed towards lower wavelength. On the other hand, since the material is chemically stable below T$_c$, in this region the thermo-optic effect can be exploited to tune the device towards higher wavelengths. Due to the positive TO coefficient [46], we observe a red shift of 90 pm/^{o}C ($d\lambda/dT$). This is illustrated in Fig. 6.22, which shows the wavelength shift of a MZI as a function of the operating temperature. The total achievable tuning then ranges from -6.6 nm to +18 nm.

In addition to the static measurement, a time resolved measurement of the wavelength shift with temperature shows that the evolution of H stabilizes within 10-15 min of annealing time. Figure 6.23a shows the wavelength shift as a func-



(a) (b)

Figure 6.23: Time resolved wavelength shift as a function of the temperature (a) wavelength shift at different operating temperature showing, trimming and tuning action and (b) Change in wavelength at 100 and 300^{o}C for increasing anneal time.

tion of sample temperature. Initially, there is a red shift due to the TO-effect and once the temperature increase beyond T_c the wavelength starts to blue shift and stabilizes after 15 min. A closer look at the wavelength shift during annealing temperatures above and below T_c shows that a stable operation can be achieved for temperatures $<T_c$, while for $>T_c$ after trimming a stable operation is observed within 15 min (Fig. 6.23b).

6.4.3 Summary

In this section, we have explored deposition of $\alpha - Si : H$ at low temperature (300^{o}C) using a plasma enhanced chemical vapour deposition technique. Silane (SiH_4) was used as the precursor gas with He dilution to form $\alpha - Si : H$. Various process parameters, such as dilution, pressure and power were studied on their effect on the film property. Material study and optical characterization show that films deposited at higher dilution and low power yield low-loss $\alpha - Si : H$. We have measured a propagation loss of 3.46 and 1.37 dB/cm for photonic wire and ridge waveguides. Using the low-loss $\alpha - Si : H$, we have demonstrated wavelength selective devices such as, ring (de)multiplexers, single and higher-order ring filter, Mach-Zehnder interferometer, AWG and PCG demultiplexers. We have proposed a trimming technique for photonic devices fabricated in $\alpha - Si : H$. By controlling the H release from the film, without degrading the propagation loss, a maximum blue shift of 6.6 nm was demonstrated. Since the refractive index of the material changes $>T_c$, the final material index after device fabrication depends on the thermal budget. Irrespective of the process temperatures, a final anneal can be used to standardize the refractive index. This work shows that deposited $\alpha - Si : H$ is nearly as good as crystalline Si for passive photonic device fabrication and has additional advantages such as flexible layer thickness with good thickness

uniformity, device response trimming and back-end CMOS integration.

6.5 Polycrystalline silicon

Polycrystalline silicon (Poly-Si) as waveguide material was first demonstrated in 1996 by Foresi et al [47]. Since then progress has been made in material study and device fabrication. High propagation loss in the waveguides is considered as the prime obstacle for photonic circuits fabricated in Poly-Si. The propagation loss in multimode photonic wires have been reduced from 75 dB/cm to 11 dB/cm through material and process engineering [48–50]. Active photonic wires devices, such as a ring resonator modulator have been recently reported with low carrier recombination rate [51]. Since poly-Si can be readily deposited, it can be used for building multilayer photonic circuits [6]. Unlike PECVD $\alpha - Si : H$, Poly-Si requires high deposition temperatures, which limits its applications to front-end integration. However, poly-Si is very attractive for applications where process temperature freedom is available and active functionalities such as carrier injection modulators.

The three main causes for loss in polycrystalline material are (1) surface roughness, (2) scattering at the grain boundaries and (3) absorption by dangling bond defects in the bulk and at grain boundaries. All the mentioned loss mechanism can be reduced by optimising the deposition and device fabrication process. The scattering loss, in particular, can be reduced by reducing the number of grain boundaries. As mentioned in section 6.3 the dangling bond defects can be cured by adding H. Since LPCVD amorphous or polycrystalline Si does not contain H it has to be added by annealing the deposited film in a passivating gas atmosphere.

In this section, we explore the suitability of poly-Si as an alternative material technology for high index contrast photonic integrated circuits. Various device processing routes and their consequence on the propagation loss are presented.

6.5.1 Experiment

By using silane (SiH_4) as a precursor gas, which is thermally dissociated, we form a solid Si film on the wafer surface. There are two ways of depositing poly-Si using LPCVD. In the first approach, an amorphous Si film is deposited at a low temperature ($<$560 ^{o}C) followed by crystallization at high temperatures ($>$560 ^{o}C) [47]. Alternatively, poly-Si can be directly deposited at high deposition temperature ($>$560 ^{o}C) [50]. The former method is preferred for photonic device since the later result in small grains and high defect density, which in turn gives a high propagation loss [48].

Table 6.8 illustrates the wafer split to optimize the process route to obtain low-loss poly-Si. The material quality is assessed through propagation loss characterisation using 500 nm wide spiral photonic wires of varying lengths. The photonic wires were fabricated on a 200 mm Si wafer with 220 nm of poly-Si on top of 2000 nm of surface polished HDP SiO_2 BOx layer. No CMP was applied

Process step	Wafers						
	$S1$	$S2$	$S3$	$S4$	$S5$	$S6$	$S7$
Pre-pattern crystallization (700^{o}C)		√	√				
Post-pattern crystallization (700^{o}C)	√			√		√	√
Thermal oxide smoothing (900^{o}C)	√	√				√	√
Hydrogen passivation anneal (450^{o}C)	√	√	√	√	√		√
Deuterium passivation anneal (450^{o}C)						√	

Table 6.8: Process sequence of wafers, √ indicating processed step.

on the poly-Si layer. The photonic wires were fabricated using 248 nm optical lithography and dry etching [52][1]. All the wafers were covered with HDP SiO_2 as cladding material. Figure 6.24 shows the cross-section SEM image, and roughness on the photonic wires. Crystallization anneals was carried out at 750^{o}C in an inert nitrogen atmosphere either before patterning the waveguides (pre-pattern crystallization) or after patterning the waveguides (post-pattern crystallization). In order to reduce sidewall roughness in the photonic wires, a thin layer of thermal oxide (2.6 nm) was grown at 900^{o}C in an O_2 atmosphere. In one of the wafers ($S7$), the oxide thickness was increased to ≈5 nm. Finally, passivation anneal was carried out at 450^{o}C in forming gas (H_2/N_2) or deuterium environment to reduce dangling bond defects in the film. Deuterium, because of its relatively large atomic weight in comparison to hydrogen is believed to be more stable, yet chemically similar to hydrogen passivation [53].

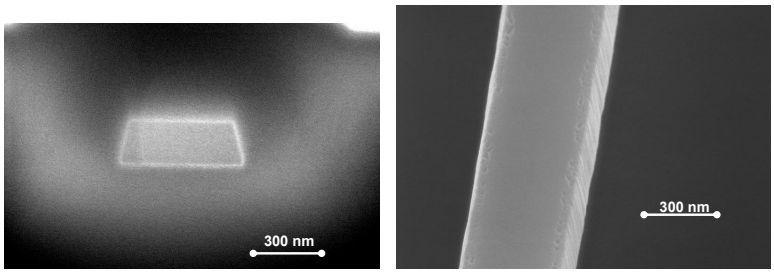
After photonic wire fabrication, the propagation loss of the wires from each wafer was characterized using the cutback method. In addition to propagation loss, crystallinity, surface roughness and film composition were characterized using TEM, AFM and FTIR spectroscopy.

6.5.2 Material characterization

6.5.2.1 Surface and film morphology

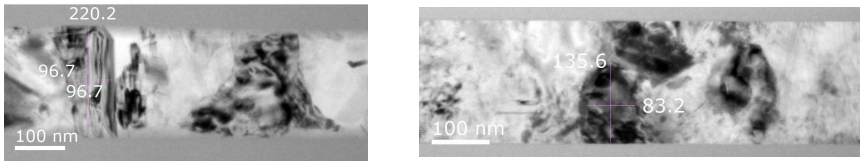
Crystallinity of the fabricated photonic wires and surface roughness was characterized using TEM and AFM. Figure 6.25a shows the crystallinity of a photonic wire from wafer $S1$ which had post-pattern crystallization (700^{o}C) and thermal oxidation (900^{o}C). Figure 6.25b shows the crystallinity of a photonic wire from wafer $S4$ which had post-pattern crystallization at 700^{o}C. In both wafers, the grain size varied between 40 and 220 nm primarily formed along the height of the film. Unlike as deposited poly-Si, which has small columnar grains recrystallized amorphous Si films form large grains, which helps to reduce scattering loss

[1] These experiments were done in the early stage of this research work when 193 nm optical lithography was not yet available for photonics.



(a) (b)

Figure 6.24: Polycrystalline photonic wire (a) emberded in oxide and (b) showing surface and sidewall roughness.



(a) (b)

Figure 6.25: Transmission electron microscope image of polycrystalline Si. Crossection is taken along the light propagation direction of post-pattern annealed waveguides (a) with addition oxidiation anneal (b) without oxidiation anneal.

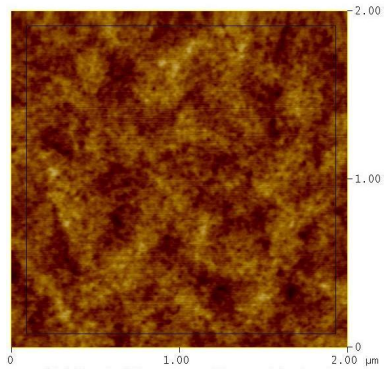


Figure 6.26: Atomic force microscope image of the surface roughness of polycystalline Si showing a roughness of 0.45 nm.

from the grain boundaries. Even though there was no observable variation in the grain size between $S1$ and $S4$, the top surface of $S1$ was slightly rougher than $S4$. This roughness can be due to exposure to the high oxidation temperature ((900^{o}C), which in addition to oxidation recrystallizes the film and can result in inter-grain stress allowing out-of-plane movement of the grains. Despite this grain movement, the surface roughness was only 0.45 nm (Fig. 6.26).

6.5.2.2 Propagation loss characterization

The propagation loss of the poly-Si photonic wires fabricated through different routes (Table 6.8) was measured using spiral wires with varying lengths and is shown in figure 6.27. Wafer $S1$ exhibited the lowest loss of 13.4 dB/cm. This wafer was post-pattern crystallized followed by thermal oxidation and hydrogenation. The pre-pattern crystallized photonic wire measured a loss of 19.76 dB/cm, which is 6.5 dB more than post-pattern crystallization ($S1$). This can be attributed to reduction in the growth centres for crystallization in $S1$, which results in larger grains and fewer grain boundaries.

Wafer $S7$, which was fabricated along with $S1$, except for longer oxidation time exhibited slightly higher loss of 16.55 dB/cm. As mentioned earlier due to longer thermal oxidation time of $S7$ there is a chance of O_2 diffusion through the grain boundaries creating scattering defect along the grain boundaries. Hence, we suspect this increase of $\approx$3 dB/cm is a consequence of O_2 diffusion. On the other hand, wafers which did not get thermal oxidation had immeasurably high propagation loss ($S3$, $S4$ and $S5$) including the wafer ($S5$) that was left amorphous and H passivated. Photonic wires passivated with Deuterium measured a loss of 19.5 dB/cm, which is $\approx$3 dB more than H passivated. We are not certain about the main reason for this difference. However, since both passivation were done at the same temperature (450^{o}C) and duration (30 min) the diffusion length of D will be shorter than for H due to the larger molecular weight [53]. Hence, a high

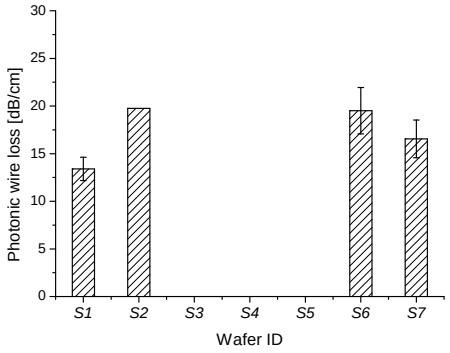


Figure 6.27: Propagation loss of photonic wires (500×200 nm) from different wafer flow (Table 6.8).

temperature and sufficiently long annealing time might reduce the loss further. For H passivation these process parameters were identified as an optimal condition for passivation anneal. After passivation the devices cannot be processed at a high temperature to avoid outgassing of passivating atoms. As explained in section 6.4.2, outgassing can lead to an increase in propagation loss.

6.5.3 Summary

In this section, we have explored polycrystalline Si deposited using LPCVD process. High defect density as deposited $\alpha - Si$ resulted in high photonic wire loss. By crystallizing and hydrogenation, the propagation loss was brought down to 19.76 dB/cm, further more, we found that by crystallizing the photonic wires after patterning the devices the propagation loss was reduced to 13.4 dB/cm. In addition to crystallization and hydrogenation, thermally grown SiO_2 provided additional crystallization and surface smoothing. However, prolonged oxidation resulted in degradation due to O_2 diffusion into the film. In summary, we have identified an optimum process route for fabricating polycrystalline Si photonic wires, which could be used for specific front-end applications.

6.6 Conclusions

In this chapter, we have outlined fabrication and characterization of deposited silicon-on-insulator technology for photonic integrated circuits. Three types of silicon dioxide and two type of deposited silicon were explored as cladding and waveguide material. The presence of $-OH$ molecules in the deposited silicon dioxide was identified as one of the major causes for the absorption loss in the cladding. Silicon dioxide deposited using high density plasma chemical vapour deposition was found to be the most suitable as buried oxide and top cladding, because it had no $-OH$ molecules and showed negligible absorption.

Amorphous and polycrystalline Si was developed and studied for their application in integrated photonic circuits. By using a low temperature (300^{o}C) plasma enhanced chemical vapour deposition process we have developed a low-loss amorphous Si layer. Propagation loss as low as 3.45 dB/cm and 1.37 dB/cm was achieved for photonic wire and ridge waveguides respectively. The achieved loss is comparable to similar devices fabricated in crystalline Si. The low-loss was achieved through process optimisation and material study. We have also demonstrated wavelength selective devices in $\alpha - Si : H$ with performance comparable to its crystalline counterparts. In addition, by exploiting the thermal properties of amorphous Si, a trimming scheme was demonstrated with a trimming range of 6.6 nm. The low temperature requirement for deposition and the interesting thermal and optical behavior of $\alpha - Si : H$ makes it an attractive alternative platform for integrated photonics and back-end CMOS integration.

Polycrystalline Si deposited using low pressure chemical vapour deposition was developed for low-loss photonic circuits for front-end CMOS integration. Photonic wires with a loss of 13.4 dB/cm were demonstrated by optimising the fabrication process route. Even though the propagation loss is higher than amorphous and crystalline Si, it can be used in specific applications. Post-pattern crystallisation and hydrogenation were found to be an optimal fabrication route for low-loss photonic wires.

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7

Application of deposited silicon for multilayer photonic integrated circuits

7.1 Introduction

The functional yield of a photonic integrated circuit can be increased by reducing the footprint of the devices. However, there is a limit to this process, determined by the wavelength of operation and the refractive index contrast. Hence, the most suitable solution for increasing the device density further is to exploit the vertical stacking of circuit layers resulting in multilayer photonic integrated circuits. Multilayer photonic integrated circuits can be realized by two approaches; bonding and deposition. The primary difference between these two approaches is the number of substrates used: in bonding each layer is fabricated on a separate substrate which are subsequently put together, while in the deposition approach multiple layers are fabricated on a single substrate.

Using a bonding approach, Raburn et al demonstrated stacking of two photonic integrated circuits in III-V material technology to fabricate a directional coupler based WDM filter [1]. This approach also enables putting together two different material technologies, which have complementary functionality [2]. Even though the bonding approach can be considered as a versatile technique, there are some limitations. Scalability of the process is a primary concern, which can seriously affect process and device yield.

The most simple approach for vertical stacking is depositing circuit layers on top of each other on a single substrate. With the developement of low-loss high index contrast core materials, such as silicon nitride [3], polycrystalline and amor-

phous silicon [4], depositing multiple circuit layers has become a straightforward approach compared to bonding. Recently, Preston at al reported a double layer photonic circuit, where ring resonstors were implemented in a deposited poly-Si layer evanescently coupled to a signal routing waveguide layer in crystalline Si [5].

The evanescent coupling between different circuit layers was exploited by Koonath et al [6] for implementing a 3-layer photonic circuit, where 3 ring resonators from different circuit layers were vertically coupled. Unlike [5], Koonath et al used a complex layer building approach called Separation by IMplantation of OXygen (SIMOX). In this approach, oxygen is implanted into the bulk Si to create SiO_2 isolation layers, which eventually resulted in two photonic circuit layers. By controlling the implantation energy and thickness of bulk Si, the number of circuit layers can be increased. The need for a high energy oxygen implanter and poor pattern fidelity make this approach less attractive in comparison to a direct deposition and patterning approach.

In this chapter, we demonstrate the use of deposited amorphous hydrogenated silicon ($\alpha - Si : H$) for building a multilayer photonic circuit. First, the requirements for multilayer circuits is outlined followed by the design of various light coupling schemes. Finally, fabrication and characterisation of a complete double layer photonic circuit with an optical via is presented.

7.2 Multilayer photonic circuit requirements

All the multilayer photonic circuit demonstrations until now claim that their approach will increase device density and use silicon real estate efficiently [5, 6]. Unfortunately, this claim could not be made true, since all the demonstrations use evanescent coupling between the layers. For evanescent coupling, the photonic layers should be closely placed for efficient light coupling. On the other hand, this will seriously affect the signal propagation by scattering and interference between the waveguides of different layers resulting in crossing loss. Hence, the circuit layers should be sufficiently isolated to avoid such losses. Figure 7.1 illustrates the typical requirements for a multilayer photonic integrated circuit. The photonic layers should be optically isolated and at the same time there should be a coupling scheme to couple light efficiently between the layers. In the following section, different layer to layer coupling mechanisms are discussed with their advantages and limitations.

7.3 Design of optical via for multilayer photonic circuits

Unlike electrons, photons cannot be transported by a simple vertical waveguide. Issues such as mode matching and reflections have to be addressed. In this section, we investigate a vertical coupling based optical vias: directional coupler, grating

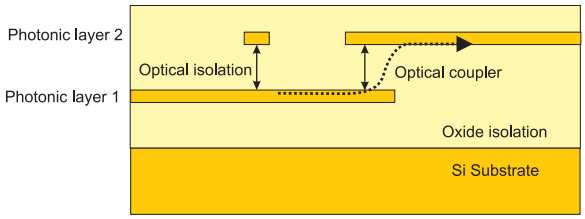


Figure 7.1: Schematic of a double layer photonic circuit showing two prime requirements, optical isolation and light coupling between layers.

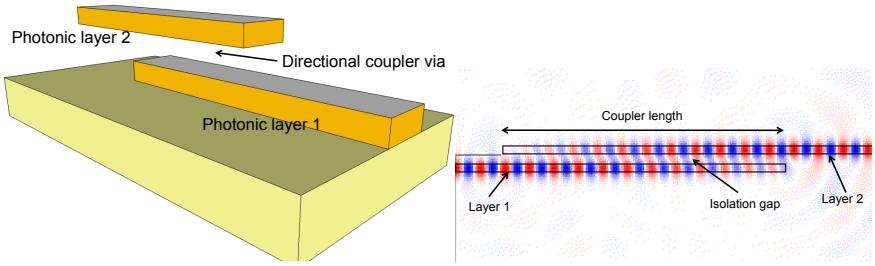


Figure 7.2: (a) Schematic representation of a directional coupler via (b) Simulation cross-section window and design parameters.

coupler and multi-mode interference coupler. The simulations were carried out using the 2D CAMFR mode solver [7].

7.3.1 Design of Directional Coupler Via (DCV)

A Directional coupler via (DCV) is similar to a planar directional coupler, which is used for optical power splitting. Instead of begin laterally coupled, the waveguides are placed vertically with a small gap between them. Figure 7.2 shows a schematic of a DCV and the simulation cross-section with the design parameters. The three primary design parameters of a DCV are the waveguide cross-section, the separation between the waveguides (isolation gap) and the length of the overlap (coupling length). For the 2D simulation, the thickness and refractive index of the photonic layers were fixed at 220 nm and 3.68 respectively.

Figure 7.3 depicts the simulation results of a DCV. The compactness of the DCV depends on the length of the coupler (L), which depends on the gap between the waveguides. Maximum coupling between the layers can be achieved either by decreasing the gap or by increasing the coupling length. Figure 7.3a clearly shows that for a narrow isolation gap of 100 nm maximum coupling of 99 $\%$ (at 1550 nm) can be obtained for a coupler length of only 2.5 μm. For a gap of 400 nm, the

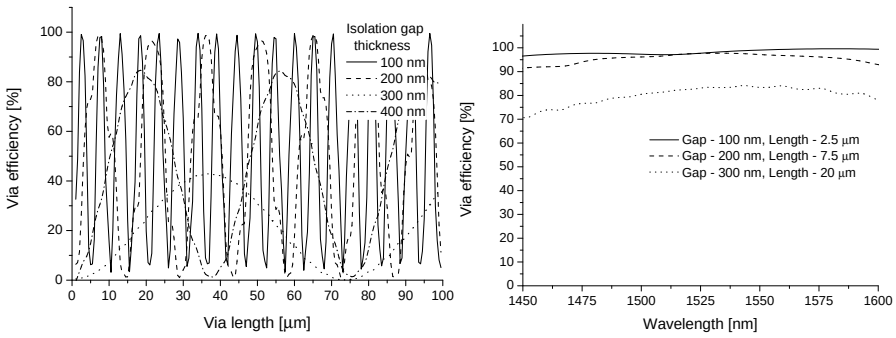


Figure 7.3: Simulated DC via efficiency (a) as a function of coupler length and (b) wavelength response.

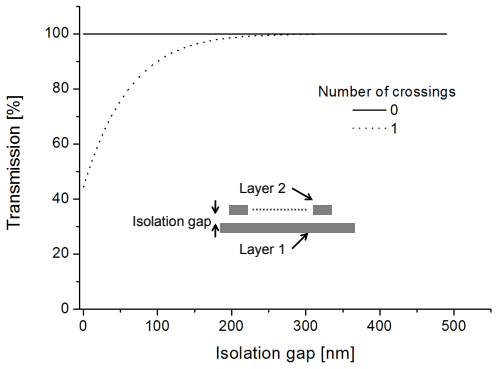


Figure 7.4: Transmssion loss due to waveguide crossing.

length increase to 36 μm for a maximum coupling efficiecy of 43 $\%$. Figure 7.3b shows the via efficiency as a function of wavelength. It can be clearly seen that a broad band ($>$ 100 nm) response can be achieved, where the coupling efficiency does not change over 5 $\%$. However, as mentioned earlier the proximity of the layers can result in crossing loss. Figure 7.4 shows the transmission loss as a result of a waveguide crossing in a double layer circuit. A minimal gap of 350 nm is required to avoid the crossing loss, which directly affects the via coupling efficiency and the length of the via. Hence, DCV can be only used in circuits where separate layers can be used for active devices and signal routing. As mentioned earlier, for high density device stacking sufficient optical isolation between is required in addition to good coupling efficiency. DCVs can deliver high coupling efficiency between the multiple layers. However, due to the thin isolation layer requirement the crossing loss is too high to be used for building multilayer circuits with high device density.

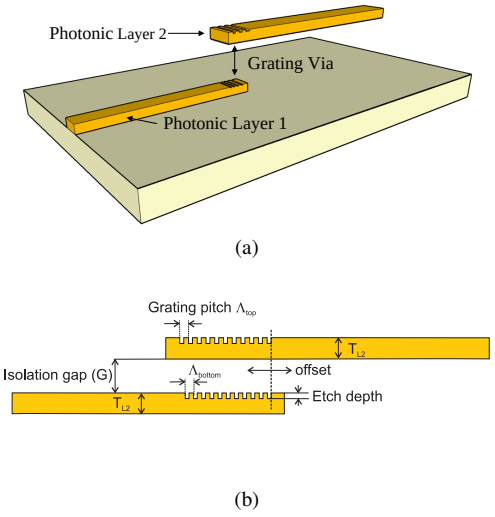


Figure 7.5: (a)Schematic of a single grating via and (b) design parameter.

7.3.2 Design of Grating Via (GV)

Grating couplers are one of the obvious options for vertical light coupling from a planar waveguide. Originally invented for efficient coupling of planar waveguides to an optical fiber [8], a similar approach can be employed for implementing an optical via. Figure 7.5 schematically illustrates a grating via (GV), which is formed by shallowly etched gratings on the waveguides placed above each other. The gratings in the waveguides diffract light out-of-plane, the diffracted light is then captured by an identical grating present above or below the diffracting grating. The grating design depends on the refractive index and thickness of the circuit layer. In our simulations, we used 220 nm of $\alpha - Si : H$ with a refractive index of 3.68 and SiO_2 as the isolation layer with a refractive index of 1.45.

A simple GV is designed by using a grating structure designed for 1550 nm TE polarization having 630 nm pitch and 50 $\%$ fill factor. Identical gratings were placed on top of each other as shown in figure 7.5. The isolation between the waveguides, grating etch depth and off-set were tuned to obtain maximum coupling. The etch depth of the grating was fixed at 70 nm as they are compatible with standard fiber coupler grating and allows to fabricate both the type of gratings together.

The parameters menthoed above were optimised by looking at the transmitted power through a GV. Figure 7.6 shows that the via efficiency as a function of isolation layer thickness. It also shows the effect of refractive index mismatch between the layers. For a matched refractive index layer, a maximum efficiency of 50 $\%$ is achieved for an isolation layer thickness of 1 μm. This thickness is sufficient for good isolation to avoid crossing loss (Fig. 7.4). Figure 7.7a shows the

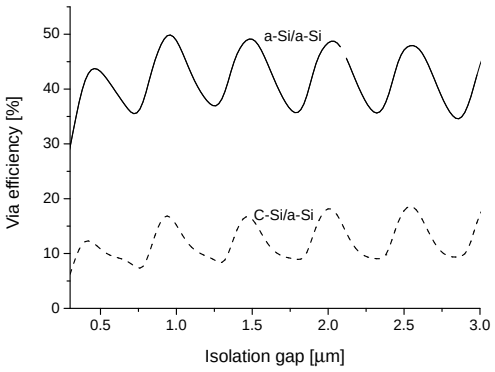
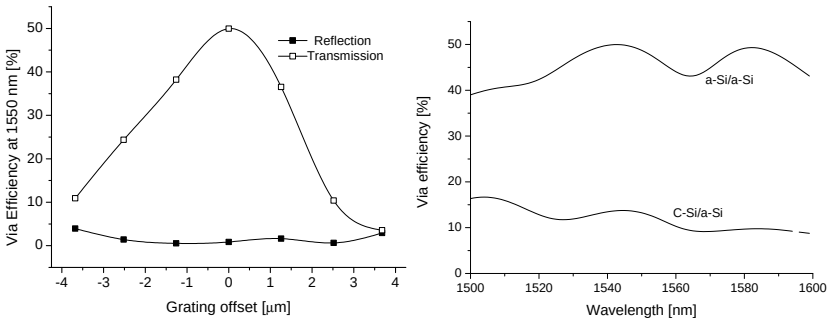


Figure 7.6: Simulated effect of isolation gap on the grating via efficiency at 1550 nm.



(a) (b)

Figure 7.7: Effect of (a) lateral offset between the grating via's and (b) variation in the refractive index between the photonic layers (bottom layer: 3.45, top layer: 3.68).

effect of an off-set on the via efficiency. A loss of 10 $\%$ in efficiency is observed for an off-set of 1 μm. In practice, the alignment tolerances of the lithography tools are within a few 10's of nm, hence the GVs can be fabricated with good alignment tolerance. Mismatch in the refractive index will result in poor modal overlap between the gratings resulting in low via efficiencies (Fig. 7.6). Figure 7.7b shows the effect of the refractive index of the material on the via efficiency. If different materials are used the gratings in each layer have to be optimised to achieve maximum coupling between them.

7.3.3 Design of Multimode Interference Via (MMIV)

A multi-mode interference coupler is a well known power splitting and combining component in integrated photonic circuits. When vertically implemented we can call it a multimode interference via (MMIV). Figure 7.8 is a schematic representation of the proposed MMIV with input and output in different circuit levels. The

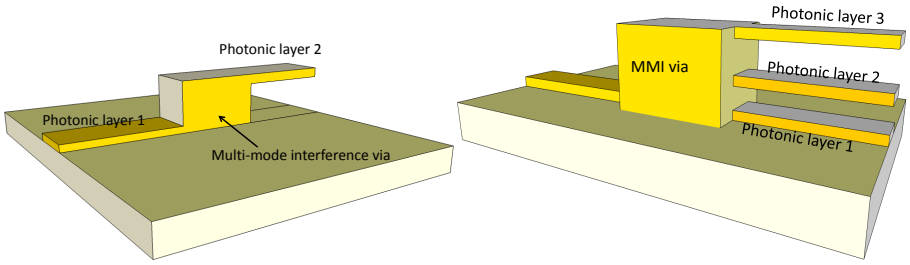


Figure 7.8: Schematic of a (a) simple multimode interference via and (b) distributed multimode interference via.

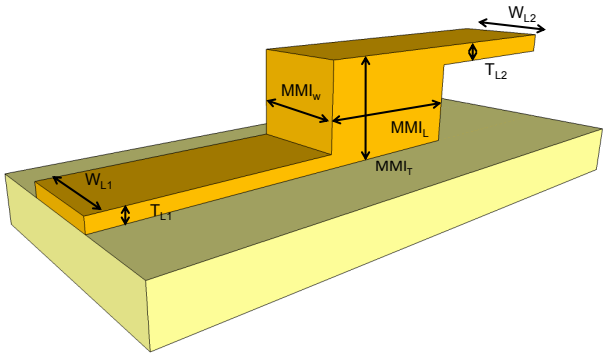
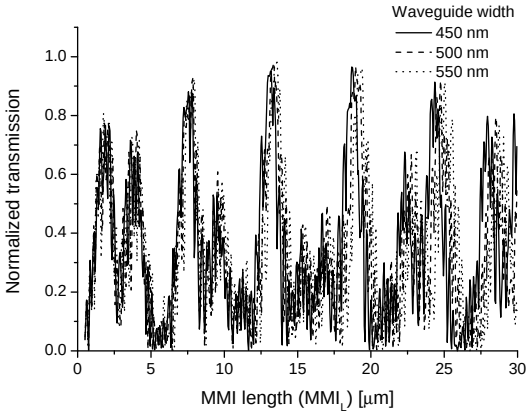


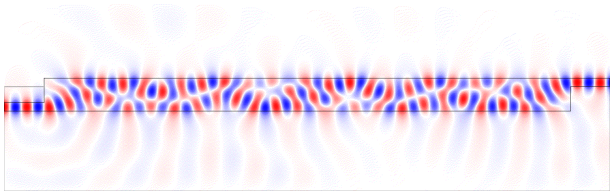
Figure 7.9: Design parameters of a MMI via.

via can be further developed as a complex multi-layer and multi-port configuration as shown in figure 7.8b [9]. Unlike DCV and GCV, different circuit layers have to be connected by a waveguide material, preferably of the same refractive index as the photonic layers to avoid reflections. The working principle of a MMIV is similar to a conventional MMI coupler: a single mode from the access waveguide excites higher order modes in the coupler generating an interference pattern along the propagation direction. Light can be collected by placing the ports at the length where the light constructively interferes.

Figure 7.9 shows the different design parameters of a MMIV. There are seven dimensional parameters and three material parameters that can be optimised to achieve a high via efficiency. In order to simplify the design process, the following was considered: the refractive index was fixed at 3.68, waveguide and MMI width ($W_{L1} = W_{L2} = MMI_W$), and thickness($T_{L1} = T_{L2}$) of the photonic layers were considered identical. The length (MMI_L) and height (MMI_T) of the MMIV were optimised by measuring the output power in layer-2, when layer-1 was excited with a TE fundamental mode. MMI_T dictates the isolation between



(a)



(b)

Figure 7.10: Simulation screen shot showing power transmission from bottom to top photonic layer through a MMI via.

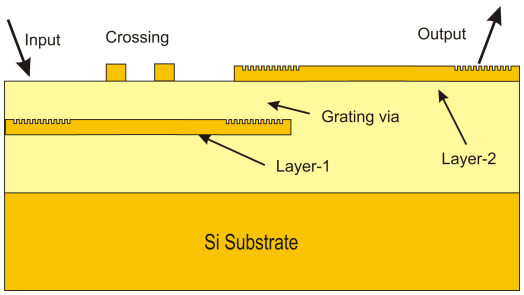


Figure 7.11: Schematic of the double layer test circuit with crossing and grating via test structure.

the photonic layers. We choose 400 nm as an isolation gap between the layer to avoid crossing loss (Fig. 7.4). Figure 7.10 shows the efficiency of a 400 nm high MMIV at 1550 nm for various MMI-lengths (MMI_L), and waveguide and MMI widths. We obtain a coupling efficiency of 98 $\%$ for a MMI_L of 13.35 μm and a $W_{L1} = W_{L2} = MMI_W$ of 500 nm (Fig. 7.10b). The length of the via can be reduced at the cost of via efficiency: a compact via can be achieved with a MMI_L of 1.75 μm with a reduced efficiency of 80 $\%$.

7.4 Double layer photonic circuits

7.4.1 Test Circuit

The grating via was chosen as a test structure to demonstrate a double layer photonic circuit. The GVs were implemented as explained in section 7.3.2. The GVs were defined with a period of 630 nm and 50 $\%$ fillfactor on a 3 μm wide photonic wire in both layers. The length of the GV was chosen as 15 μm for both the layers. Some of the GVs were misaligned to assess the effect on the coupling efficiency. Misalignments of 70, 90, 130 and 200 nm were introduced along the propagation direction. An intermediate layer thickness of 1000 nm was chosen allowing good isolation between the layers. In addition to the GVs, waveguide crossing loss measurement structures were also implemented. The test structure consists of a straight photonic wire in layer-1 and dummy crossings with various numbers (0-91) of crossings in layer-2. Figure 7.11 shows the test structures used to demonstrate the double layer photonic integrated circuit.

7.4.2 Fabrication of double layer photonic circuit

A double layer photonic circuit was fabricated on a 200 mm SOI wafer. The first photonic layer was defined in crystalline Si and the second layer was defined in deposited $\alpha - Si : H$. Figure 7.12 illustrates the fabrication steps involved in

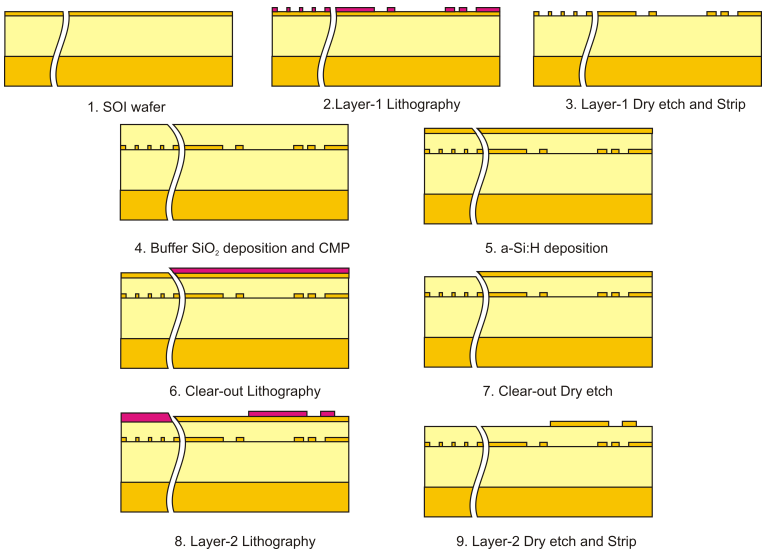
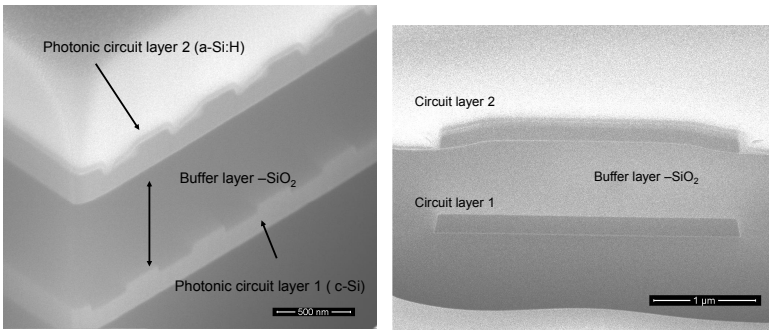


Figure 7.12: Fabrication process overview of a double layer photonic circuit.

realizing a double layer photonic integrated circuit. Firstly, the circuit patterns of layer-1 are defined in crystalline Si Step-2 and -3 are repeated to define waveguides (220 nm), and shallowly etched (70 nm) gratings for via and fiber-chip couplers. Following layer-1 definition, 1050 nm of isolating SiO_2 was deposited using a high density plasma chemcial vapour deposition technique (Fig. 7.12 step-4). A short planarizing chemical mechanical polishing (CMP) is applied on SiO_2 to remove topography. During this process ≈50 nm of SiO_2 is consumed resulting in an isolation of 1000 nm. After CMP, 220 nm of $\alpha - Si : H$ was deposited as a second photonic layer, layer-2. As mentioned earlier, alignment between circuit layers is critical in multilayer circuits. Hence, in order to reduce alignment errors, the $\alpha - Si : H$ in layer-2 is cleared on top of the alignment structures as shown in figure 7.12 step-6 and -7. After exposing the alignment structures in layer-1, layer-2 circuits are aligned and fabricated. Similar to layer-1, both shallow-etched gratings and fiber-chip couplers, and deep etch waveguides and crossings were defined in layer-2 by repeating step-8 and -9. Figure 7.13 shows the cross-section scanning electron micrography of a fabricated grating via and waveguide crossing.

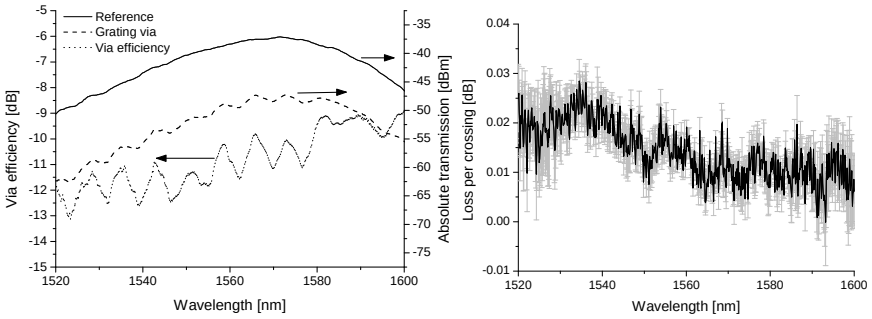
7.4.3 Optical characterization of double layer photonic circuits

The fabricated devices were characterized by coupling light from a broad-band light source into layer-1 and the output light from layer-2 is measured by a spectrum analyser. Figure 7.14a shows the transmission spectrum through a single GV. The efficiency of the GV is calculated by normalizing the via spectrum with a straight waveguide without a GV. With a simple design, we have achieved a



(a) (b)

Figure 7.13: Cross-section micrograph of (a) grating via and (b) crossing from a double layer photonic integrated circuit.



(a) (b)

Figure 7.14: (b) Measured transmission spectrum and efficiency of a single grating via and (b) Crossing loss in a double layer photonic circuit.

coupling efficiency of 11 % with 1- and 3-dB bandwidth of 22 and 38 nm respectively. The measured efficiency closely matches the simulated efficiency (13 %) of the fabricated circuit with the refractive index mismatch between the layers (Fig. 7.7b). Due to this mismatch, the radiation loss in the Via alone was ≈3 dB. The misaligned GVs did not show any degradation in the coupling efficiency, which demonstrates good alignment tolerance of the GVs.

The loss due to crossings in-between the photonic layers was measured from the transmitted power through a series of straight photonic wires in the first (bottom) photonic layer with a different number of crossings on the second layer. After measuring the transmission through photonic wires with 4 to 91 crossings, the linear regression shows a crossing loss of ≈0.013dB/crossing (Fig.7.14b). The achieved crossing loss is an order of magnitude lower than the inplane waveguide crossing loss [10].

7.5 High Efficiency Grating Fiber Coupler

Grating couplers are an attractive solution for coupling light from an optical fiber to a nanophotonic waveguide [8, 11]. A shallow etch grating fiber coupler diffracts light both upward (to fiber) and downwards (to substrate). The coupling efficiency to a fiber can be increased by reflecting the downward diffracting using a mirror. The mirror can be a metal layer or a Bragg mirror. Using gold as a bottom mirror an efficiency of 69 $\%$ was demonstrated for a 10 $\times$ 10 μm grating coupler [12]. This process involves bonding and substrate removal, which is complex and expensive, and since gold is being used, this process is not CMOS-compatible.

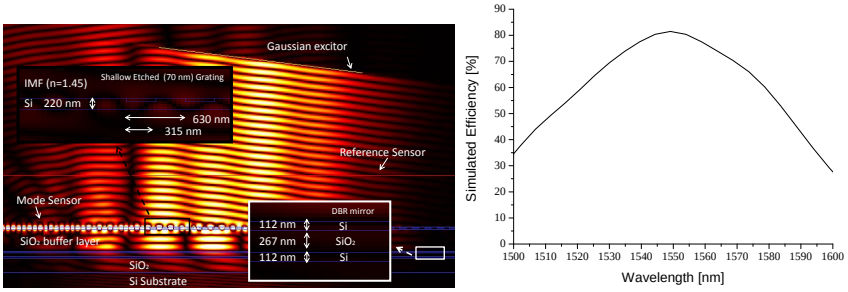
An alternative and simple approach is to reflect back the downward diffracted light with a Bragg mirror, which can be CMOS compatible. By depositing layers of high and low refractive index materials, such as Si and SiO_2 a Bragg mirror can be made over a complete wafer. On top of the mirror, photonic circuits including fiber couplers can be defined in a low-loss $\alpha - Si : H$.

7.5.1 Design of high efficient fiber coupler with bottom mirror

The coupling structure was optimised with a particle swarm optimization algorithm for a silicon waveguide core thickness of 220nm. The field profile of the optimal design is shown in figure 7.15a generated by a finite difference time domain (FDTD) simulation. The period of the grating is 630nm with a duty cycle of 50 $\%$ and the etch depth is 70nm. The number of grating periods is 25. For a buffer thickness of 1.44 μm, the reflected light from the Bragg mirror interferes constructively. The Bragg mirror is defined by two pairs of Si and SiO_2 with 112 nm and 267 nm respectively. The fiber is tilted under an angle of 10^o to avoid a large second order reflection. For this angle, the optimal waveguide width of the grating is 15m. The refractive index of the surrounding medium is 1.45, which corresponds to SiO_2 or Index Matching Fluid (IMF). Theoretically, the coupling efficiency is 82$\%$ for TE polarized light at 1550nm (Fig. 7.15b) with a bandwidth of 45 and 90 nm for 1- and 3-dB respectively. The simulation and optimization was carried out by D. Vermeulen.

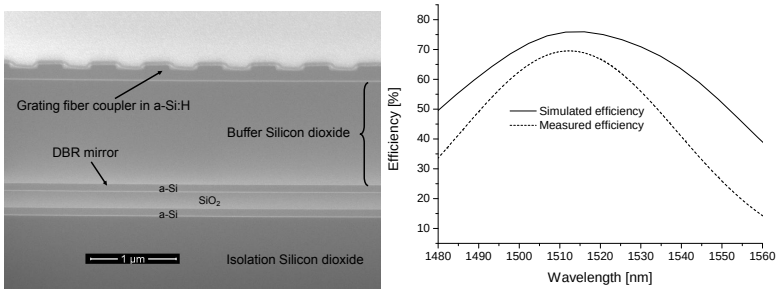
7.5.2 Fabrication of fiber couplers with bottom mirror

The grating fiber couplers with a bottom mirror were fabricated on a 200mm Si wafer. First a 1 μm SiO_2 isolation layer was deposited on a bare Si wafer. Then the Bragg mirror was defined by successive deposition of a 112 nm layer of $a-Si$ and a 267 nm layer of SiO_2. The $a - Si$ was deposited using the low pressure chemical vapour deposition process (LPCVD) and the SiO_2 was deposited by high-density plasma chemical vapour depositon (HDP). On top of the Bragg mirror, 1.48 μm of buffer SiO_2 was deposited, followed by a CMP process for planarization, which resulted in a final thickness of 1.44 μm. After CMP, 220 nm of low-loss $\alpha - Si : H$ layer was deposited [13]. The grating couplers and waveguides were fabricated using 193nm optical lithography and dry etching [14].



(a) (b)

Figure 7.15: FDTD simulation Results of a grating fiber coupler with a Bragg mirror (a) Field profile and (b) Coupling efficiency for the optimised structure.[courtesy D. Vermeulen]



(a) (b)

Figure 7.16: (a) Cross-section scanning electron micrograph of one of the fabricated grating fiber coupler with Bragg bottom mirror and (b) Measured and simulated coupling efficiency of the realized structure.

Figure 7.16a shows the cross-section scanning electron micrograph of one of the fabricated grating fiber couplers with Bragg bottom mirror.

7.5.3 Optical characterization of fiber couplers

The coupling efficiency was characterized with a fiber-to-fiber measurement. The test structures consist of identical input and output gratings couplers connected by a waveguide. Fiber-to-fiber transmission was measured by launching light into the input coupler from a single mode fiber connected to a broadband light source (SLED) and the light from the output coupler is captured by another single mode fiber connected to a spectrum analyser. The input and output fiber were positioned at an angle of 10^o to the sample normal and index matching fluid was applied between the optical fiber facet and the fiber coupler to avoid reflections at the fiber

facets. The measured coupling efficiency is 69.5 $\%$ for a single grating coupler with a 1dB-bandwidth of 36 nm and a 3 dB-bandwidth of 63 nm (Fig. 7.16b). The simulated efficiency for the actually fabricated device is 76 $\%$ as shown in figure 7.16b. The non-optimal waveguide width of 10 μm explains 5 $\%$ of the difference in coupling efficiency between measurement and simulation.

7.6 Conclusion

In this chapter, we presented optical via schemes for multilayer photonic circuits and demonstrated a double layer photonic circuit. Three optical via schemes directional coupler, grating via and multimode interference via were designed for coupling light from one photonic layer to other. From simulations, we found that the directional coupler via and multimode interference via yield high efficiency. Since the directional coupler via cannot be used for high density multilayer circuits due to layer-to-layer crossing loss, the multimode interference via is considered as the most viable via scheme. However, from fabrication point of view, grating couplers are simpler to implement than a multimode interference via. We have demonstrated a via efficiency of 11 $\%$ for a grating via coupling a crystalline Si bottom layer and amorphous Si top layer in a double layer photonic circuit. The coupling efficiency can be improved by using a using the same material for both the layer, for instance, amorphous silicon or by separately optimising the vias on the different layer.

In addition, by taking advantage of the layer deposition, we have also demonstrated high efficiency grating fiber-chip coupler by using bottom DBR mirror. We have demonstrated a coupling efficiency of 69.5 $\%$, which is twice that of a standard grating fiber-chip coupler.

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8

Conclusions and future work

8.1 Conclusions

Silicon photonics is an attractive platform for integration photonics. High refractive index contrast, transparence to infrared wavelengths and above all compatibility with CMOS fabrication technology makes silicon photonics a formidable technology for photonic integrated circuit and electronic-photonic integration. This work addresses key challenges in silicon photonic integrated circuit fabrication technology; high resolution and volume CMOS compatible fabrication technology, and secondly an alternative high index contrast device platform for electronic-photonic integration.

We developed fabrication technology for silicon photonic circuits using 193 nm optical lithography and dry etching process in a 200 mm wafer scale fabrication facility. The optical lithography and dry etch process have been designed to deliver a non-uniformity of $\pm 1\%$ over a 200 mm wafer, for a 450 nm photonic wire this means that the waveguide width is with in ± 4.5 nm. In comparison to standard CMOS process uniformity of $\pm$5-10$\%$, the developed process shows substantial improvement. Using this process, we have demonstrated low-loss waveguides, with propagation loss as low as 1.36 dB/cm for a photonic wire of 450 nm, which is the lowest reported so far for this fabrication technology.

We have also studied the uniformity of the wavelength selective devices in addition to physical linewidth uniformity. We have found that the uniformity of the devices within a chip depends on the length scale, identical devices which are placed close showed less non-uniformity compared to millimetre spaced devices. Intra-die and inter-die measurements showed a standard deviation of <1 nm of

the resonance peak, while over a 200 mm wafer it was 1.5 nm. The effect of pattern/device density on the device uniformity was studied and we found that uniform distribution of pattern/devices yields better uniformity. Even so, optically isolated devices as far as 10 μm were found to affect the absolute dimension and response of a wavelength-selective device. This distance determines the limitation of the device density within a chip.

Since the traditional SOI is limited to a set of thickness, so we developed an advanced fabrication technology to accommodate different waveguide geometry. The developed process allows flexible thickness and cross-section of the waveguides within a circuit. Using this approach, we have demonstrated a high-efficiency fiber-chip grating coupler, which requires a silicon thickness of 380 nm to couple light into a 220 nm thick photonic wire. We have achieved a coupling efficiency of 70$\%$ with a 3dB bandwidth of 80 nm. With an optimised dry etch process, we were able to achieve a propagation loss of 1.77 dB/cm for a 450 nm wide photonic wire.

In this work, we have developed an alternative high refractive index material platform: amorphous and polycrystalline silicon for photonic integrated circuits. Polycrystalline silicon deposited using high temperature low pressure chemical vapour deposition process was found to the inherently highly lossy. However, by using optimised process sequence and forming gas anneal, we achieved a propagation loss of 13 dB/cm for a 500 nm wide photonic wire, which is one of the lowest reported for this cross-section. The loss is very high and makes it less attractive for low-loss application. Nevertheless, it can be used in applications where a high temperature process is required and has high loss penalty.

Amorphous silicon usually has high optical absorption in infra-red wavelengths. In this work, we engineered the low temperature plasma enhanced chemical vapour deposition process to yield a back-end compatible, low-loss waveguide material. Using this material, we demonstrated a propagation loss of 3.45 dB/cm for a photonic wire and 0.7 dB/cm as an estimated upper bound for material loss at 1550 nm. Various wavelength-selective devices fabricated in hydrogenated amorphous silicon showed comparable performance with similar devices in crystalline silicon. By exploiting the hydrogen content in the material, the refractive index of the material was trimmed by using post-fabrication thermal treatment. By combining thermo-optic property and trimming property, we found that the device can be either trimmed or tuned over a wavelength range of 24.6 nm. This technique can be used to compensate for fabrication inaccuracies. We have also found that the trimming can be achieved without inducing additional loss in the material. However, the maximum thermal limit for processing amorphous silicon is 400 ^{o}C above this temperature we have found that almost all the hydrogen is driven out result in a material with very large absorption loss.

Since hydrogenated amorphous silicon can be deposited as layer stacks, we have fabricated a double layer photonic circuit coupled through a grating optical via. By using a simple design, we have demonstrated a modest via efficiency of 11 $\%$.The ability to deposit multiple layer opens new interest in the multilayer photonic circuit which can increase the number of functionalities integrated in a

single chip.

8.2 Future work

One of the main goals in this work was to realize silicon photonic devices in a high volume CMOS manufacturing facility. Even though we have reached many of our targets, there is still scope for improvements and further exploration of some of the issues.

1. The propagation loss of the photonic wires could be still improved by using post-fabrication treatments. The post-fabrication treatments explored in this work can be applied to photonic wires fabricated with the optimal patterning process. Furthermore, the surface states and contamination on the waveguides should be studied to reduce the propagation loss further. Since the propagation loss strongly depends on the patterning process any process drifts can result in higher loss. Dedicated monitoring, mainly for dry etching process should be done periodically as a short loop test which can reduce process drifts.

2. The issue of non-uniformity still needs deeper study and understanding. In order to build sufficient statistics one should measure large set of devices, which is time consuming, laborious and can result in human errors. Implementing an automated measurement scheme can help to extract large data set quickly and reliably. With large data set, the underlying non-uniformities, both systematic and random can be distinguished with sufficient contrast. This will also help to discriminate various sources.

3. The effect of pattern density on the device non-uniformity should be explored further. Since the new design layout often contains density control structures the overall effect on individual devices can lead to design rule ratification.

4. The propagation loss of hydrogenated amorphous silicon can be further improved by exploring a wider parameter space of the deposition process. Hydrogenated amorphous silicon is an attractive material not only for its low-loss and flexible property. There are recent studies showing better nonlinear properties compared to other material platforms. The nonlinear properties can be exploited for optical functions such as wavelength conversion, amplification and modulation. Since this material is CMOS compatible and can be deposited on a variety of substrates it have many advantages compared to conventional nonlinear materials. A better understanding the origin of the nonlinear process in this material could help for material engineering.

5. The propagation loss of polycrystalline silicon can be improved by using 193 nm optical lithography and dry etch process. Active devices, such as

high speed modulation can be readily fabricated in polycrystalline silicon, which has a low carrier lifetime compared to crystalline silicon.

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A
Publications

A.0.1 Publications in international journals

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A.0.4 Highlights and Awards.

1. **Silicon photonics: Mass CMOS production**, Research highlight in Nature Photonics, Vol.4, p. 7, 2010.

2. SPIE best paper award at photonics 2009.

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B

Lithography simulation parameters

lithography Simulation Settings in PROLITH

PROLITH

trench_AR237J_AC29

PROLITH--trench_AR237J_AC29

Wafer Processes
- Process 5: ArF JSR AR237J (resist)
  - Thickness (nm): 330
- Process 4: Brewer ARC 29A (layer)
  - Thickness (nm): 77
  - Refractive Index (real): 1.82
  - Refractive Index (Imaginary): 0.34
- Process 3: Silicon (layer)
  - Thickness (nm): 220
  - Refractive Index (real): 0.883143
  - Refractive Index (Imaginary): 2.77779
- Process 2: Si Dioxide (layer)
  - Thickness (nm): 2000
  - Refractive Index (real): 1.56312
  - Refractive Index (Imaginary): 0
- Process 1: Silicon (substrate)
  - Refractive Index (real): 0.883143
  - Refractive Index (Imaginary): 2.77779

Resist

Type	Positive Chemically Ampli
Material	ArF JSR AR237J
Vendor	JSR
User Defined	Yes
Developer	User Defined
Thickness (nm)	330
Abs. Parameter A (1/um)	0
Abs. Parameter B (1/um)	1.1
Rate Constant C (cm2/mJ)	0.0455
Unexposed Refractive Index (real)	1.7135
Exposed Refractive Index (real)	1.7135
Refractive Index Change on Expose	0
Thermal Decomposition Activation E	0
Thermal Decomposition Ln(Ar) (1/se	-20
PEB Acid Diffusivity Activation Ener	19.65
PEB Acid Diffusivity Ln(Ar) (nm2/se	26.563
PEB Base Diffusivity Activation Ener	0
PEB Base Diffusivity Ln(Ar) (nm2/se	-20
Amplification Reaction Order	1
Amplification Reaction Activation En	19.657
Amplification Reaction Ln(Ar) (1/sec	21.135
Diffusion-Controlled Reaction Activa	0
Diffusion-Controlled Reaction Ln(Ar)	20
Acid Evaporation Activation Energy	0
Acid Evaporation Ln(Ar) (1/sec)	-20
Bulk Acid Loss Activation Energy (k	0
Bulk Acid Loss Ln(Ar) (1/sec)	-20
Relative Quencher Concentration	0.162
Room Temperature Diffusion Lengt	0
PEB Acid Base Quenching Activatio	0
PEB Acid Base Quenching Ln(Ar) (1	20
Acid Diffusivity Variation	Constant
Base Diffusivity Variation	Constant
Development Rmax (nm/s)	100
Development Rmin (nm/s)	0.1
Development Mth	-100
Development n	3
Relative Surface Rate	0.6
Inhibition Depth (nm)	120

Coat and Prebake

Bake Model	Ideal
Time (sec)	0
Temperature (C)	130

Mask

Type	1D Parametric
Name	1D Binary Scattering Bar -
Rotate 90 degrees	No
Mask Simulation Mode	Kirchhoff
Background Intensity Transmittance	0
Background Phase (deg.)	0
Feature Width (nm)	180
Mask Pitch (nm)	2180
Number of Scattering Bars	2
Binary Scattering Bar Size (nm)	500
Binary Primary Scattering Bar Spac	500

Imaging Tool
- Source Shape
  - Name: Conventional--Partially Co
  - Gaussian: No
  - Partial Coherence: 0.85
- Oblique Incidence at Mask: No
- Illumination Spectrum
  - Name: Cymer XLA-300 ArF
  - Wavelength Range (nm): 1e-005
- Illumination Polarization: Unpolarized
- Immersion Enabled: No
- Wavelength (nm): 193
- Numerical Aperture: 0.63
- Reduction Ratio: 4
- Flare: 0.02
- Use Defocus With Wavelength: No

Exposure and Focus

Dose Calibration	Wafer Side
Dose Correctable	1
Focal position relative to	MIDDLE
Positive numbers shift	UP
Exposure (mJ/cm2)	23
Focus at Mask (um)	0
Focus (um)	0.05
Focal Averaging	No

Vibrations
- X/Y Vibration Model: None

Post Exposure Bake

Bake Model	Ideal
Time (sec)	90
Temperature (C)	130
Surface Contaminant Type	Base
Contaminant Surface Concentration	0.001
Surface Contaminant Diffusion Leng	50

Development

Developer	User Defined
Development Model	Original Mack Model
Develop Time (sec)	60

Numerics

Image Calculation Model	Vector
Type of Resist Model	Normal PROLITH Operati
Number of Exposure Passes	1
Source Grid Speed Factor	4
Speed Factor for XY Step	6
Speed Factor for Z Step	4
Source Grid step size	0.05
X step size (nm)	9
Z step size (nm)	3.3

Metrology
- Simulation Region
  - Top: 0
  - Right: 450
  - Bottom: 0
  - Left: -450
- Litho Metrology
  - CD Measurement: Standard
  - CD Threshold Type: Relative
  - Measurement Height (%): 50

PROLITH

trench_AR237J_AC29

CD Measurement Offset (nm)	0	Sidewall Angle Specification (deg.)	80
Critical Shape Error	Not Calculated	Resist Loss Specification (%)	10
Aerial Image Intensity Threshold	0.5	Exposure Latitude Spec for DOF (	10
Image In Resist Intensity Threshol	0.5	Process Window Constraint	None
Exposed Latent Image PAC Thres	0.5	Standard Planes	
Latent Image PAC/Blocking Thres	0.5	Y	
Analysis		Plane Position (nm)	0.00
Profile Analysis Side	Average	Start Position (nm)	-450.00
Process Window Measurement	Rectangle	End Position (nm)	450.00
HD Contrast Upper Threshold (%)	70	Litho Target CD (nm)	180.00
HD Contrast Lower Threshold (%)	20	Aerial Image Tone	Space
Linewidth Specification (%)	10		

C

Etch rate comparison

Etch depth comparison

Figure C.1 and C.2 depict the cross-section scanning electron microscope image of dry etch done on polycrystalline and crystalline silicon respectively. The dry etch was done using same etch recipe and mask. The etch characterization shows that there is no observable difference in the etch depth beyond the resolution of the characterization tool. This confirms that process developed using polycrystalline silicon can be used on crystalline silicon without any uncertainty in etch rates.

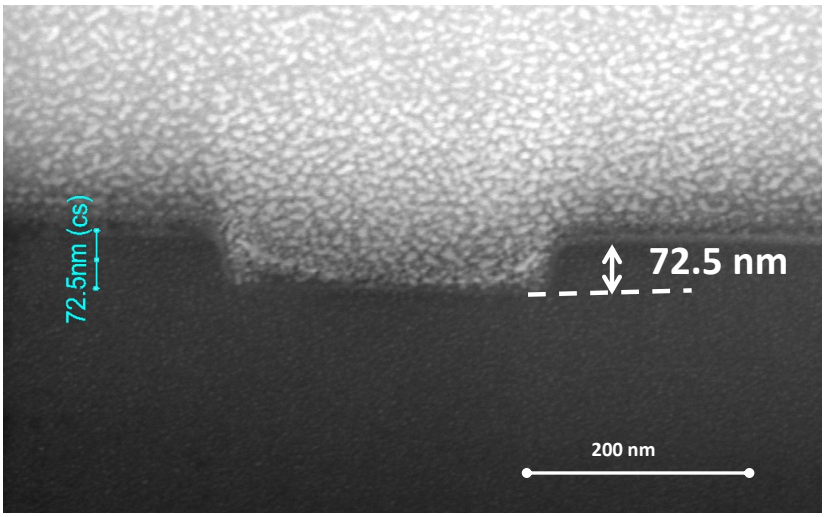

Figure C.1: Cross-section scanning electron microscope image of 70 nm etch in Polycrystalline silicon.

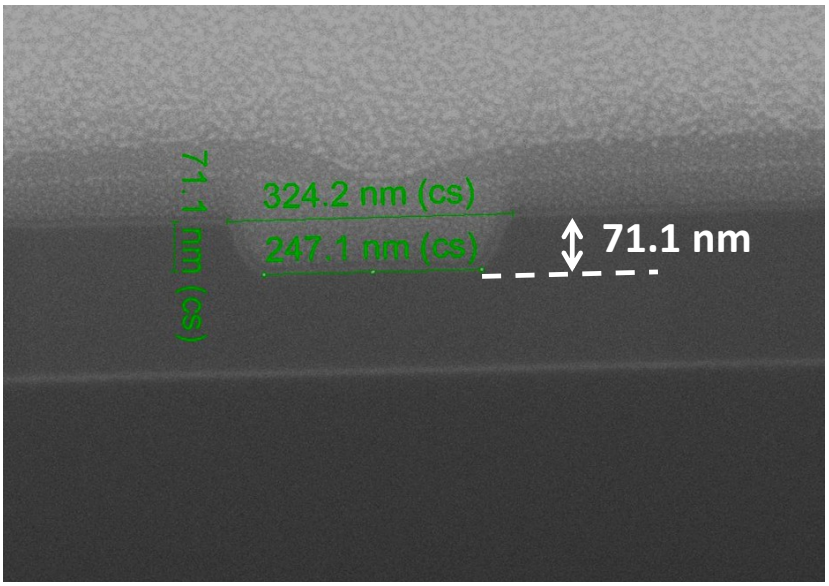

Figure C.2: Cross-section scanning electron microscope image of 70 nm etch in crystalline silicon.

D

Photonic wire loss summary

Photonic wire loss summary

Table D.1 summarizes propagation loss of some of the photonic wires fabricated during the course of this research work.

Resist process

A- $1 - AC29 - 77 - AR1682J - 330$

Etch process

A- $ZJW - PM1 - PICMOS - P060119 - D04$
B- $ZSS - PM1 - P090086 - D02$
C- $ZSS - PM1 - APWG220NM$
D- $ZSS - PM1 - WG220NM$
E- $ZSS - PM1 - APWG220NM - P2$

Strip process

V- $STDSTRIP/SPMAPM$
W-$POLYEPTEST4/POWETONL$
X-$POLYEPTEST4/LONGPOWE$

Layer ID	Lot/wafer ID	etch recipe	Strip	Wire width	Loss	Clad
A11	X060008-D14	A	V	450	2.85 $\pm$ 0.067	Air
	X060008-D14	A	V	470	2.73 $\pm$ 0.095	Air
	X060008-D15	A	V	450	4.65 $\pm$ 0.65	Oxide
	X060008-D15	A	V	470	4.58 $\pm$ 0.659	Oxide
Homer	P090086-D02	B	X	406	4.18 $\pm$ 0.12	Air
	P090086-D02	B	X	440	4.51 $\pm$ 0.13	Air
	P090086-D03	B	X	406	2.88 $\pm$ 0.25	Air
	P090086-D04	B	X	450	3.18 $\pm$ 0.05	Air
	P090086-D07	C	X	450	1.72 $\pm$ 0.05	Oxide
	P090086-D07	C	X	436	1.77 $\pm$ 0.05	Oxide
	P090086-D07	C	X	406	2.07 $\pm$ 0.05	Oxide
Test2	P090100-D02	D	V	480	4.57 $\pm$ 0.02	Air
Test2	P090100-D03	D	W	470	4.34 $\pm$ 0.02	Air
Test2	P090100-D04	D	X	500	4.16 $\pm$ 0.06	Air
HANGOVER	P100118-D03	E	X	500	2.41 $\pm$ 0.06	Air
	P100118-D03	E	X	500	2.4 $\pm$ 0.02	Air
SWORD	P100144-D07	E	X	500	2.5 $\pm$ 0.03	Air
	P100144-D07	E	X	500	2.46 $\pm$ 0.03	Air
SHAWSHANK	P100198-02	E	Z	490	2.38 $\pm$0.1	Air
WG-DF	P100016-D02	E	X	450	2.14 $\pm$ 0.03	Air
WG-DF	P100016-D03	E	X	500	1.86 $\pm$ 0.01	Air
GOLLUM	P100198-D07	E	X	450	1.35 $\pm$ 0.06	Oxide
TEST 2	P090100-D19	E	X	500	3.21 $\pm$ 0.09	Air

Table D.1: Photonic wire loss history.