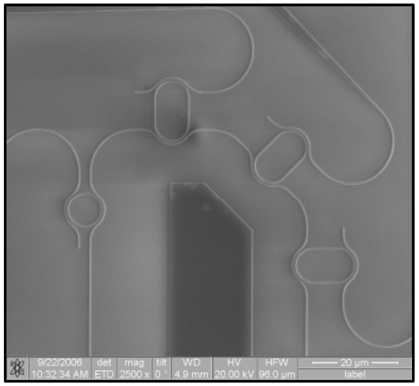
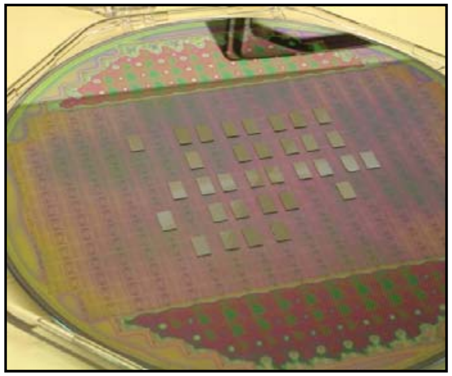
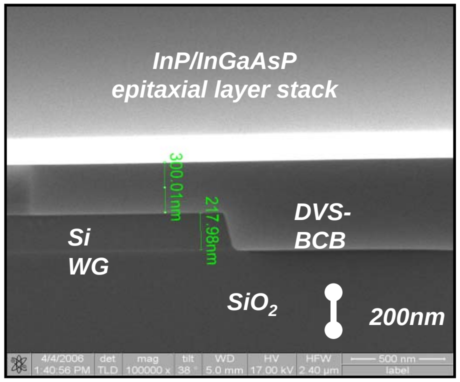
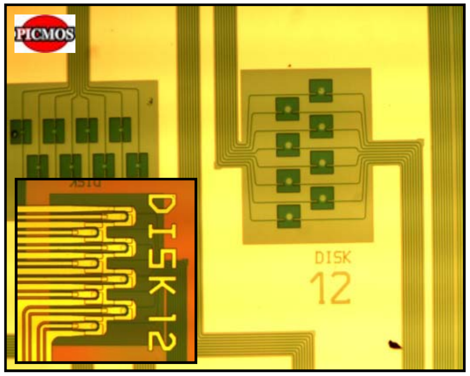
III-V silicon heterogeneous integration

Dries Van Thourhout – IPRM '08, Paris









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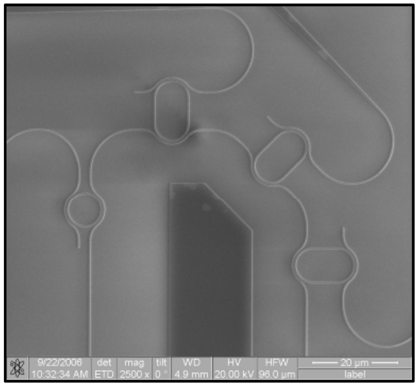

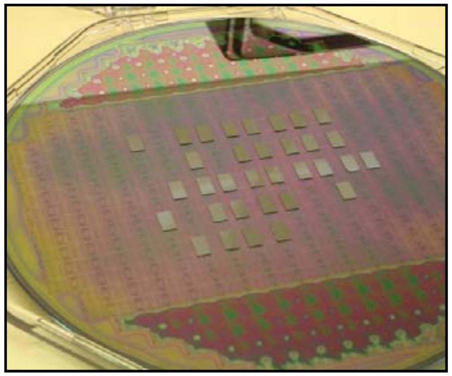

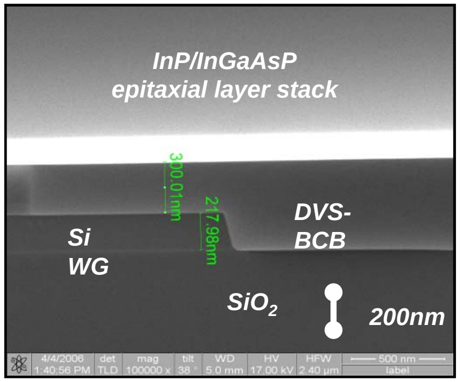

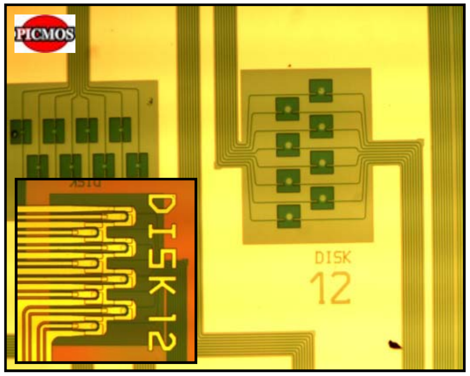

1. Silicon photonics is great !!!

2. But we still need InP

3. III-V silicon integration

4. Devices

Acknowledgements

Photonics Research Group

- III-V silicon integration:
  - G. Roelkens, J. Van Campenhout, J. Brouckaert, L. Liu
- Silicon Processing
  - W. Bogaerts, P. Dumon, S. Selvarajan, R. Baets

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- R. Notzel, X.J.M. Leijtens (TU/e) (epitaxy)
- C. Lagahe, B. Aspar (TRACIT) (planarization)

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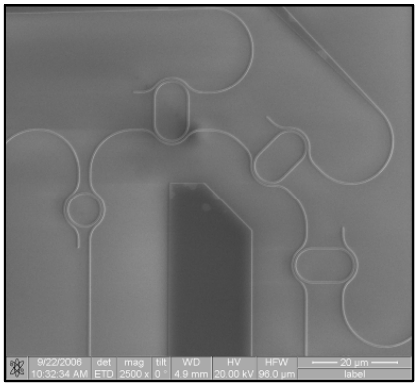
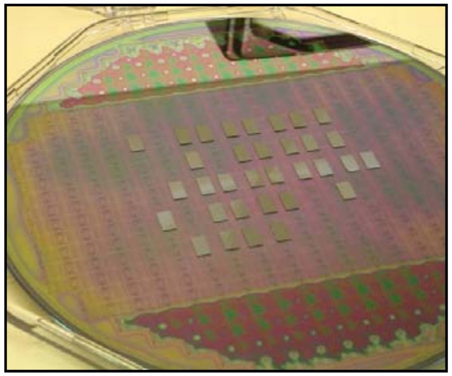
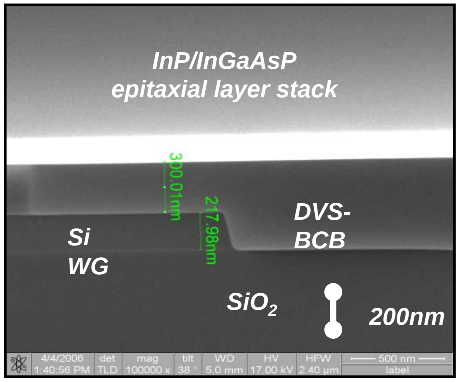
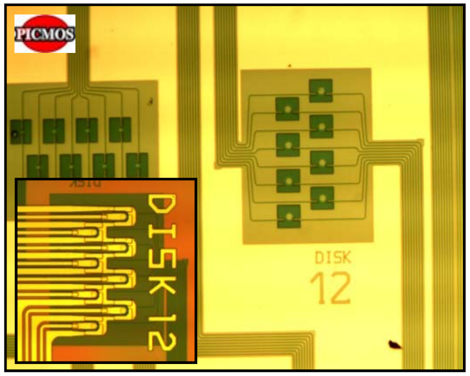
imec
aspire invent achieve

III-V silicon heterogeneous integration









1. Silicon photonics is great !!!

2. But we still need InP

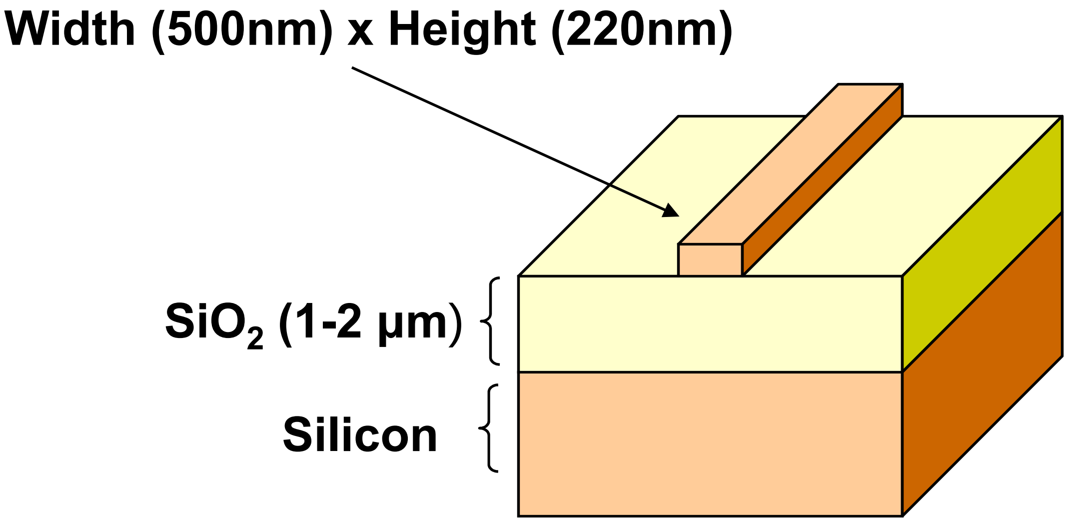
3. III-V silicon integration

4. Devices

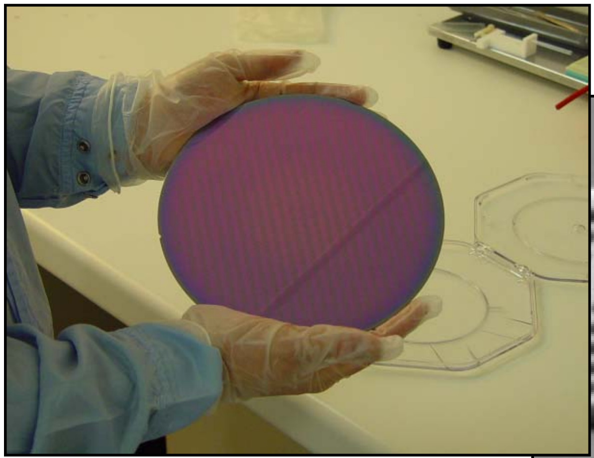
blems?

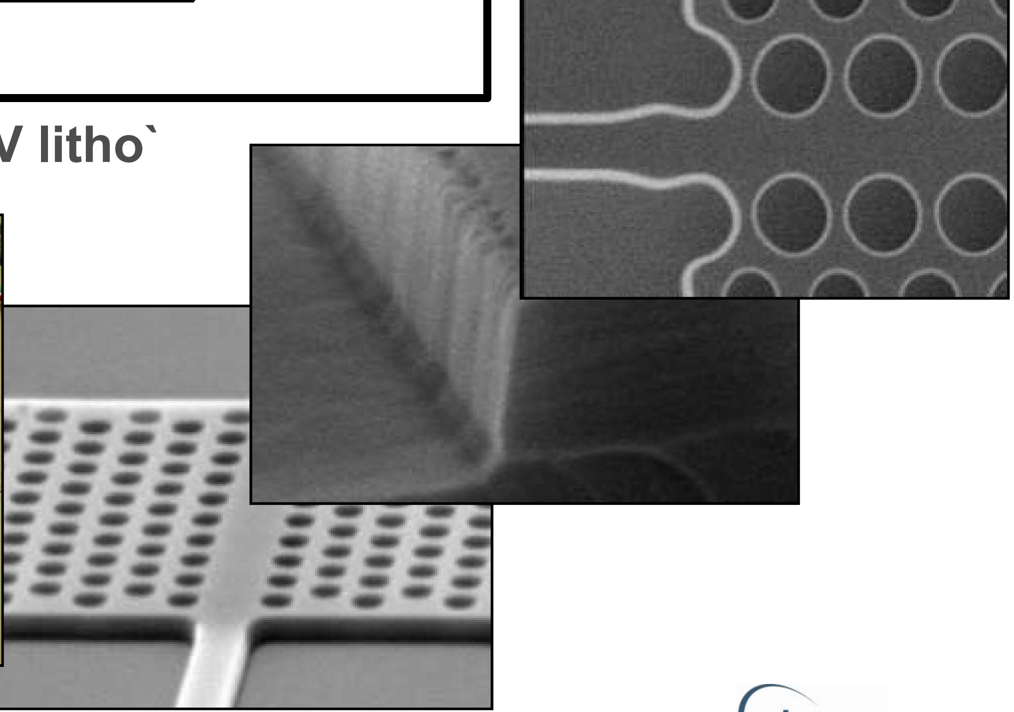
m, 1.55 µm)

pact circuits



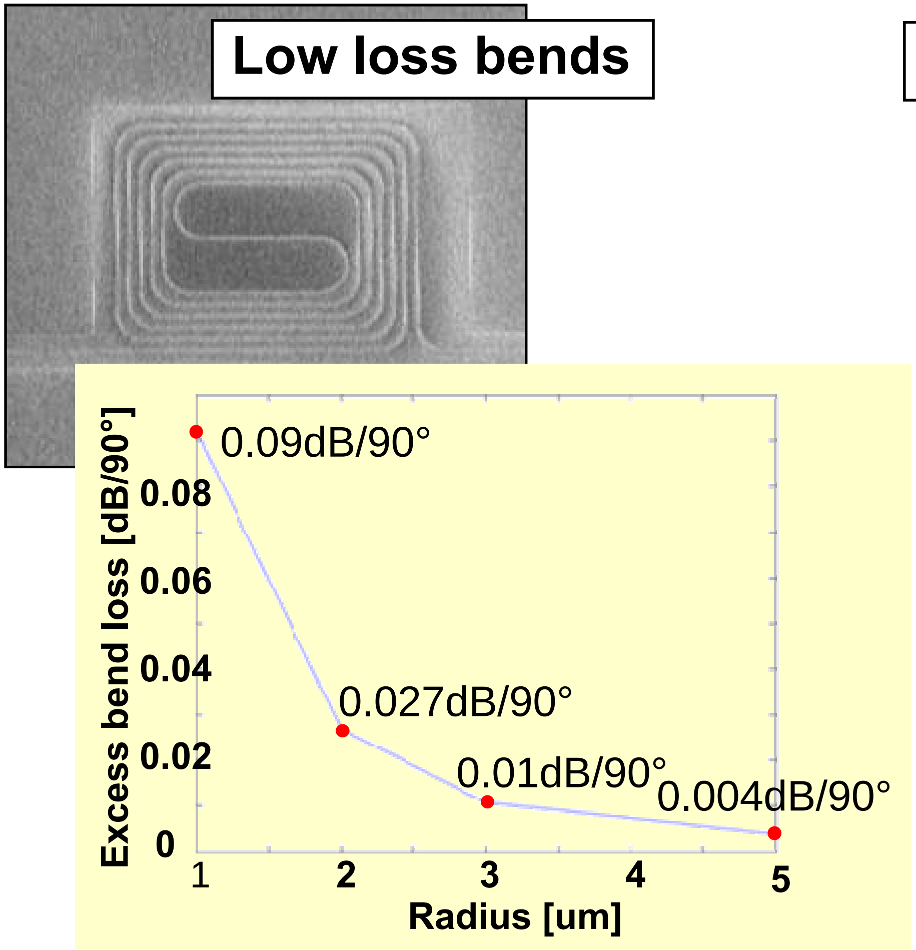
- Pattern definition: DUV litho`



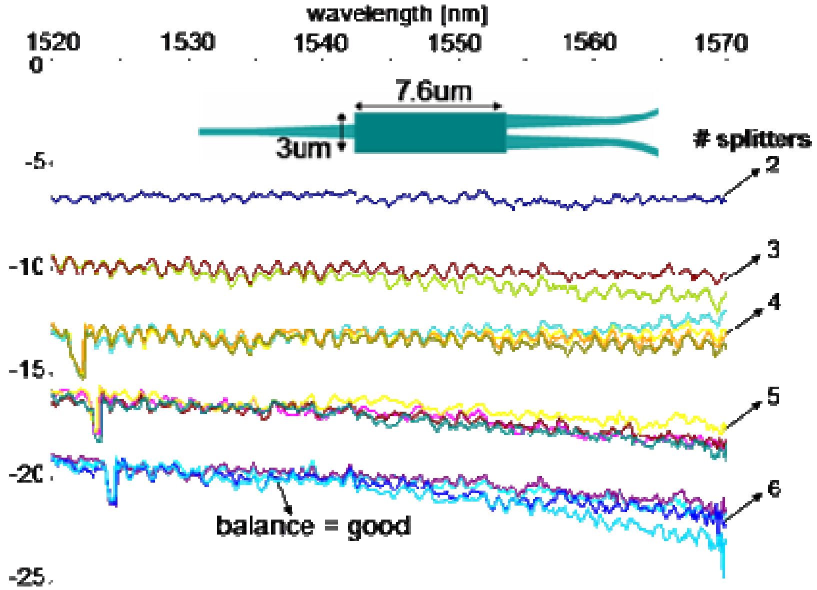


Photonic wiring

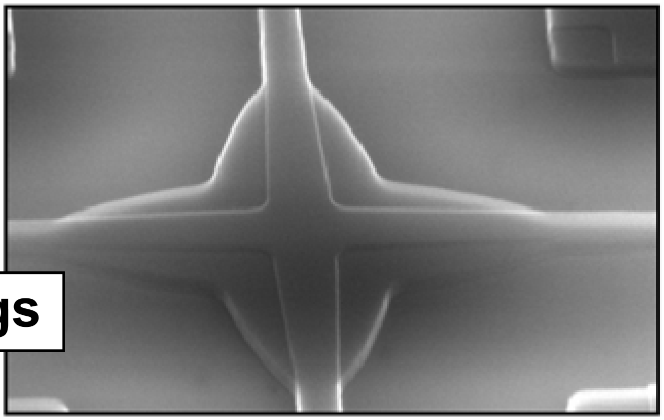
Low loss bends



<0.3dB excess loss for splitters

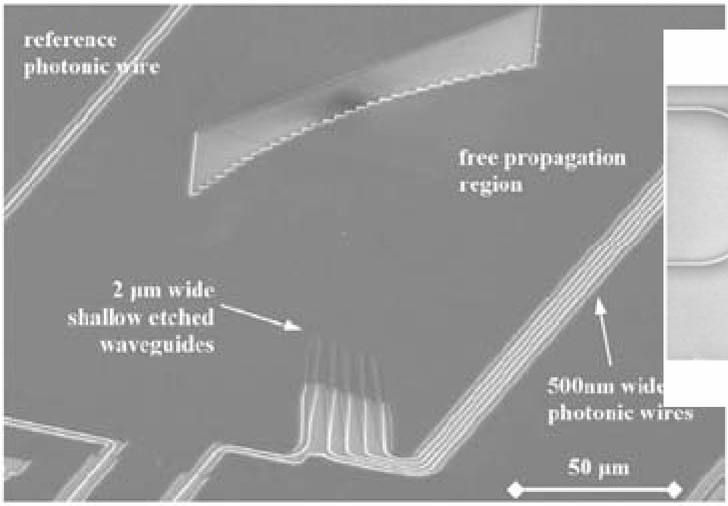


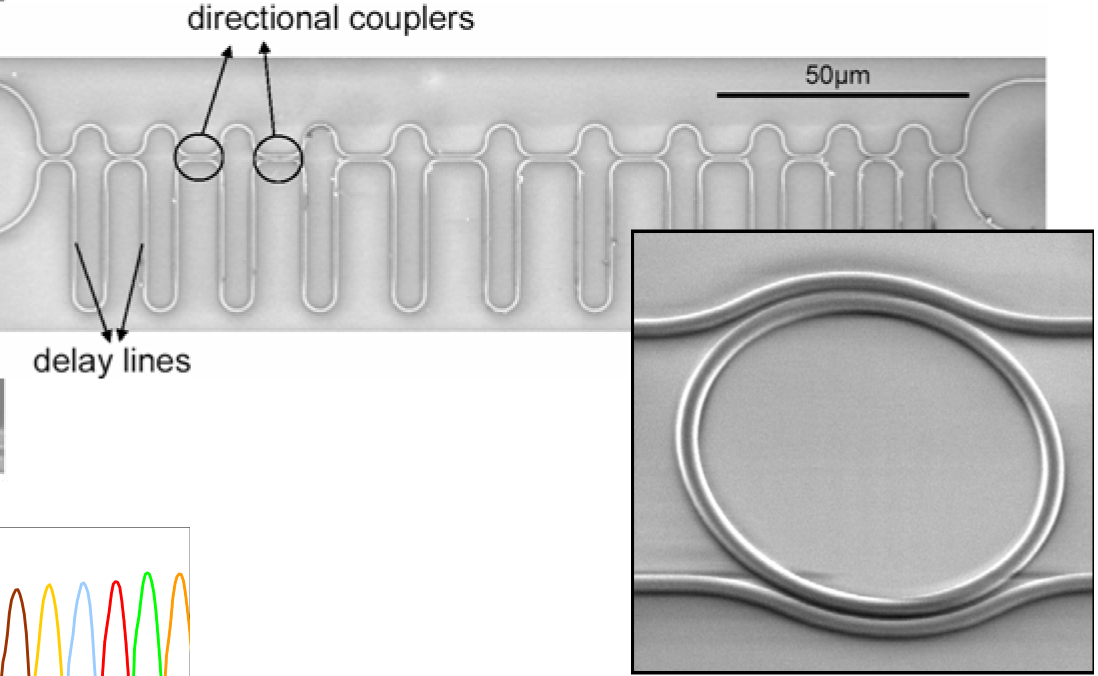
97% transmission in crossings

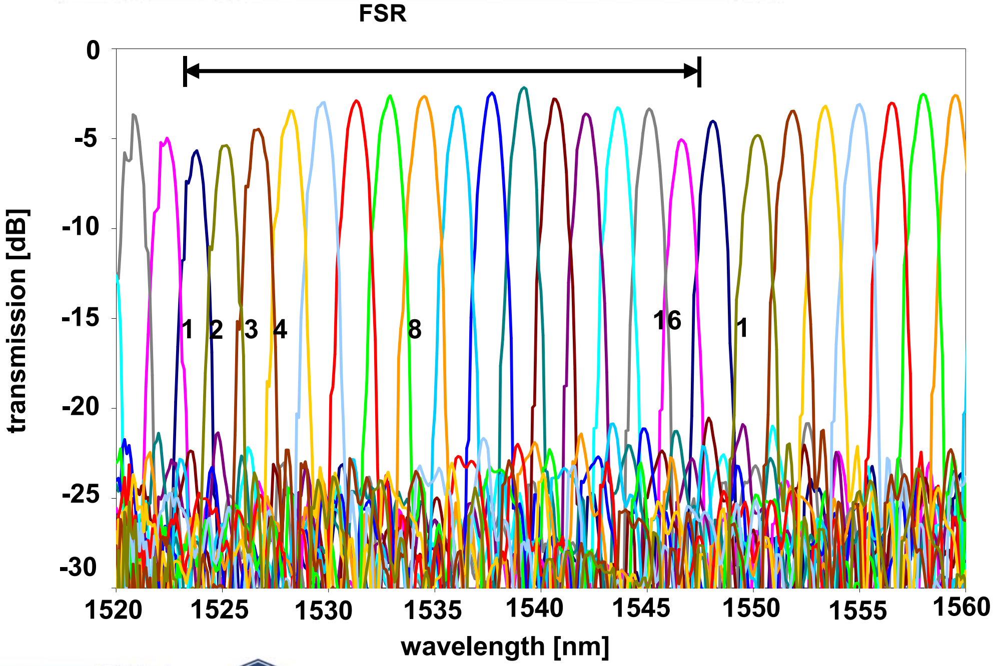


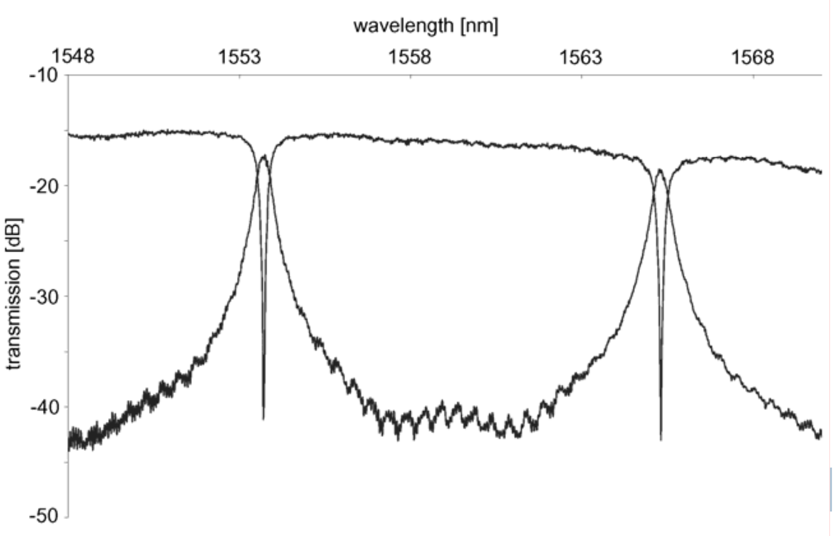
(b)

Wavelength dependent devices

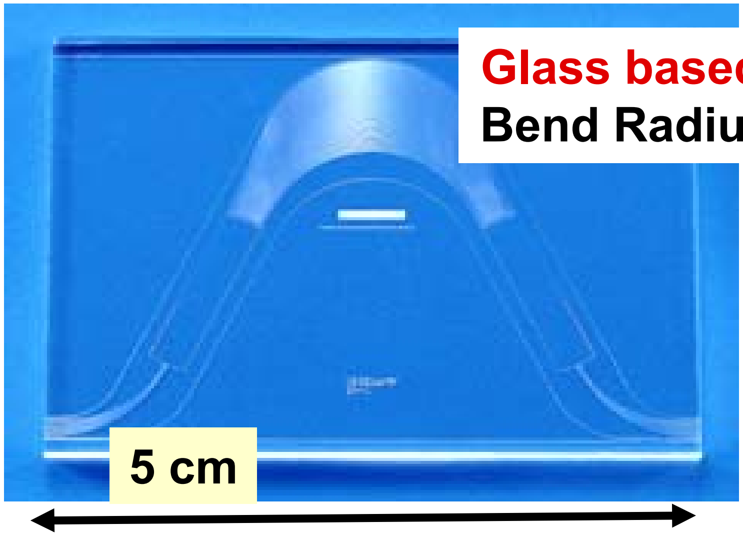




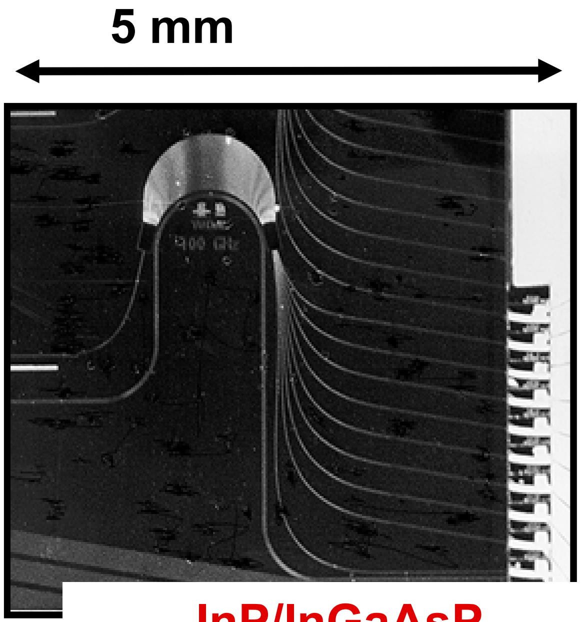




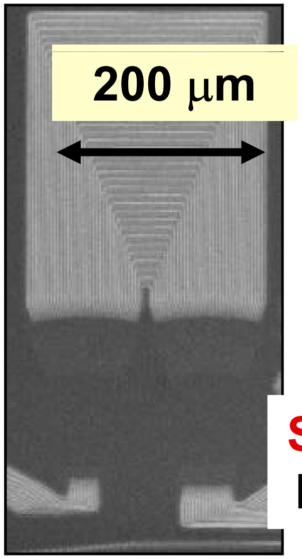
Increasing Index Contrast



Glass based devices
Bend Radius ~ 5 mm

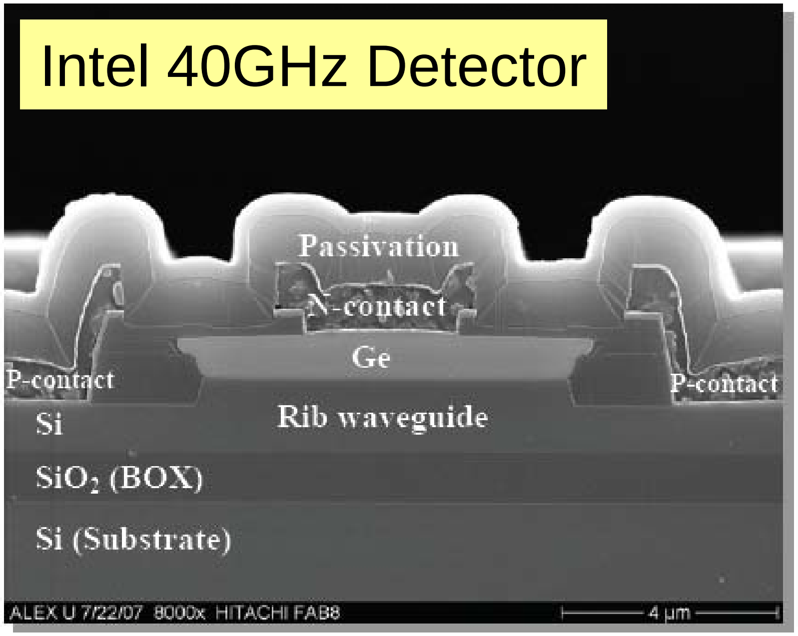


InP/InGaAsP
(bend radius ~ 500um)

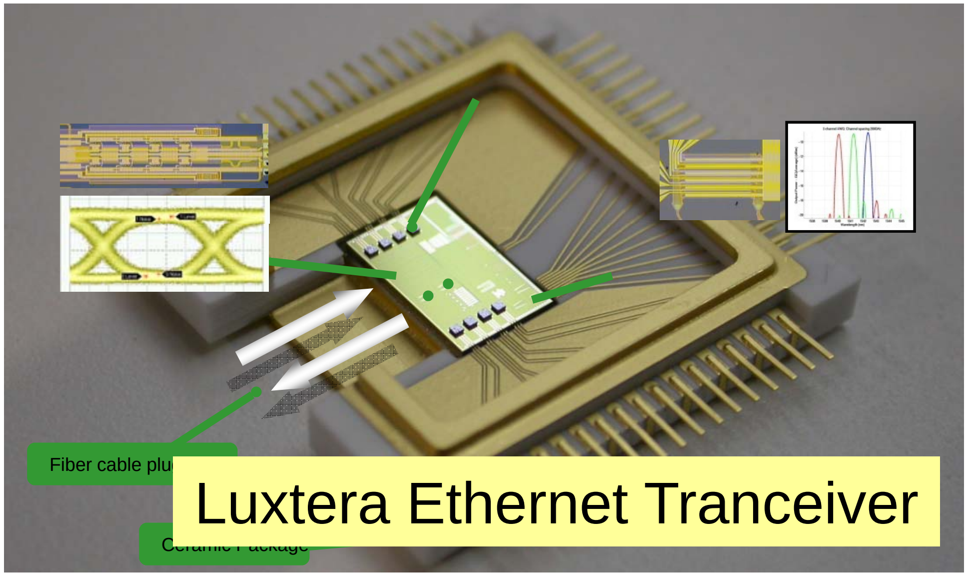


Silicon photonic ICs
Bend Radius < 5µm

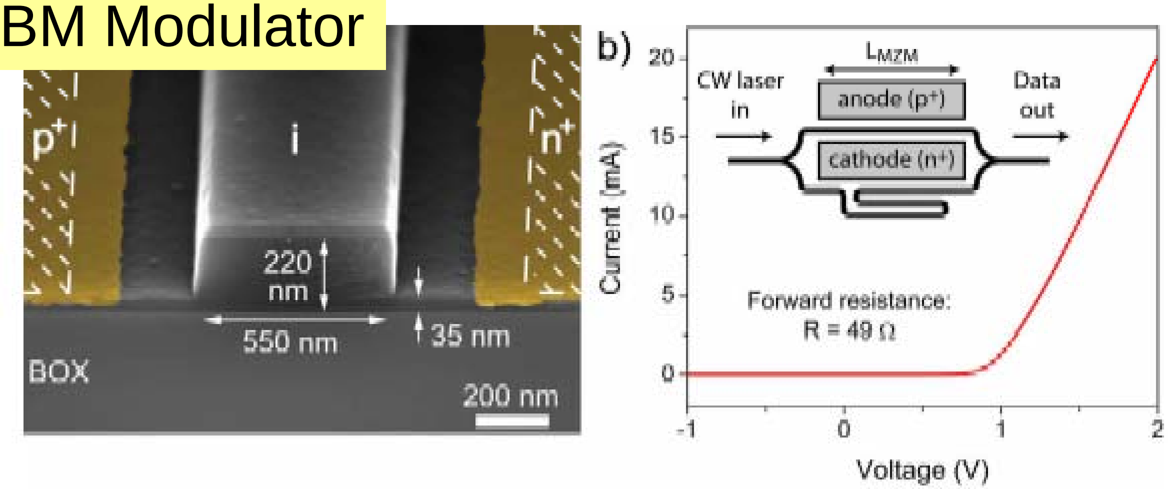
Silicon Photonics



Intel 40GHz Detector



Luxtera Ethernet Tranceiver

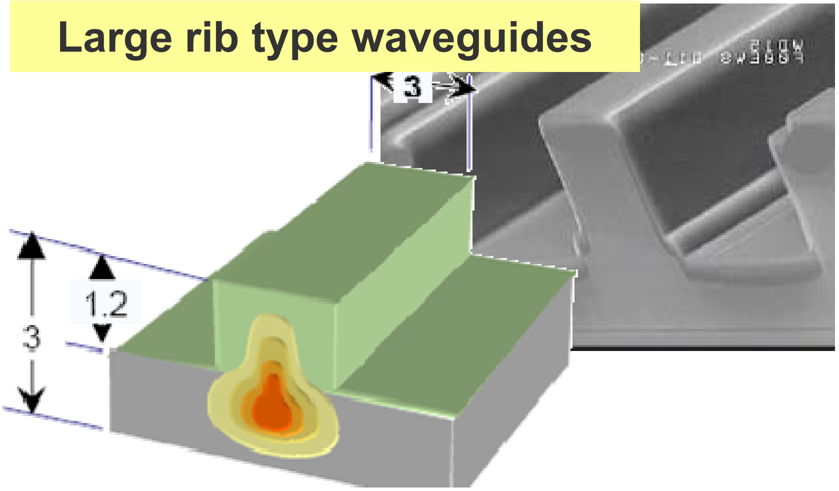


IBM Modulator

Silicon Photonics

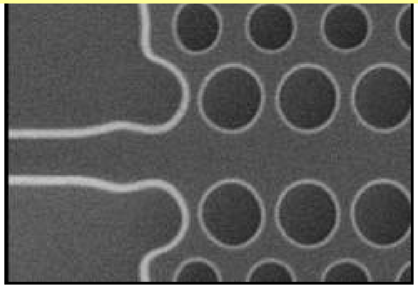
Silicon photonics comes in many flavors …

Large rib type waveguides



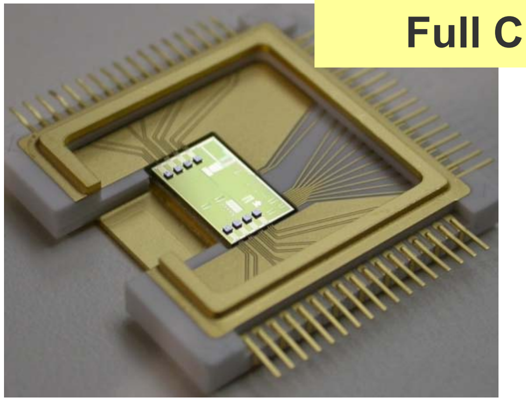
- Easy coupling with fiber
- Large device size
- e.g. www.kotura.com

Small core devices



- Optimized for nanophotonics
- Small device size
- This work and many others

Full CMOS integration



- Fabricated in CMOS process
- Directly integrated with electronics
- e.g. www.luxtera.com

III-V on silicon ?

Silicon photonics gives us:

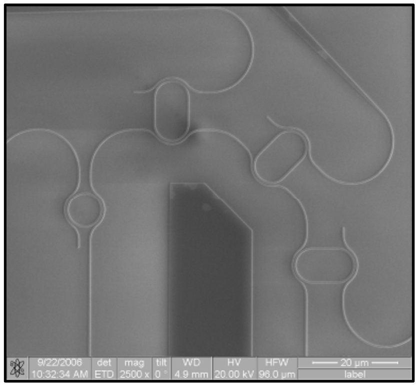
- Excellent passives
- Fast modulators, fast photodetectors
- But: (almost) no light …

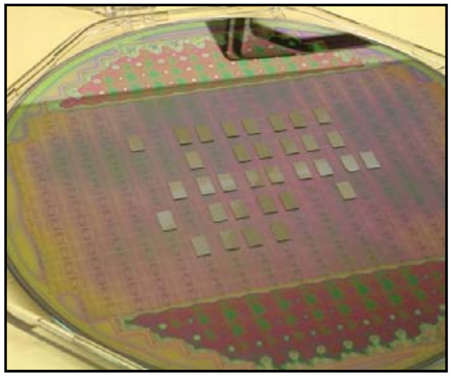
➔ **Need for integration with III-Vs**

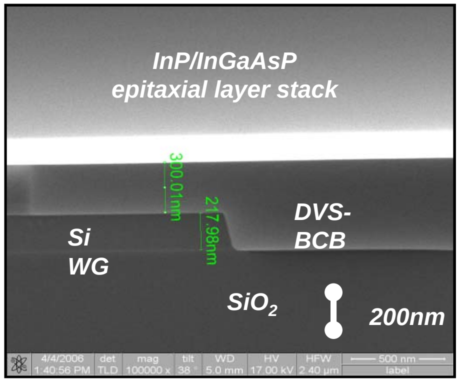
Requirements

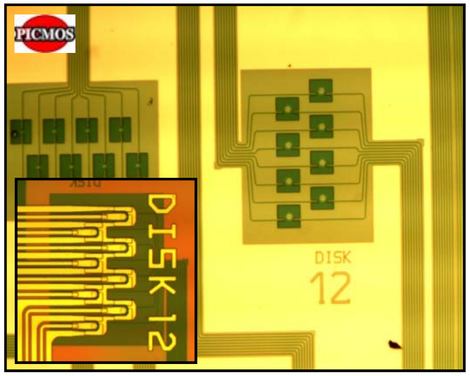
- High density (~10-20um device pitch)
- High alignment accuracy (~100nm)
- Waferscale processes

III-V silicon heterogeneous integration









1. Silicon photonics is great !!!

2. But we still need InP

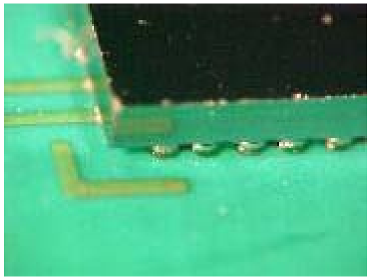
3. III-V silicon integration

4. Devices

III-V on silicon

There are several ways to integrate III-V on SOI

- Flip-chip integration of opto-electronic components



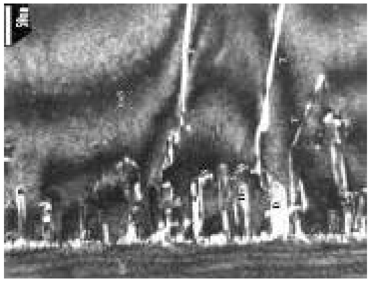
☺ most rugged technology

☺ testing of opto-electronic components in advance

☹ slow sequential process (alignment accuracy)

☹ low density of integration

- Hetero-epitaxial growth of III-V on silicon



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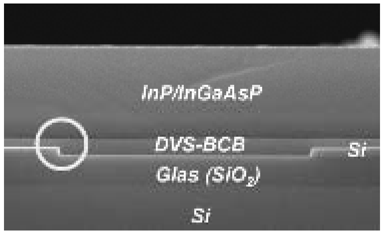
See other talks at this conference

- Bonding of III-V epitaxial layers



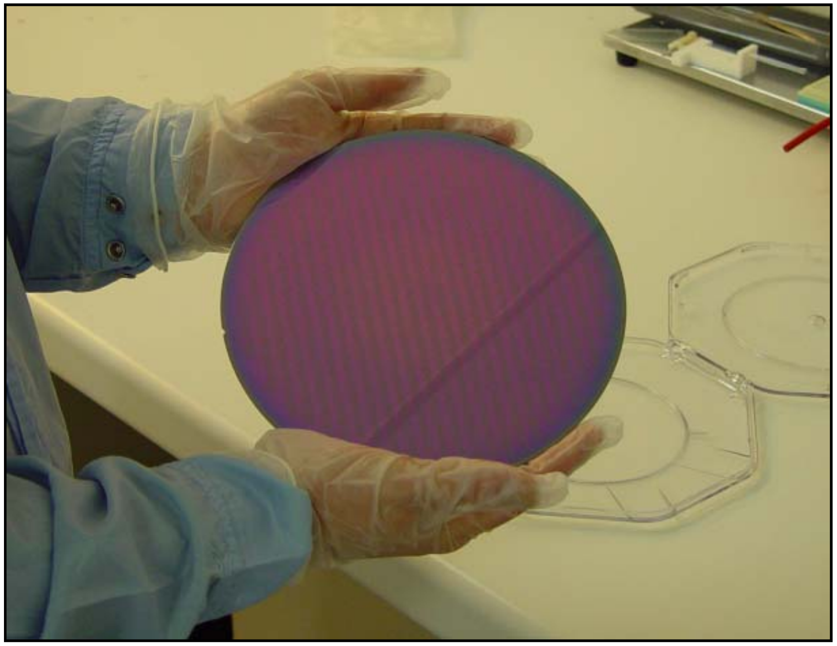
☺ sequential but fast integration process

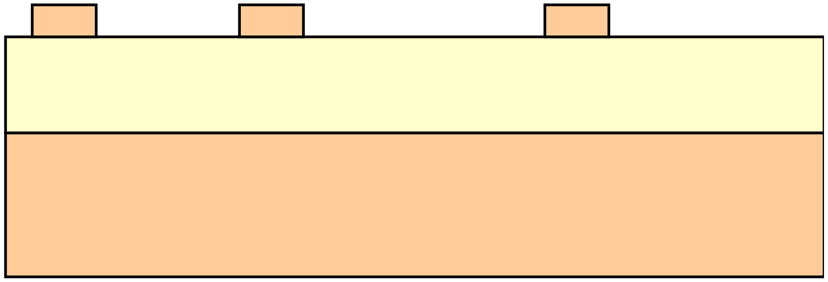
☺ high density of integration, collective processing

☺ high quality epitaxial III-V layers

Proposed integration process

Starting point: Processed SOI-waveguide wafer

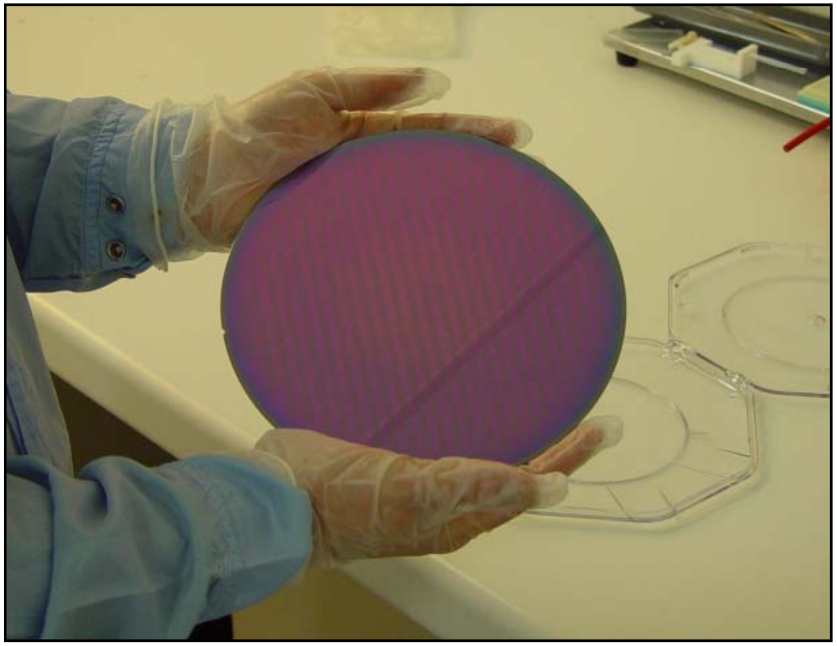


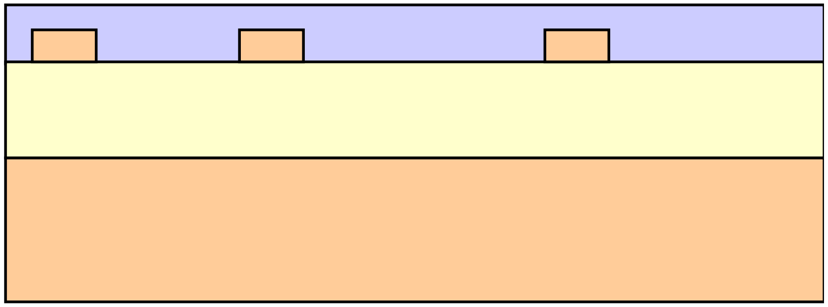


- 193nm or 248nm DUV lithography
  - Fabricated in pilot CMOS-line

Proposed integration process

Planarization

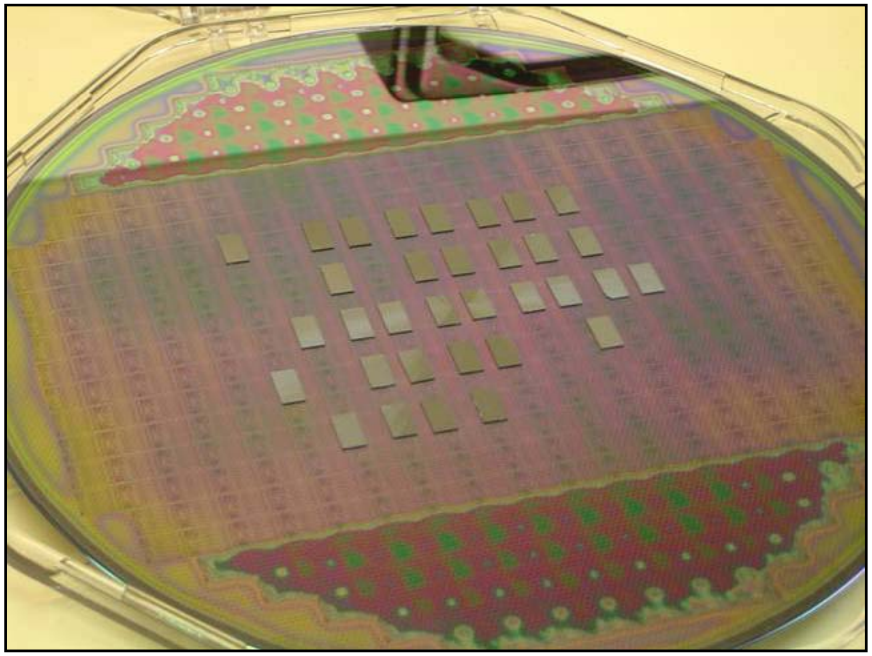


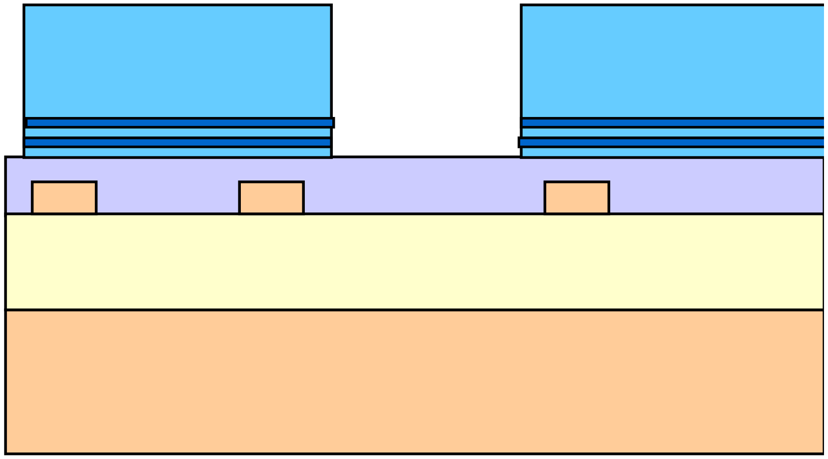


- Planarization
  - Using BCB (50nm to 2um) (UGent/IMEC)
  - Using SiO_2 (TRACIT - CEA-LETI)

Proposed integration process

Die-to-wafer bonding

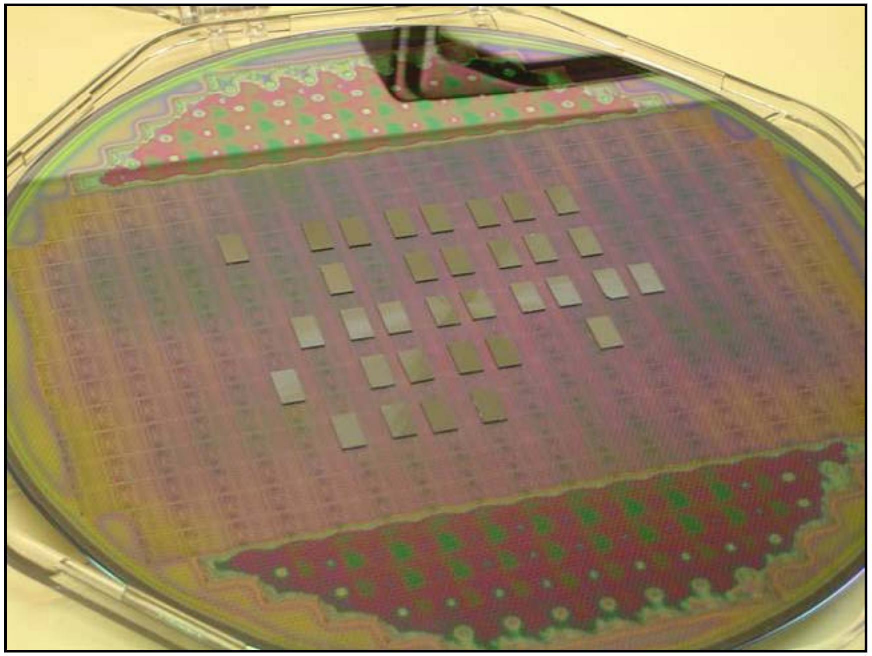


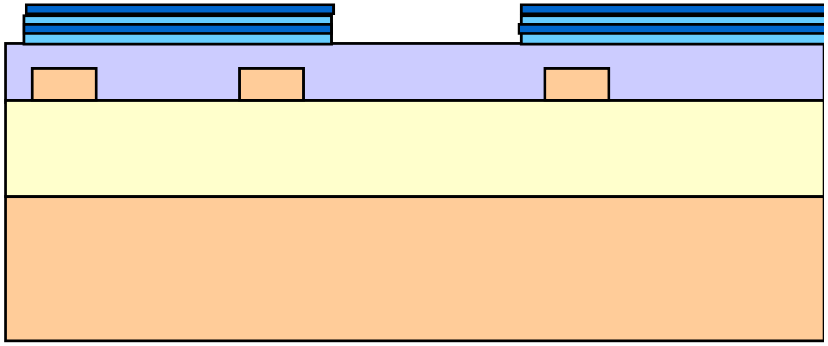


- Bonding InP-dies on top of planarized SOI-wafer
  - Low alignment accuracy required
  - ➔ Fast pick-and-place

Proposed integration process

Substrate removal

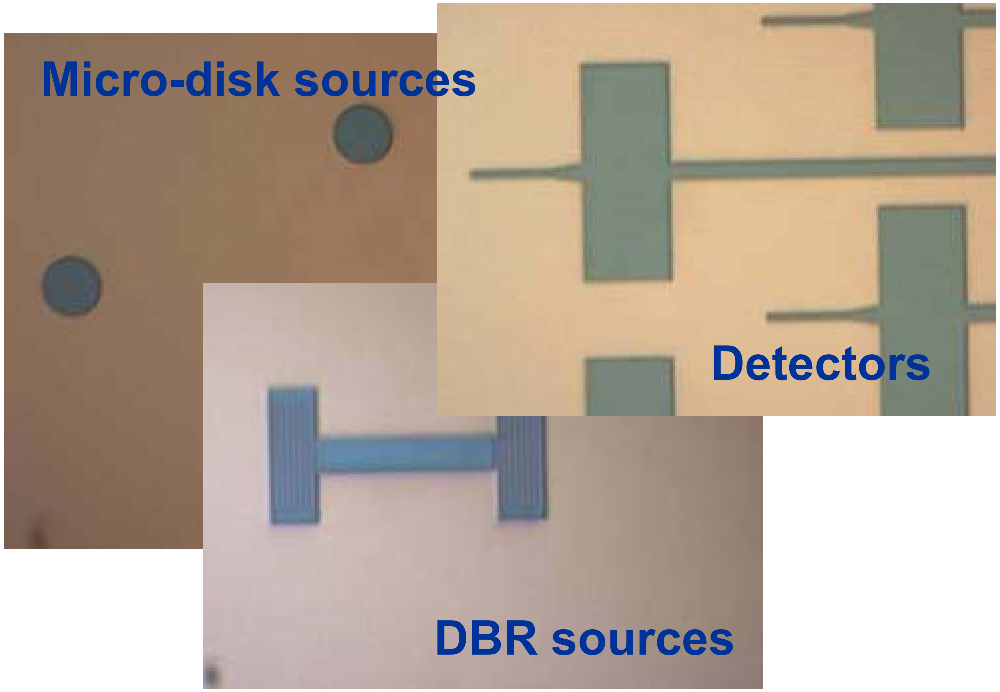


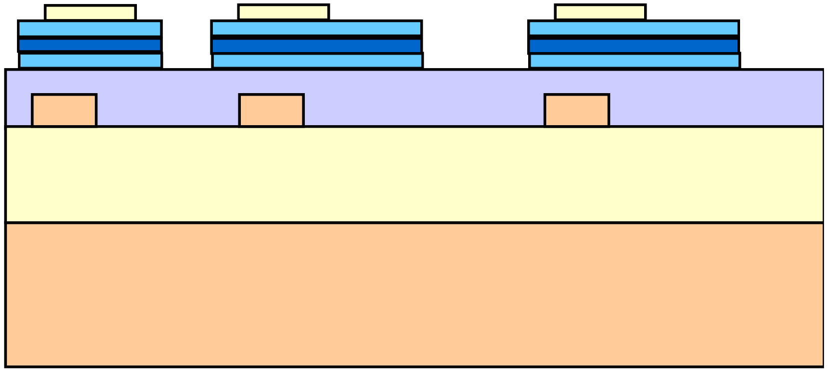


- Remove InP-substrate down to etch stop layer
- Remove etch stop
- Thin membrane remains (200nm ~ 2 µm)

Proposed integration process

Hardmask deposition

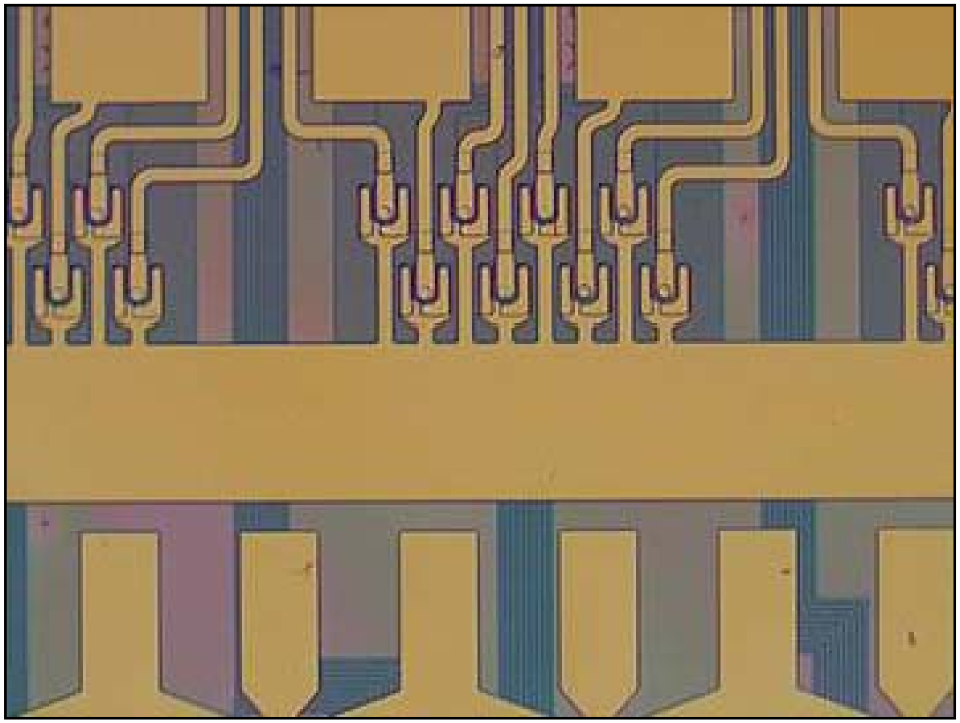


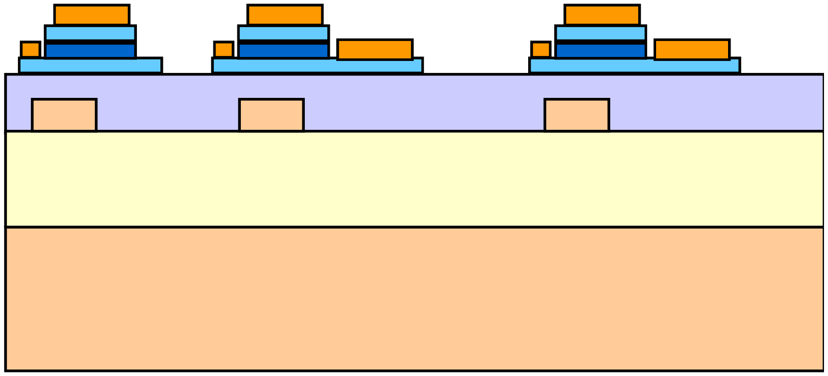


- Decontamination and hardmask deposition
  - Alignment of waveguides and devices through lithographic methods

Proposed integration process

Processing of InP-optoelectronic devices





- Mesa etching and Metallization
  - "Waferscale" processing !!!
    - on 2cm^2 pieces (UGent, INL)
    - on 200mm wafers (CEA-LETI)

III-V/Silicon photonics

Bonding of III-V epitaxial layers

- Molecular die-to-wafer bonding
    - Based on van der Waals attraction between wafer surfaces
    - Requires “atomic contact” between both surfaces

      - very sensitive to **particles**

      - very sensitive to **roughness**

      - very sensitive to **contamination of surfaces**
- Adhesive die-to-wafer bonding
    - Uses an adhesive layer as a glue to stick both surfaces
    - Requirements are more relaxed compared to Molecular

      - glue compensates for particles (some)

      - glue compensates for roughness (all)

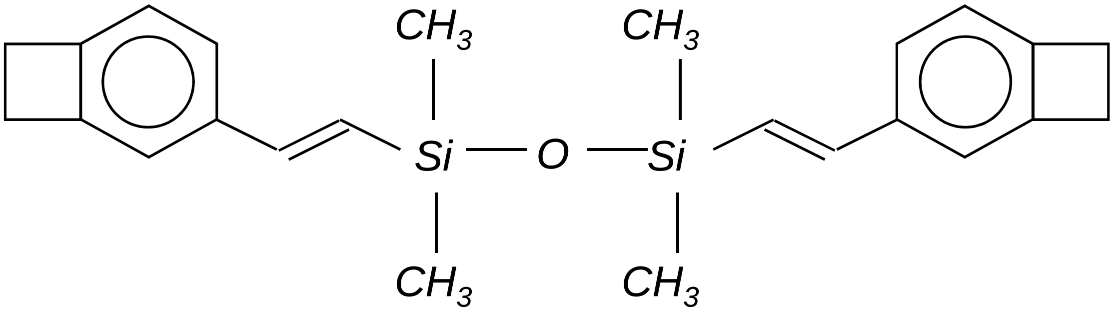
      - glue allows (some) contamination of surfaces

Bonding Technology

Requirements for the adhesive for bonding

- Optically transparent <0.1dB/cm
- High thermal stability (post-bonding thermal budget) 400C
- Low curing temperature (low thermal stress) 250C
- No outgassing upon curing (void formation) OK
- Resistant to all kinds of chemicals $HCl, H_2SO_4, H_2O_2, \ldots$

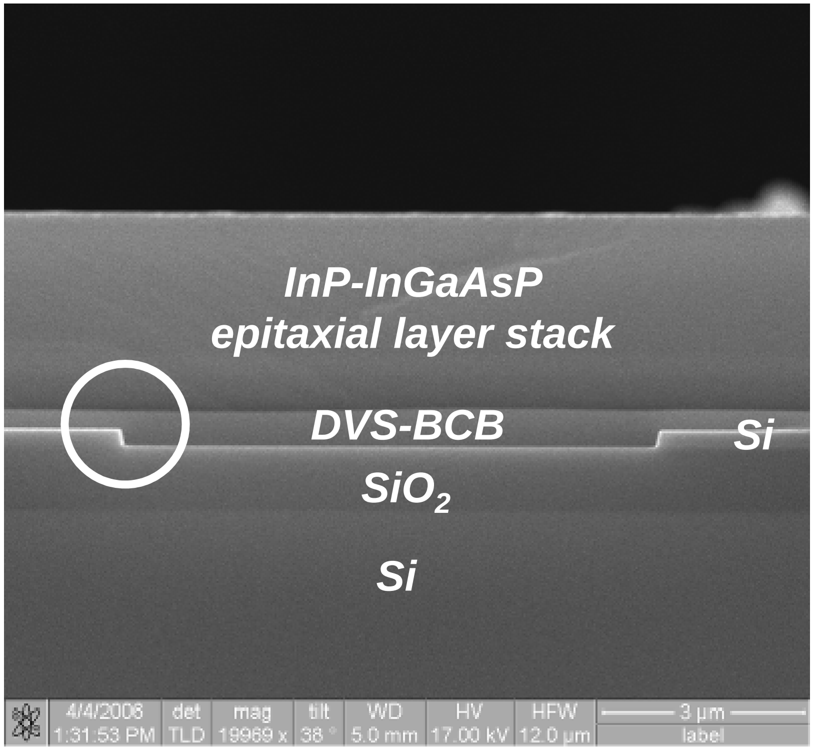
DVS-BCB satisfies these requirements

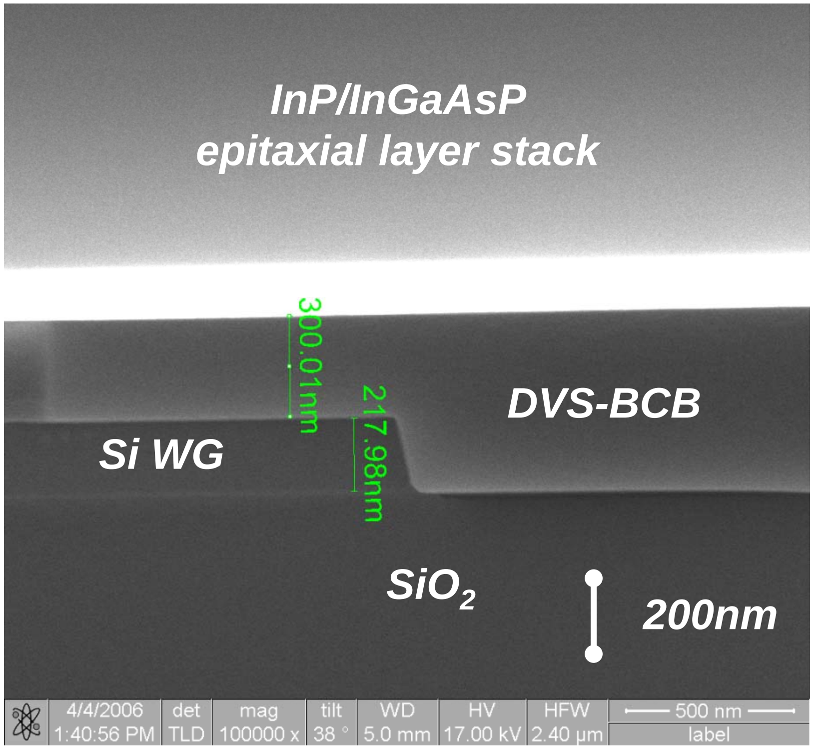


1,3-divinyl-1,1,3,3-tetramethyldisiloxane-bisbenzocyclobutene

Bonding Technology

Cross-sectional image of III-V/Silicon substrate

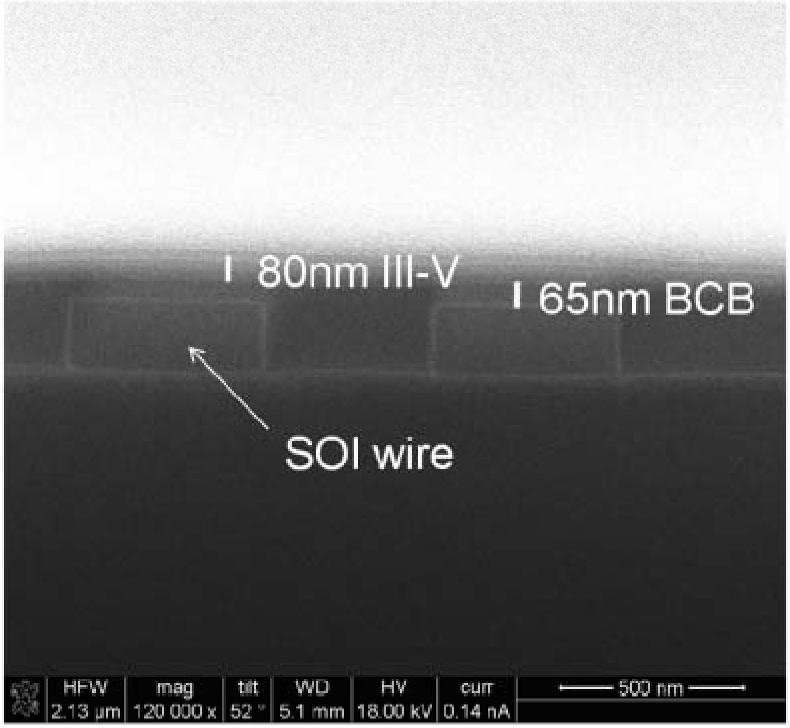


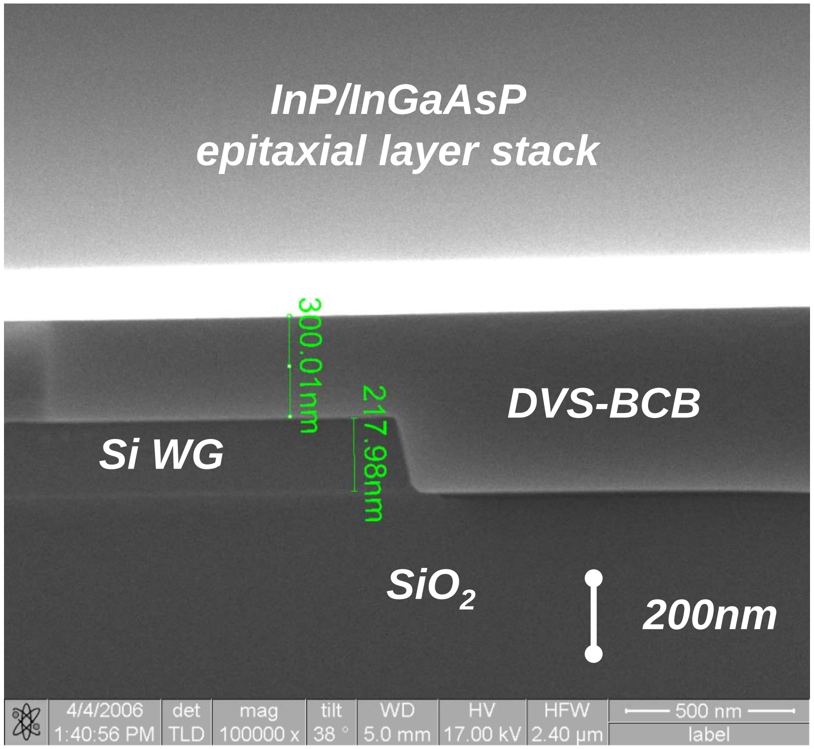


- **300nm bonding layer routinely and reliably obtained**

Bonding Technology

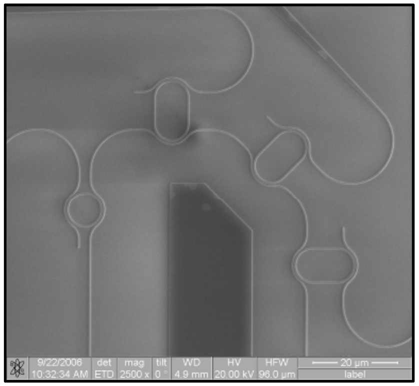
Cross-sectional image of III-V/Silicon substrate

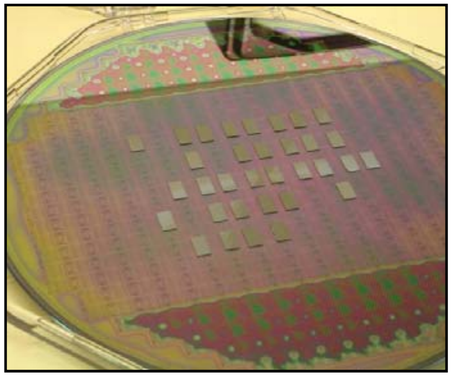


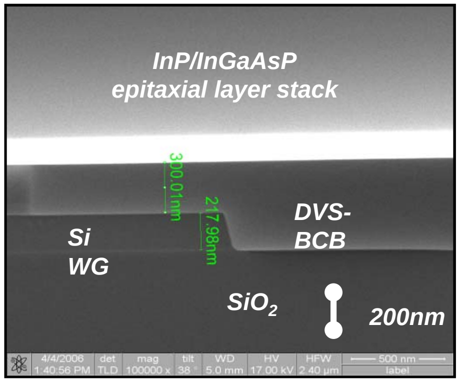


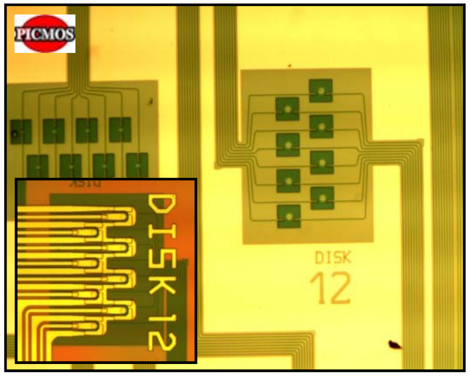
- **300nm bonding layer routinely and reliably obtained**
- **Recently also sub-100nm layers demonstrated**

III-V silicon heterogeneous integration









1. Silicon photonics is great !!!

2. But we still need InP

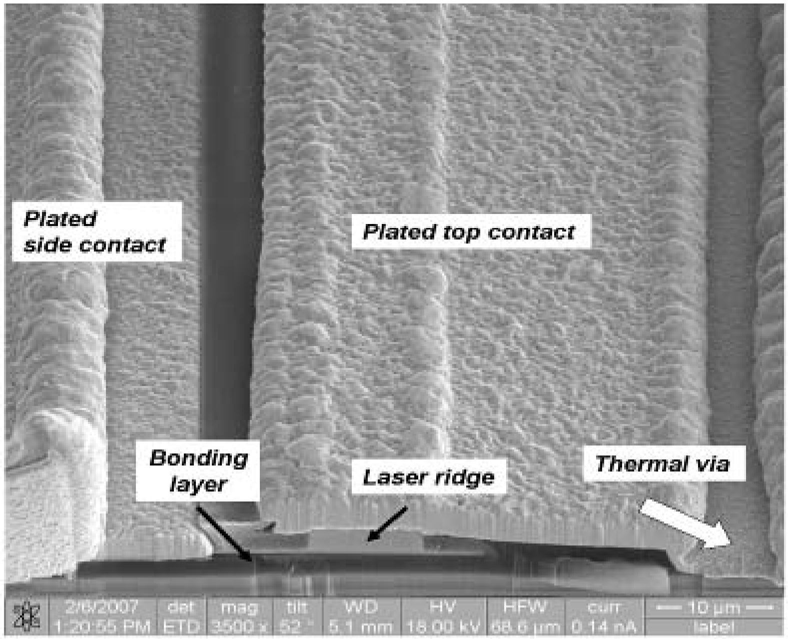
3. III-V silicon integration

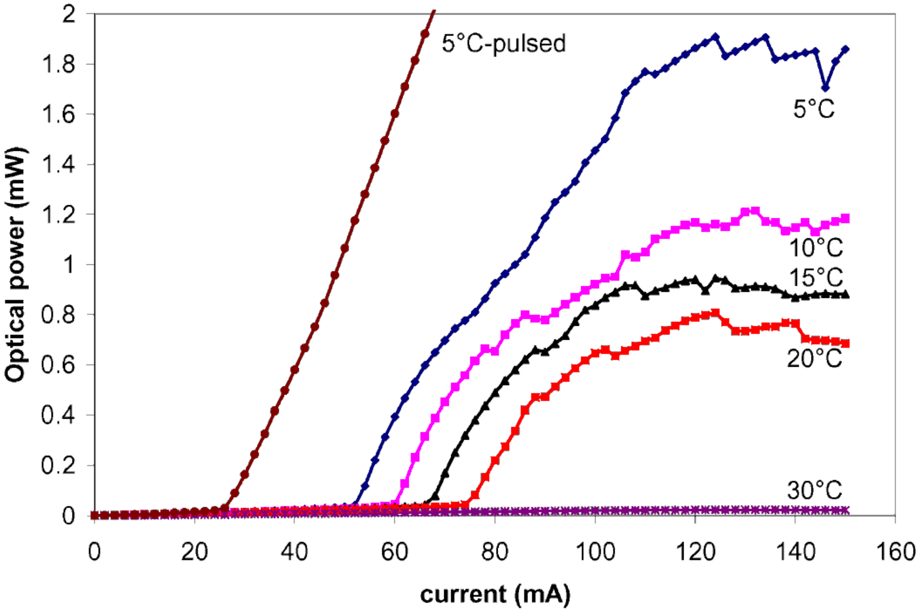
4. Devices

Integrated Devices: laser diode

Integrated laser diodes

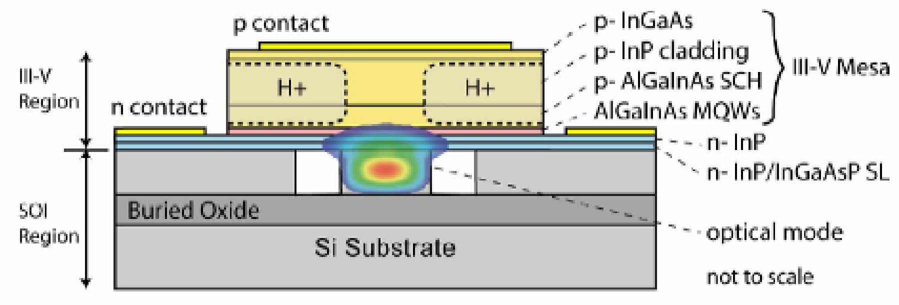
- First only pulsed operation due to high thermal resistivity DVS-BCB
- Integration of a heat sink to improve heat dissipation
- Continuous wave operation achieved this way



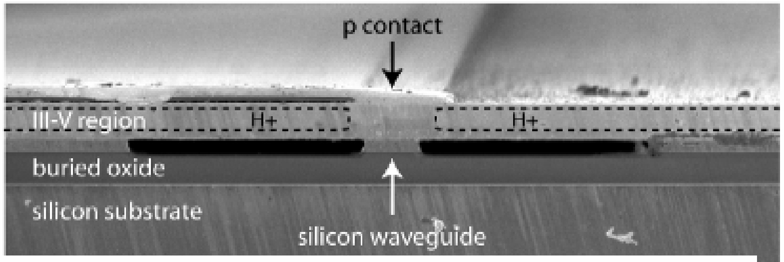


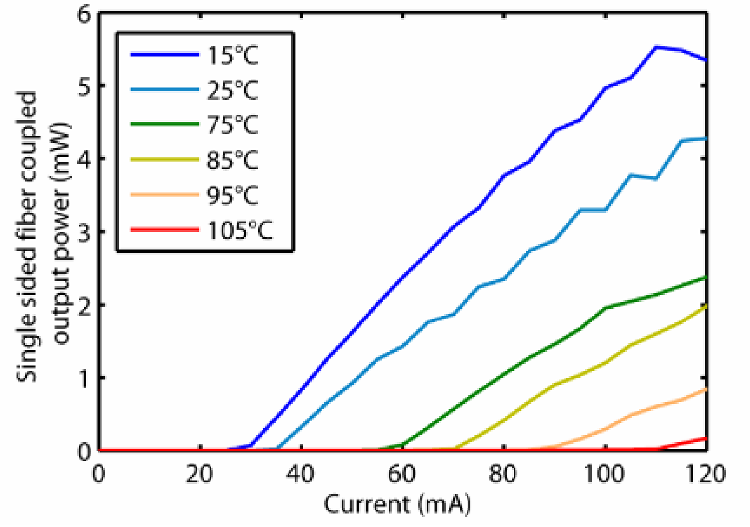
Other groups

Intel / UCSB Hybrid laser

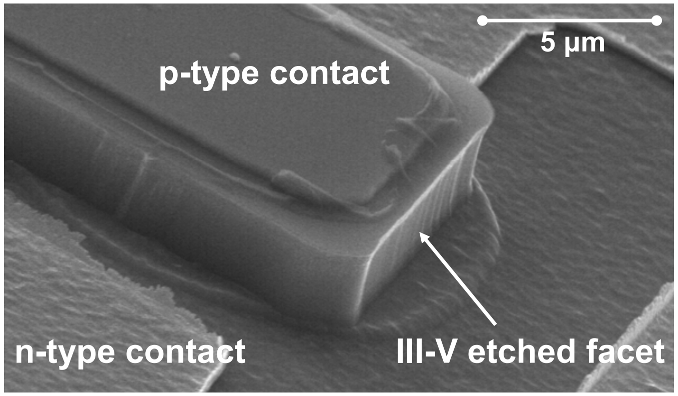


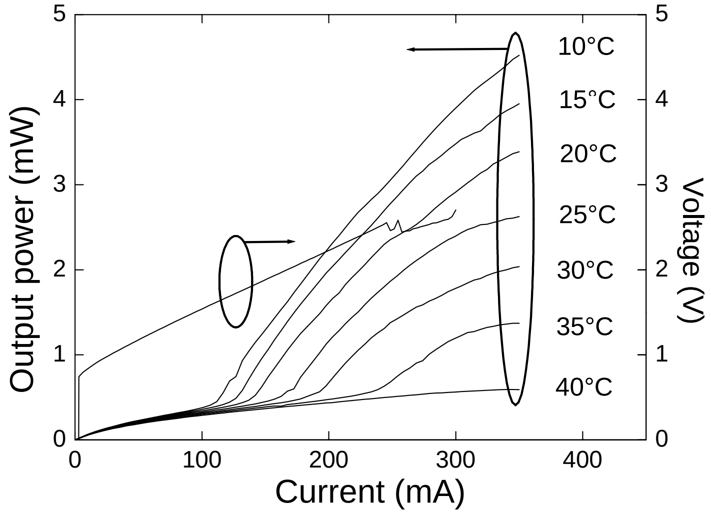
(a)





CEA-LETI / III-V lab





(IPRM ‘08, paper MoA4.2)

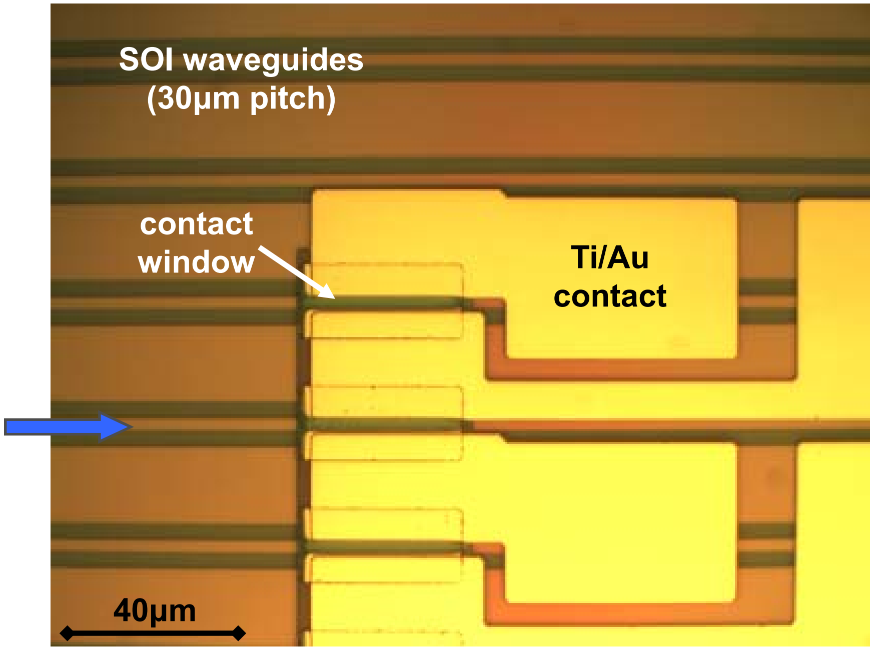
MSM detectors

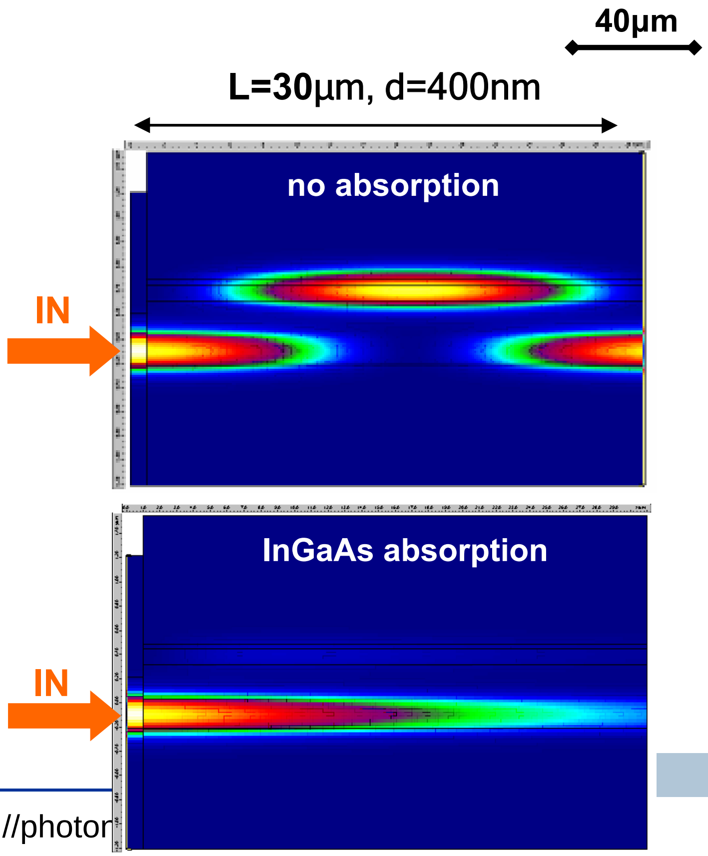
- Etching of detectors in III-V
- Spinning insulation layer of polyimide
- Opening contact window
- Metallization

25µm long detector

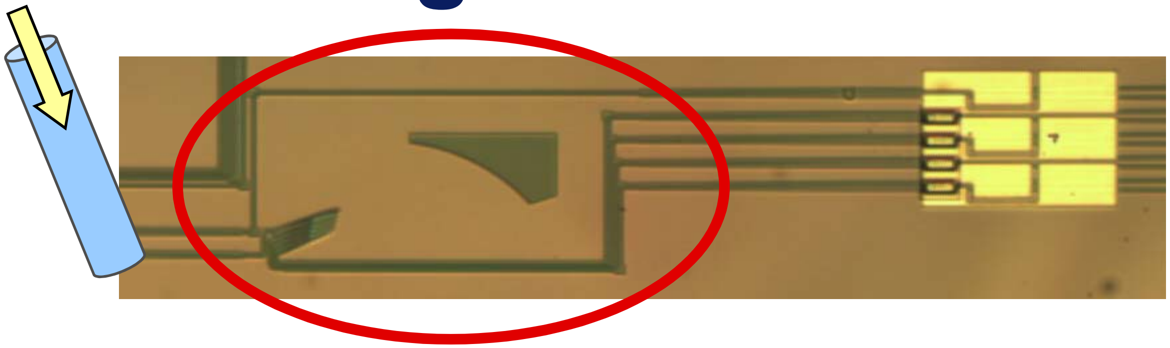
R = 1.0A/W (1550nm), IQE = 80% (5V bias)

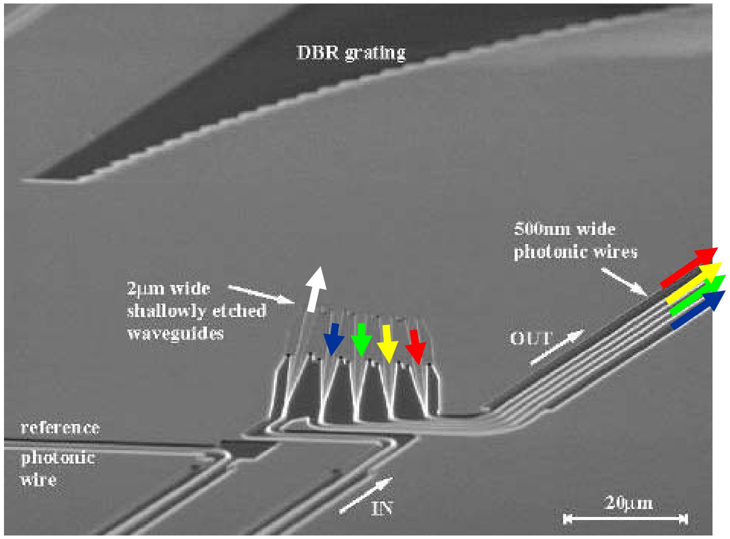
I_{dark} = 3nA (5V bias)





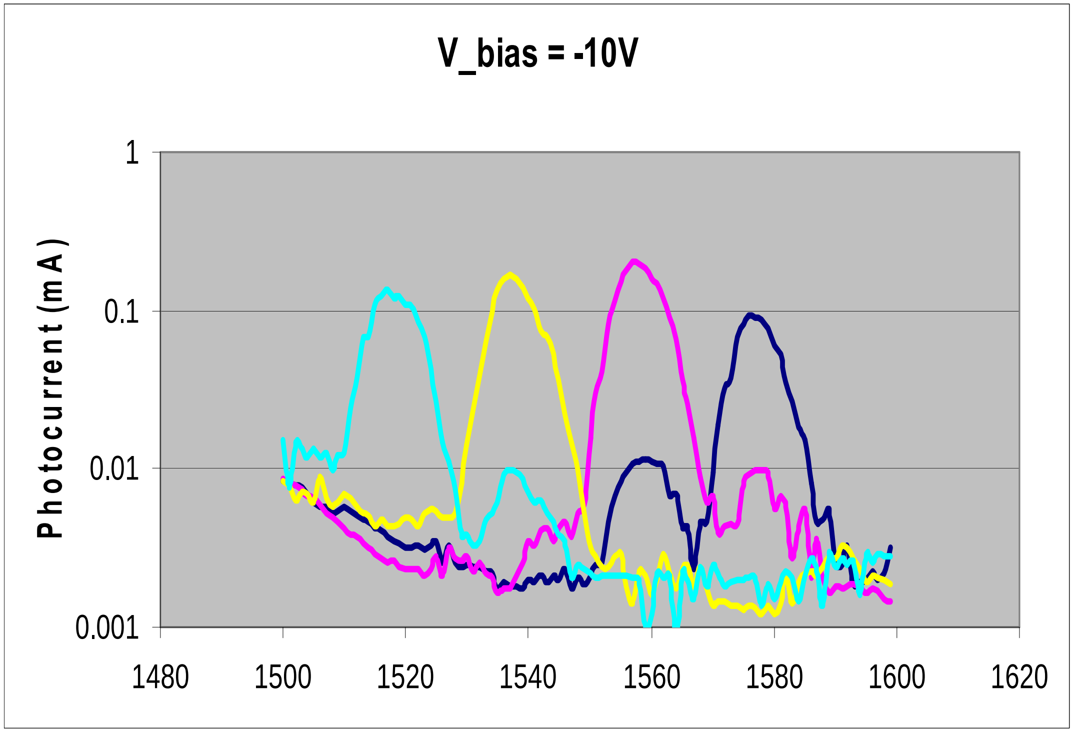
Wavelength selective filter





1x4 demux, Δλ=20nm,

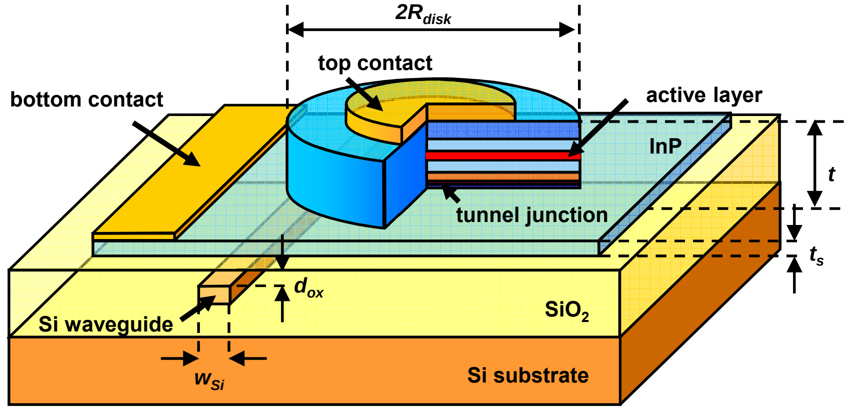
280µm x 150µm



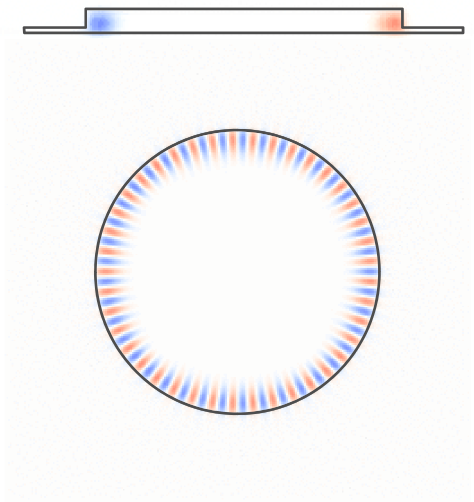
Integrated microdisk laser

Microdisk laser design

- Whispering-gallery modes
- Central top contact
- Bottom contact on thin lateral contact layer (t_S)
- Hole injection through a reverse-biased tunnel-junction

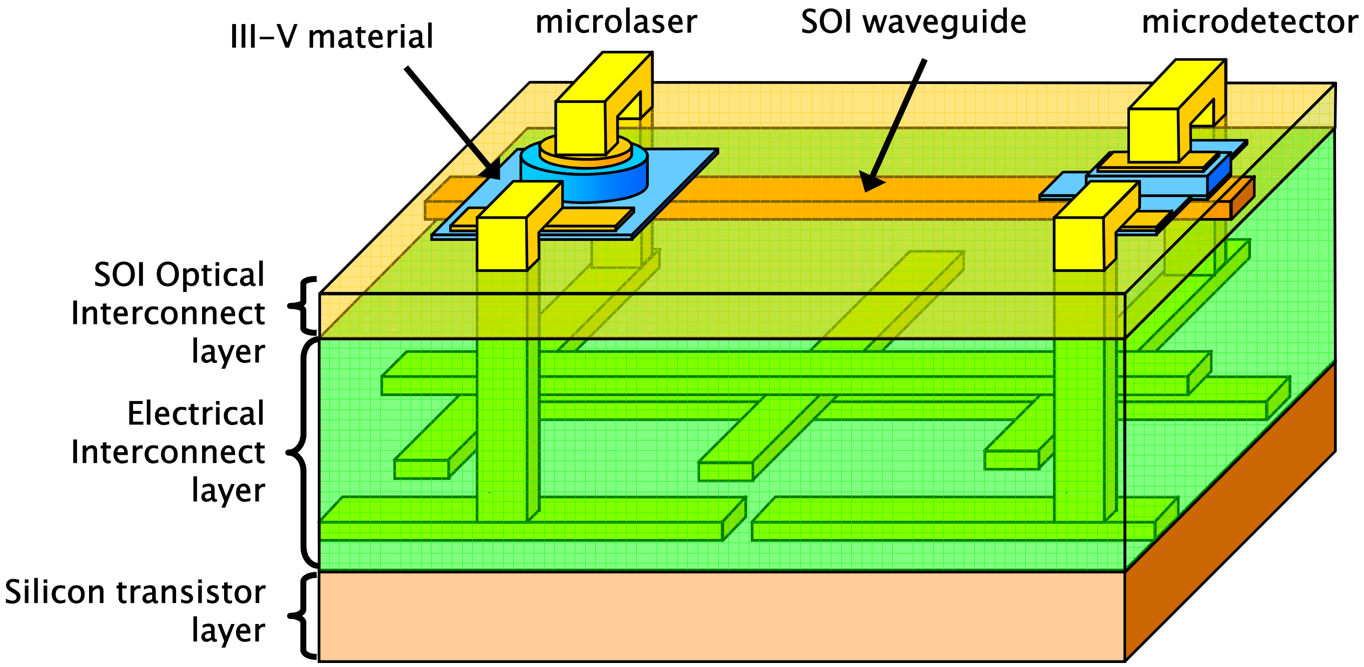


- Microdisk thickness $0.5 < t < 1\mu m$
- Evanescent coupling to SOI wire waveguide ($500x220nm^2$)



On-chip optical interconnect ?

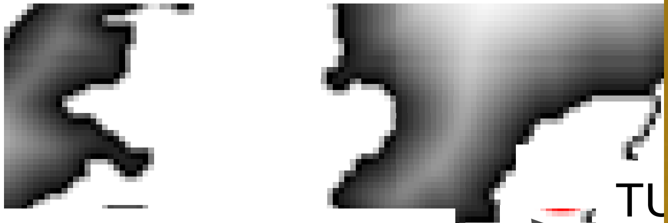
Integrate photonic interconnect on CMOS ?



- Need integrated interconnect layer on top of CMOS
  - Silicon wiring for interconnect
  - III-V microdevices for sources and detectors

PICMOS

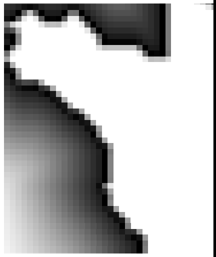
A collaborative project …



TU

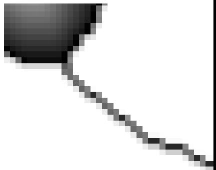
IMEC: metallization

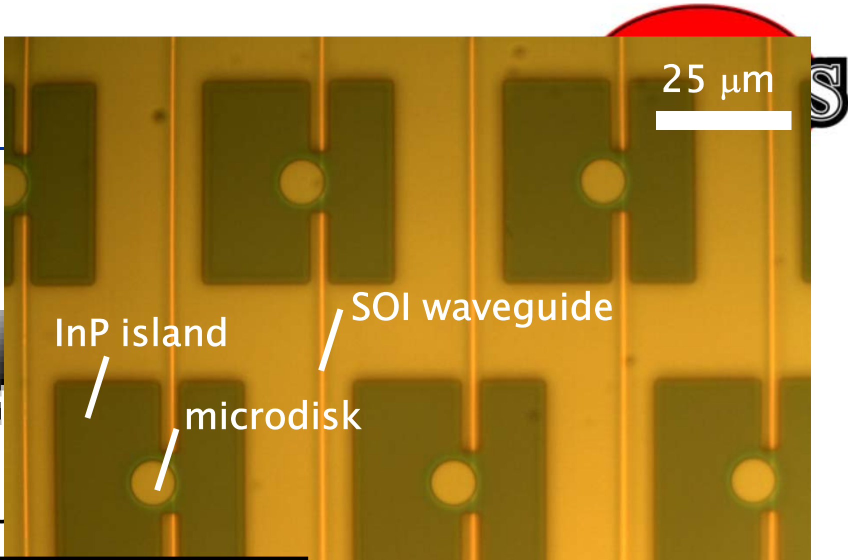
III-V proc

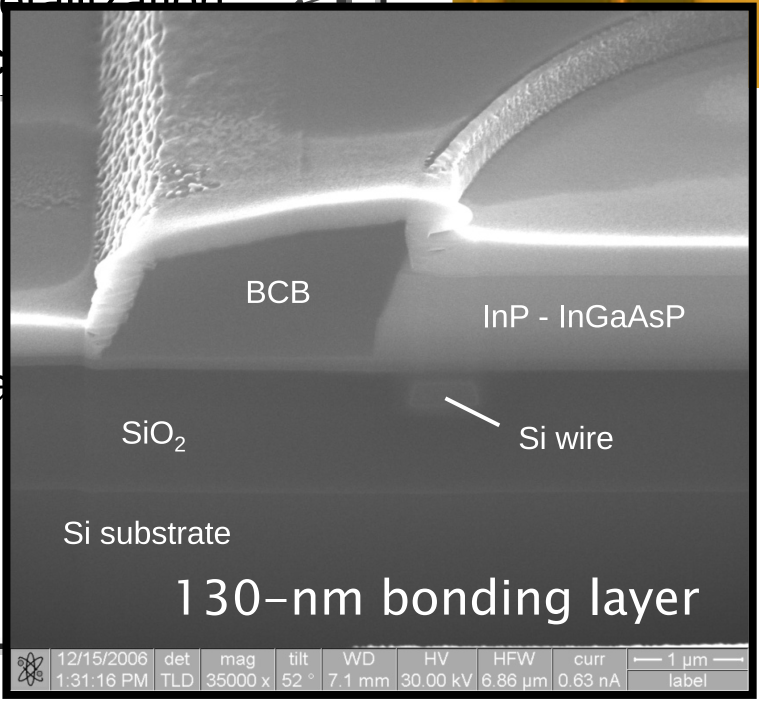


INL: substrate remova

INL: source etching



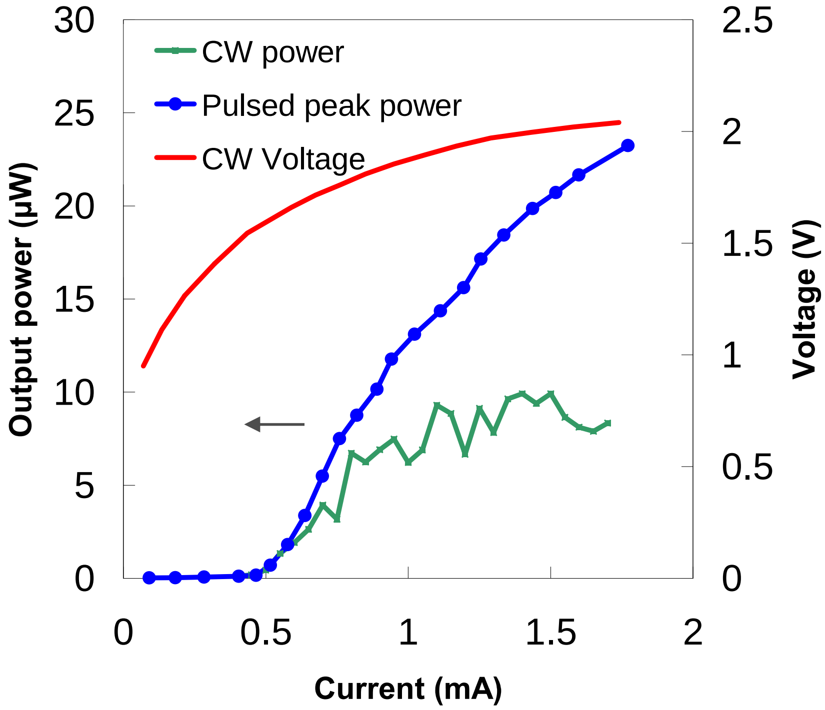


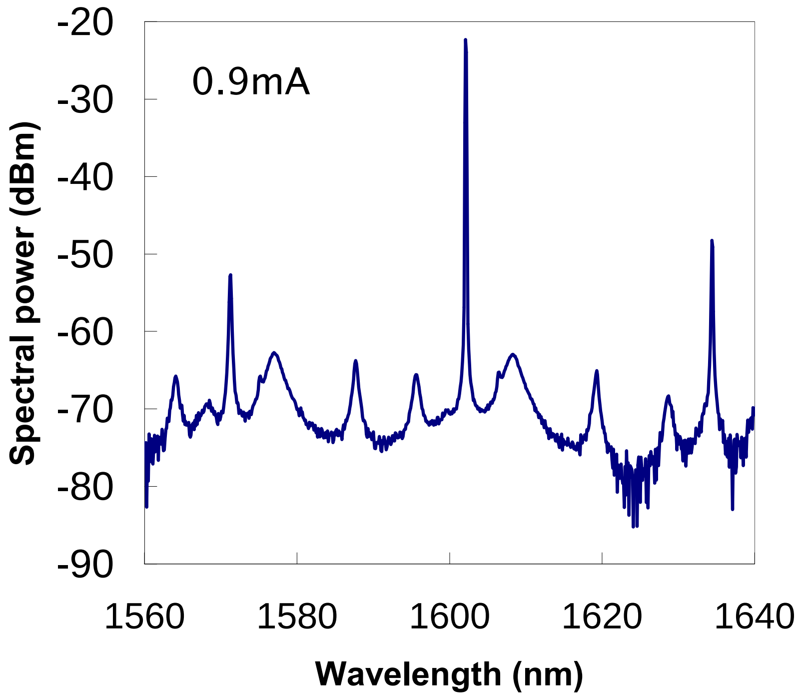


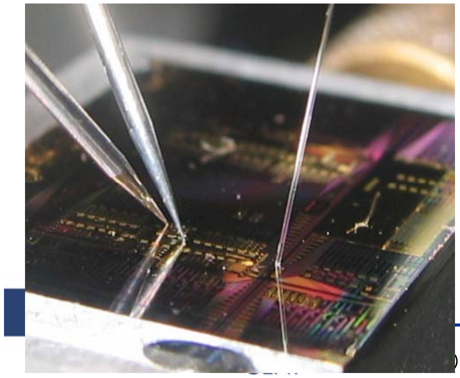
Six cleanrooms but still working devices …

Continuous-wave lasing

1-µm thick, 7.5-μm devices exhibit continuous-wave lasing







Threshold current I_{th} = 0.5mA, voltage V_{th} = 1.5-1.7V

slope efficiency = 30μW/mA, up to 10μW

(Pulsed regime: up to 100μW peak power)

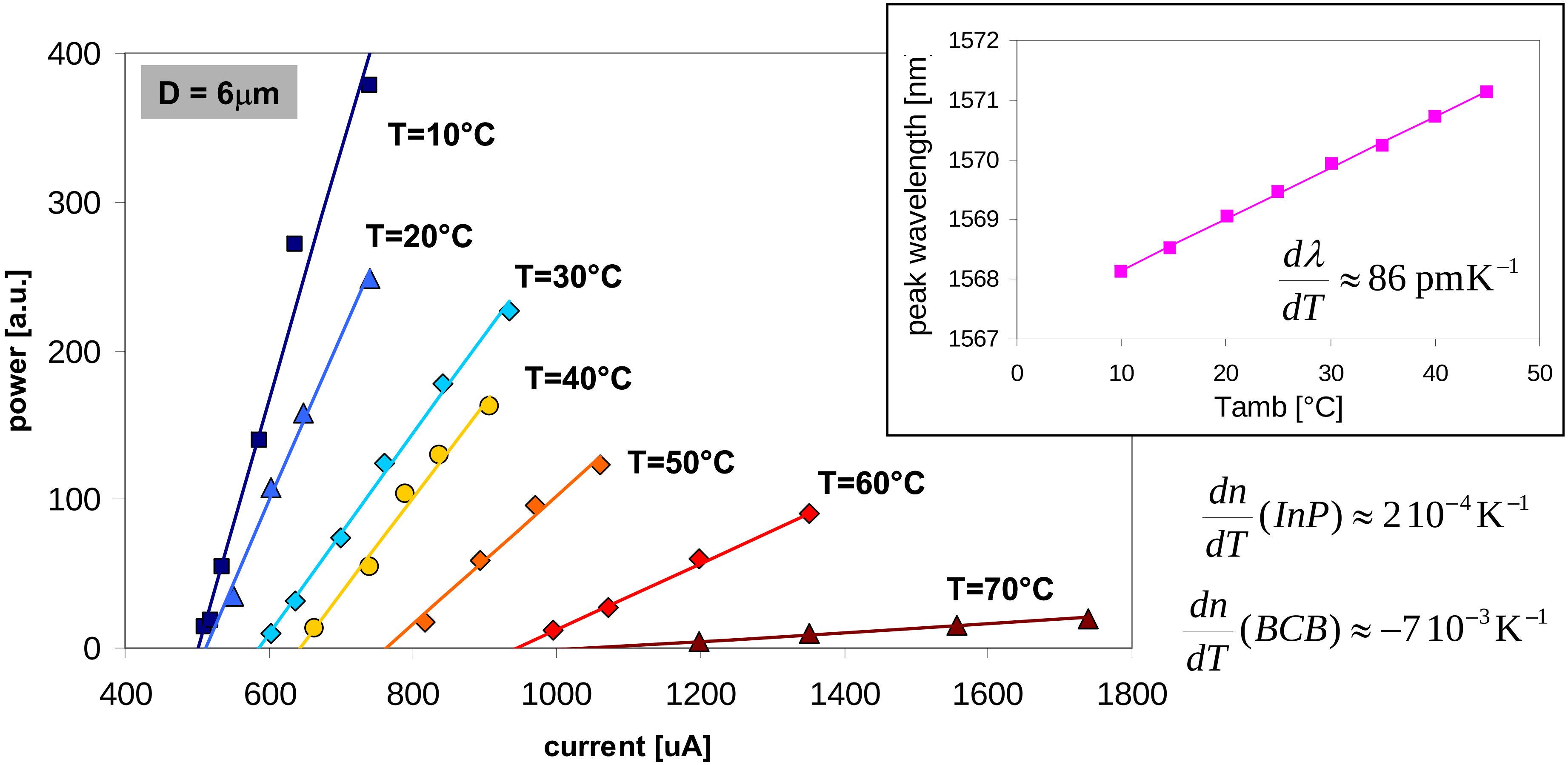
J. Van Campenhout et al., *"Electrically pumped inp-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit"* Optics Express, May 2007

Temperature dependence

PICMOS

“Laser emission up to 70°C”

(pulsed operation)

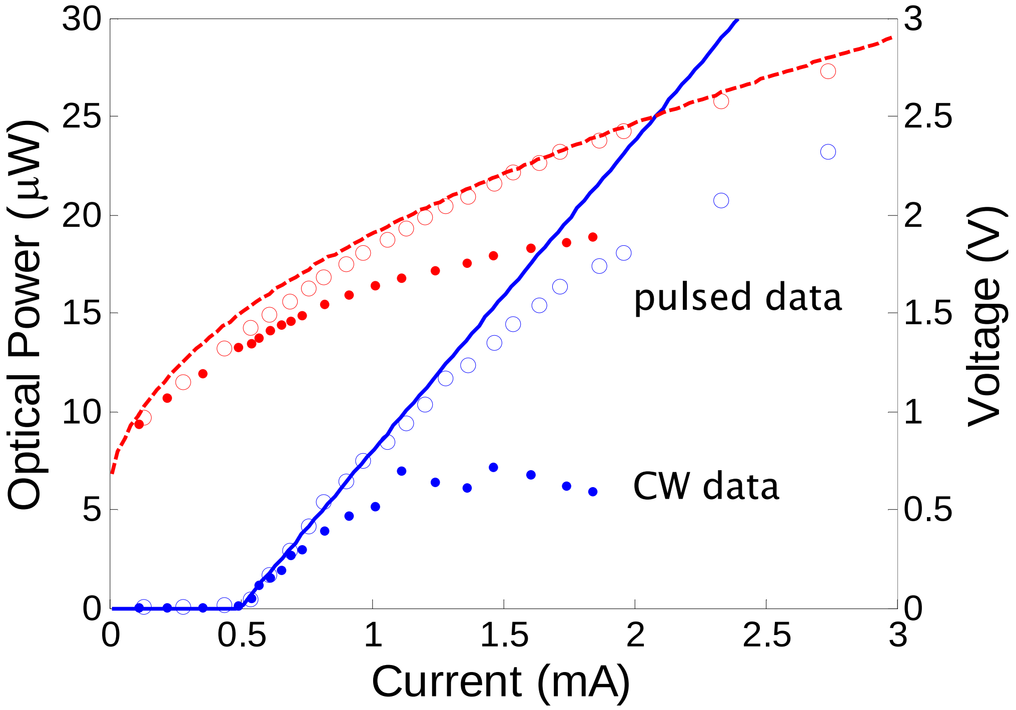


$$\frac{d\lambda}{dT} \approx 86\ \mathrm{pmK}^{-1}$$

$$\frac{dn}{dT}(InP) \approx 2\,10^{-4}\,\mathrm{K}^{-1}$$

$$\frac{dn}{dT}(BCB) \approx -7\,10^{-3}\,\mathrm{K}^{-1}$$

Fit to experimental data

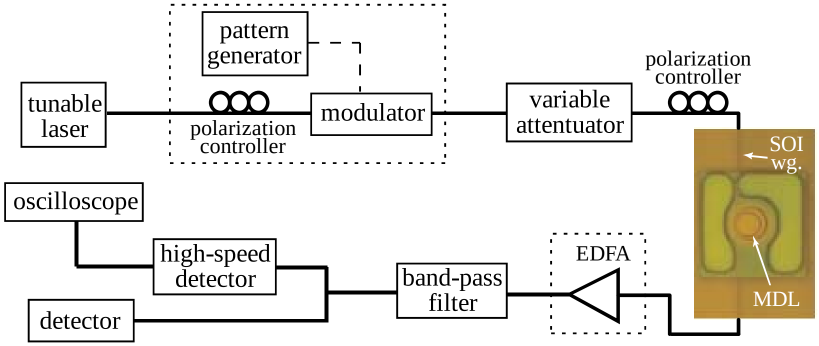


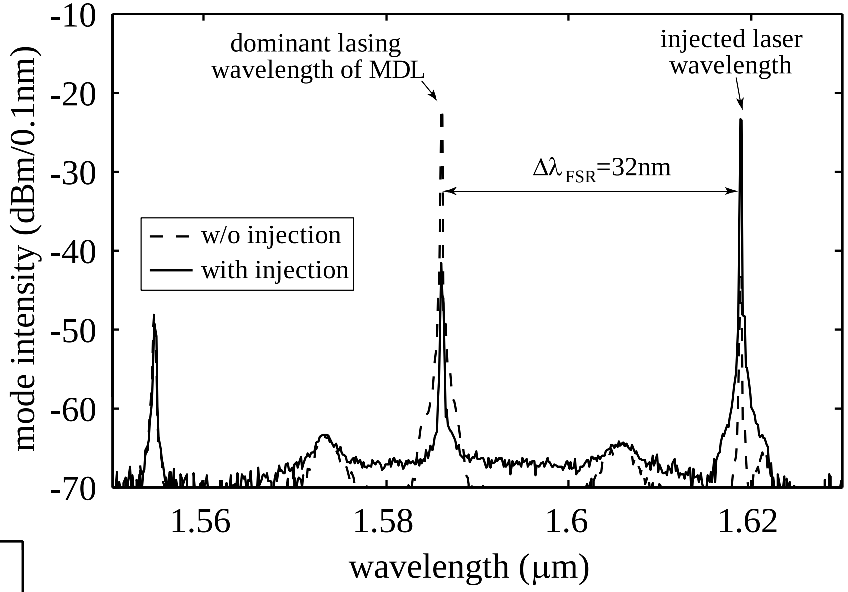
Model can be fitted to pulsed experimental data, assuming:

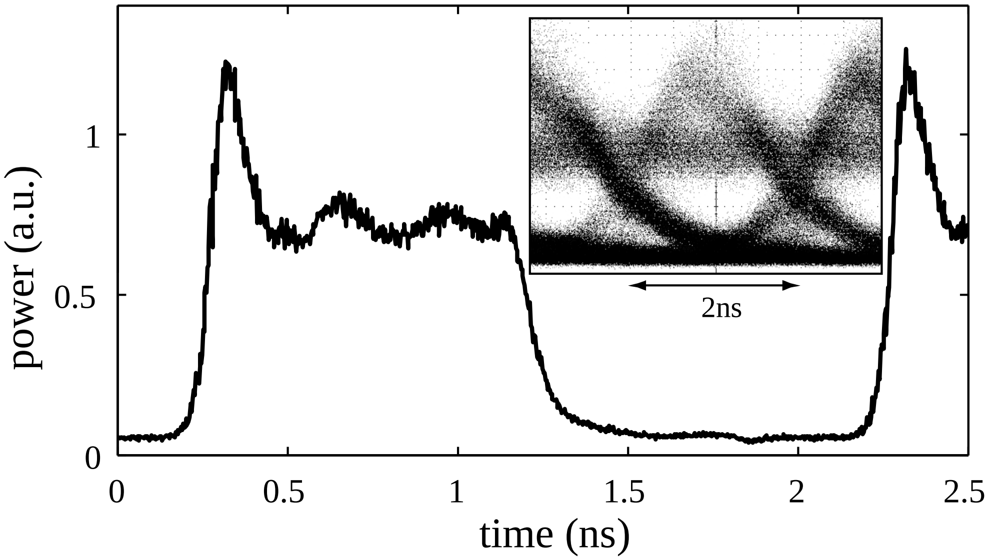
- uniform injection: injection efficiency =0.36x0.7=0.25
- coupling loss = 3cm^{-1} (simulation)
- tunnel-junction p-doping N_a = 2x10^{18}cm^{-3}
  (design target N_a = 2x10^{19}cm^{-3}, SIMS analysis: N_a ~ 8x10^{18}cm^{-3})
- fitted scatter loss = 8cm^{-1} (passive ring resonators: 7-13cm^{-1})

Consistent fit, except for tunnel-junction p-doping and saturation effect

Ultra-low-power Wavelength conversion



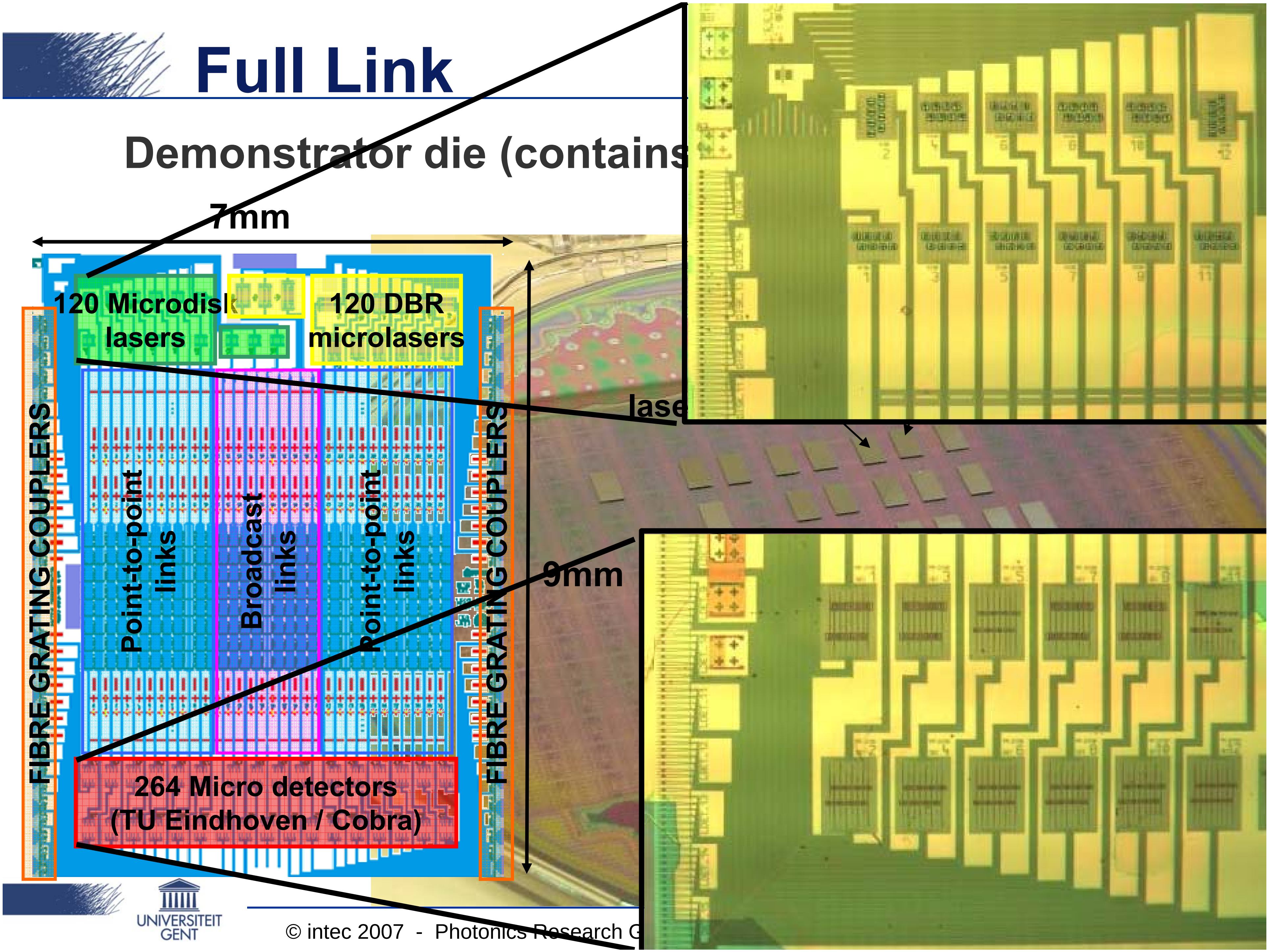




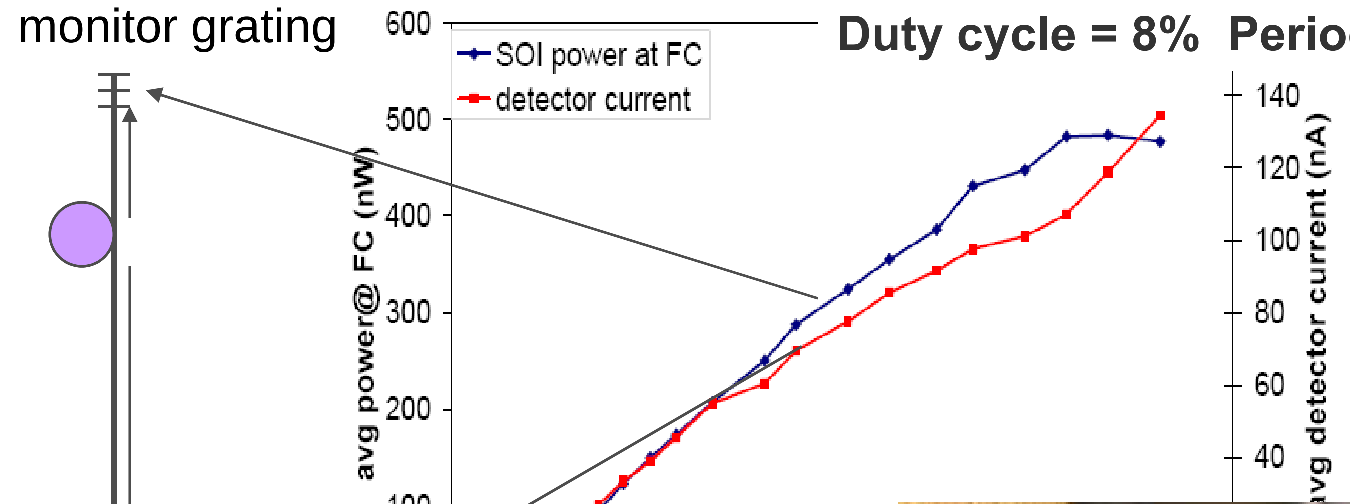
- No control power needed.
- Wavelength conversion with only 6.4uW control power.
- 5Gbps dynamic results.

Full Link

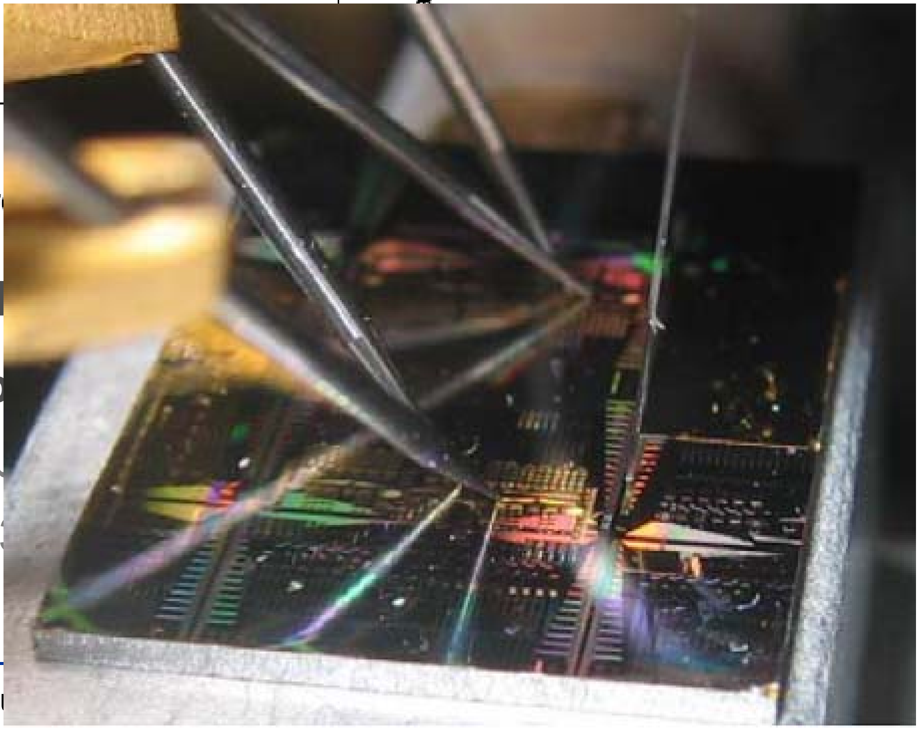
Demonstrator die (contains



Pulsed operation of the link



Duty cycle = 8% Period = 1 µs



- **Detector not biased (0V), negl**
- **Performance under pulsed op**
  - **Threshold current < 700**
  - **Detector efficiency of 0.2**

Outlook & conclusion

We demonstrated:

- Ultra-dense waveguiding
  - < 2 µm pitch (waveguide-to-waveguide)
- A powerfull III-V on Silicon integration technology
- Several proof-of-principle demonstrators
  - Electrically pumped micro-disk sources on silicon platform
    - 500 µA threshold current
  - Micro-detectors on silicon platform
    - 1.0A/W
- Fabrication using waferscale processes

k & conclusion

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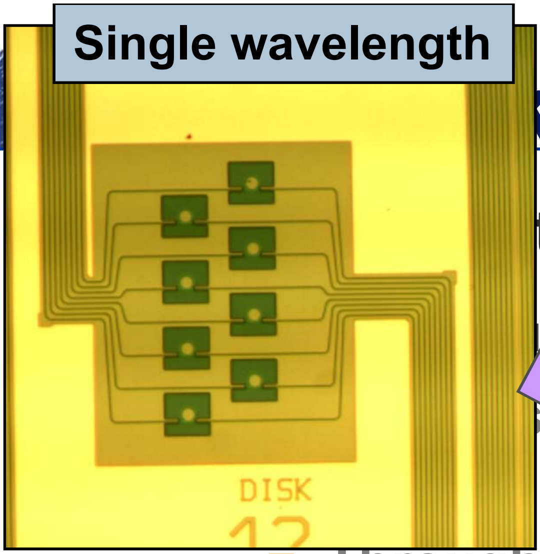
30% in

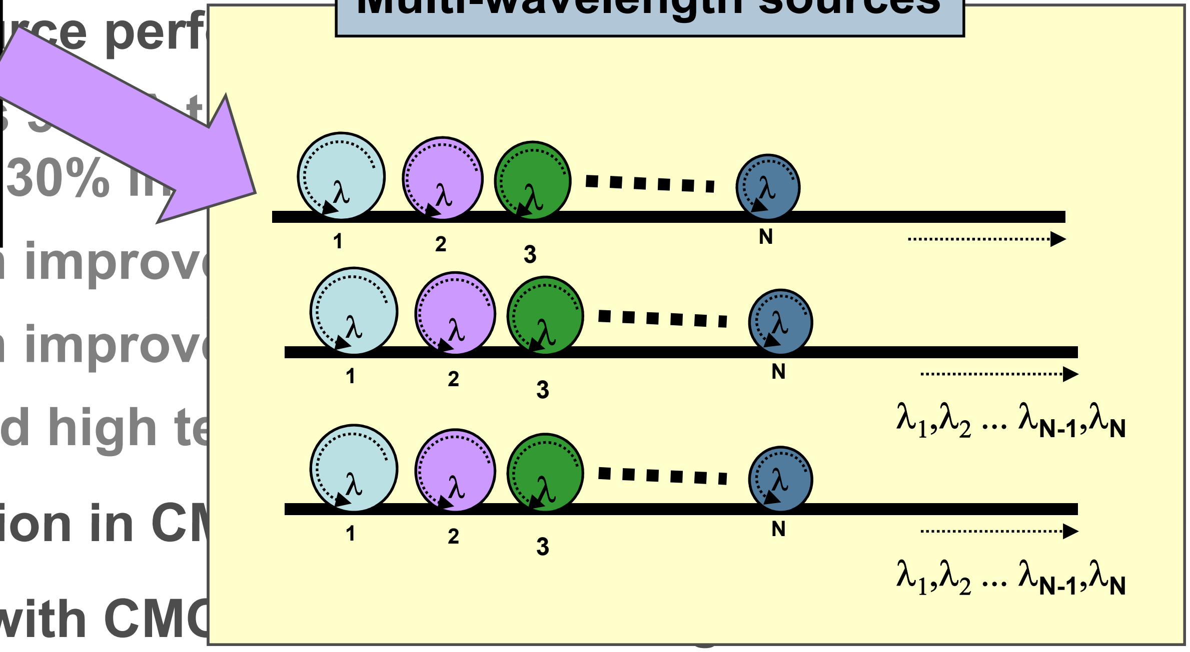
- Through improv
- Through improv
- Improved high te

- Full fabrication in CM
- Integration with CMO
- Implement WDM-functionality

Single wavelength

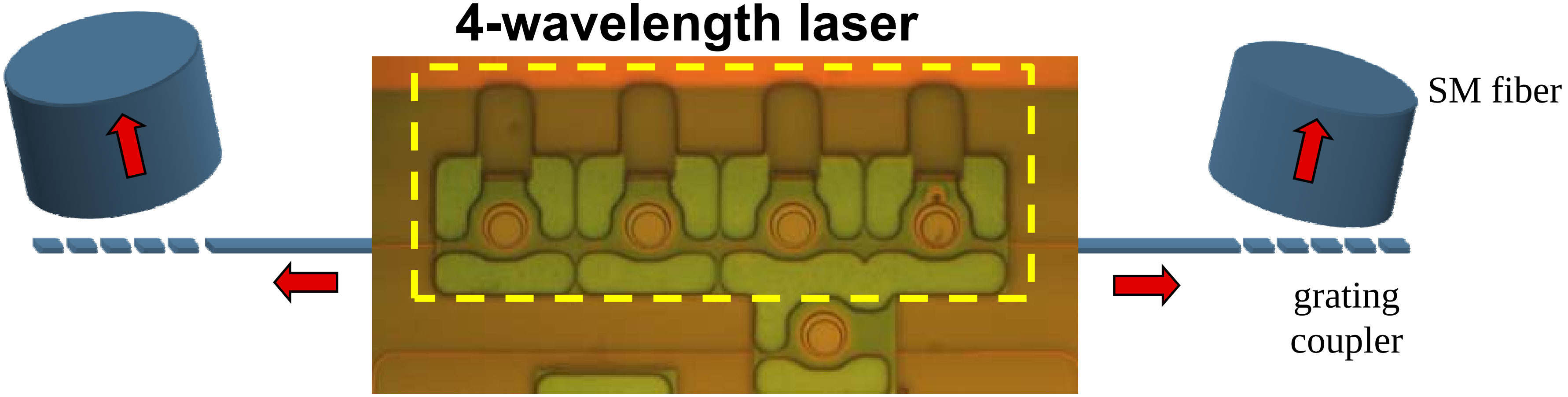


Multi-wavelength sources

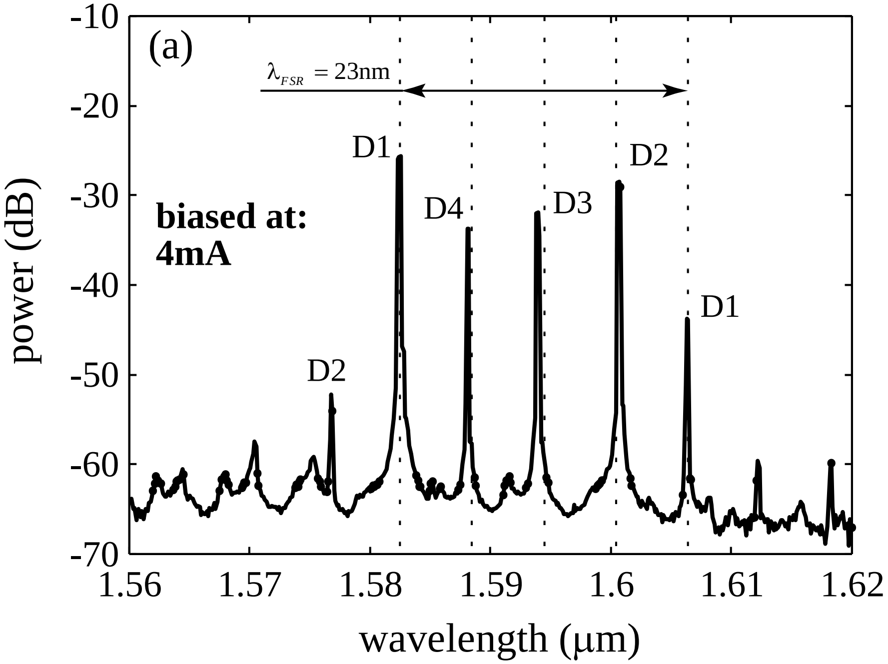


Multi-wavelength Laser

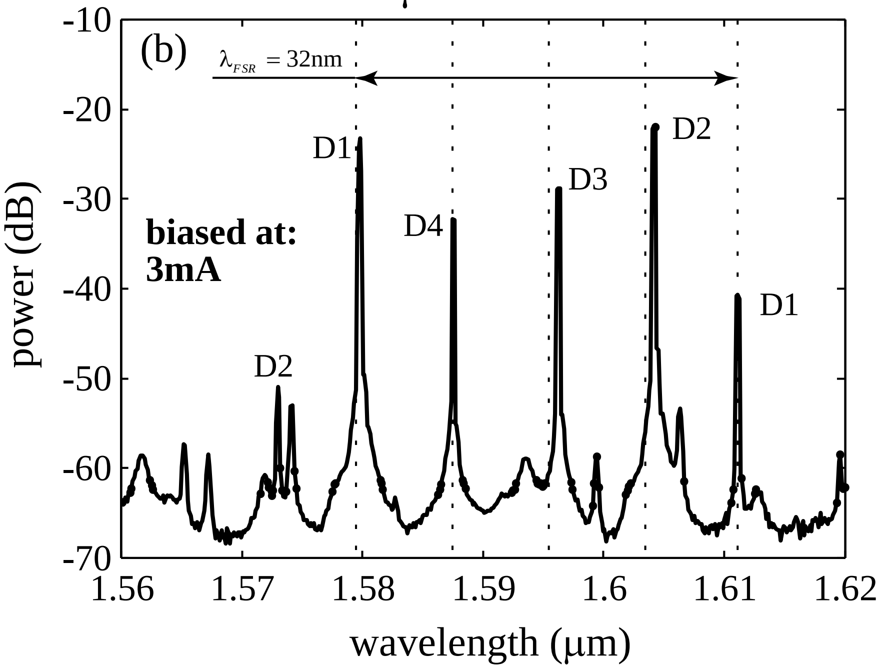
4-wavelength laser



10μm diameter



7.5μm diameter



Outlook & conclusion

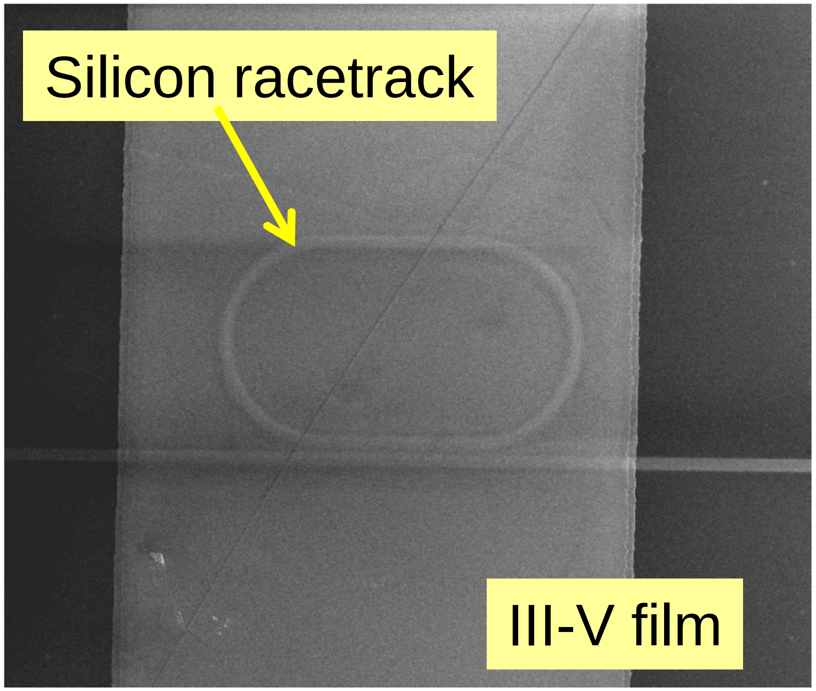
We still need to:

- Improve source performance
  - Towards 50 µA threshold current – 10GHz modulation speed – 30% internal efficiency
  - Through improved processing
  - Through improved device design
  - Improved high temperature operation
- Full fabrication in CMOS pilot-line
- Integration with CMOS electronic driving circuit
- Implement WDM-functionality
- Simplify overall processing

Outlook & conclusion

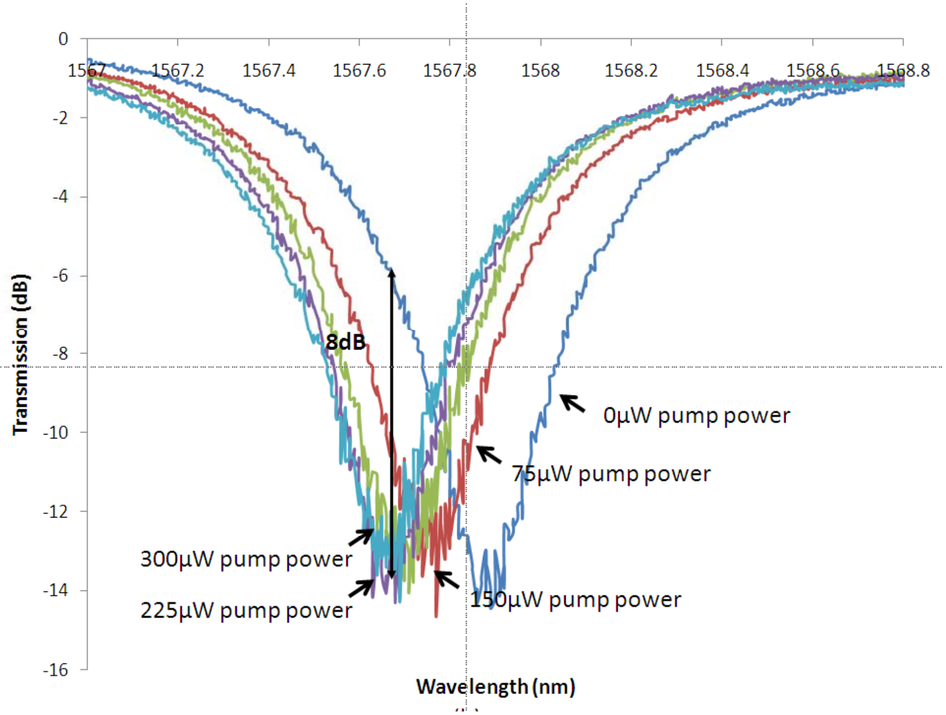
Simplify processing

- Avoid critical patterning in the III-V layer



Silicon racetrack

III-V film



Acknowledgements

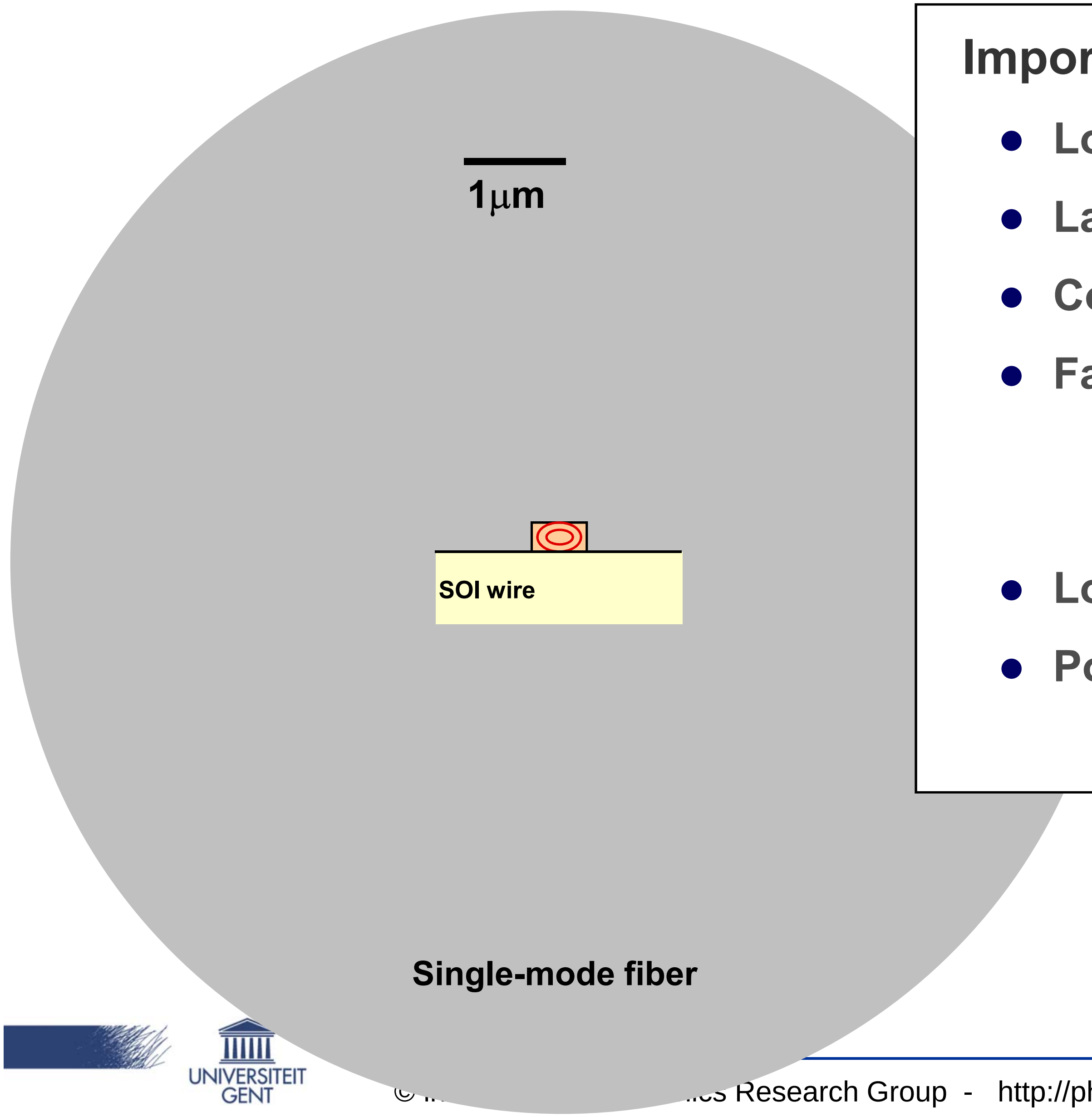
Photonics Research Group

- III-V silicon integration:
  - G. Roelkens, J. Van Campenhout, J. Brouckaert, L. Liu
- Silicon Processing
  - W. Bogaerts, P. Dumon, S. Selvarajan, R. Baets

PICMOS team

- J.M. Fedeli, L. Di Cioccio (LETI) (molecular bonding, processing)
- C. Lagahe, B. Aspar (TRACIT) (planarization)
- C. Seassal, P. Rojo-Romeo, P. Regreny, P. Viktorovitch (INL) (processing, epitaxy)
- R. Notzel, X.J.M. Leijtens (TU/e) (epitaxy)

Fiber-chip coupling



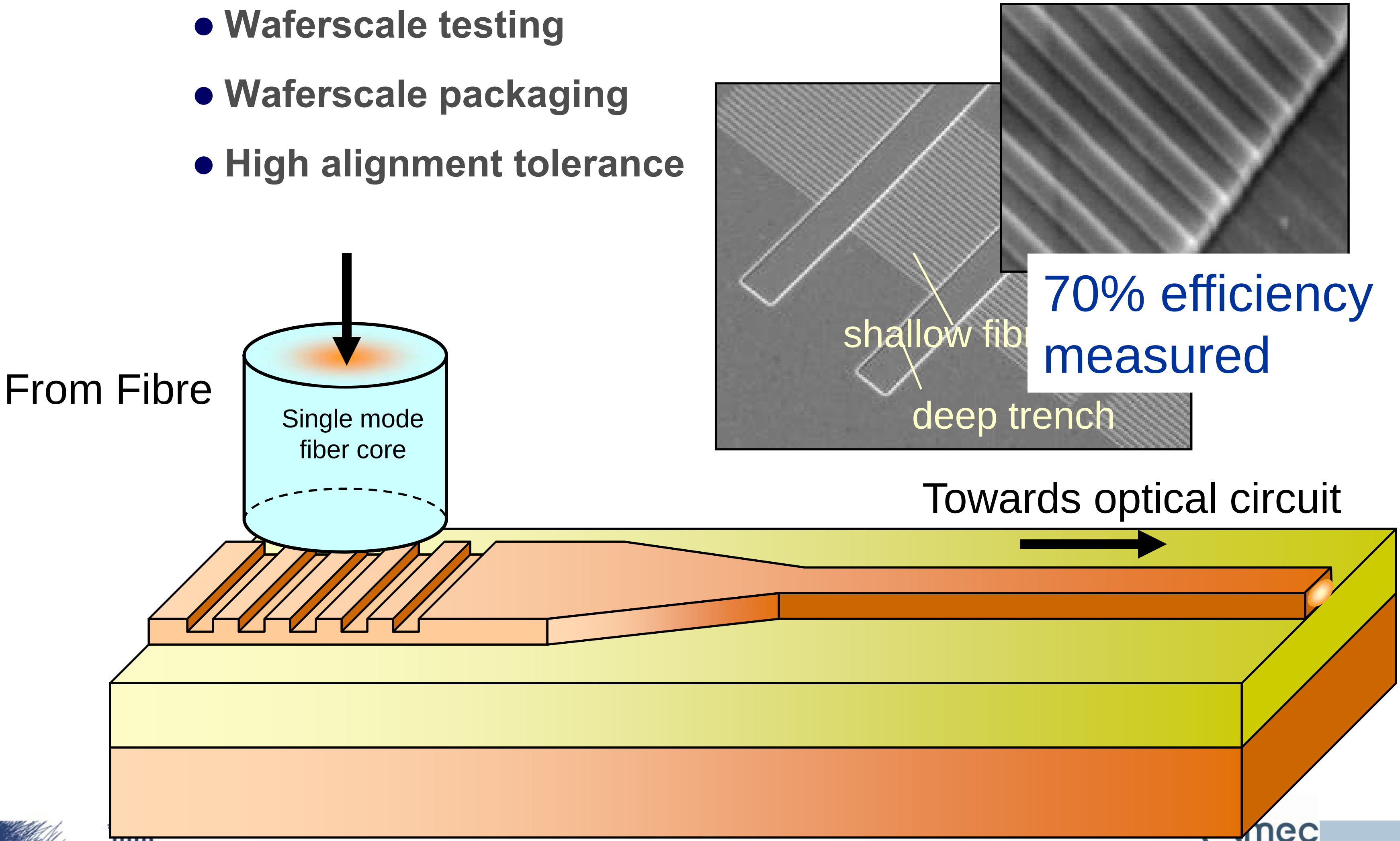
Important:

- Low loss coupling
- Large bandwidth
- Coupling tolerance
- Fabrication
  - Limited extra processing
  - Tolerant to fabrication
- Low reflection
- Polarization ?

Coupling to fiber – Grating coupler

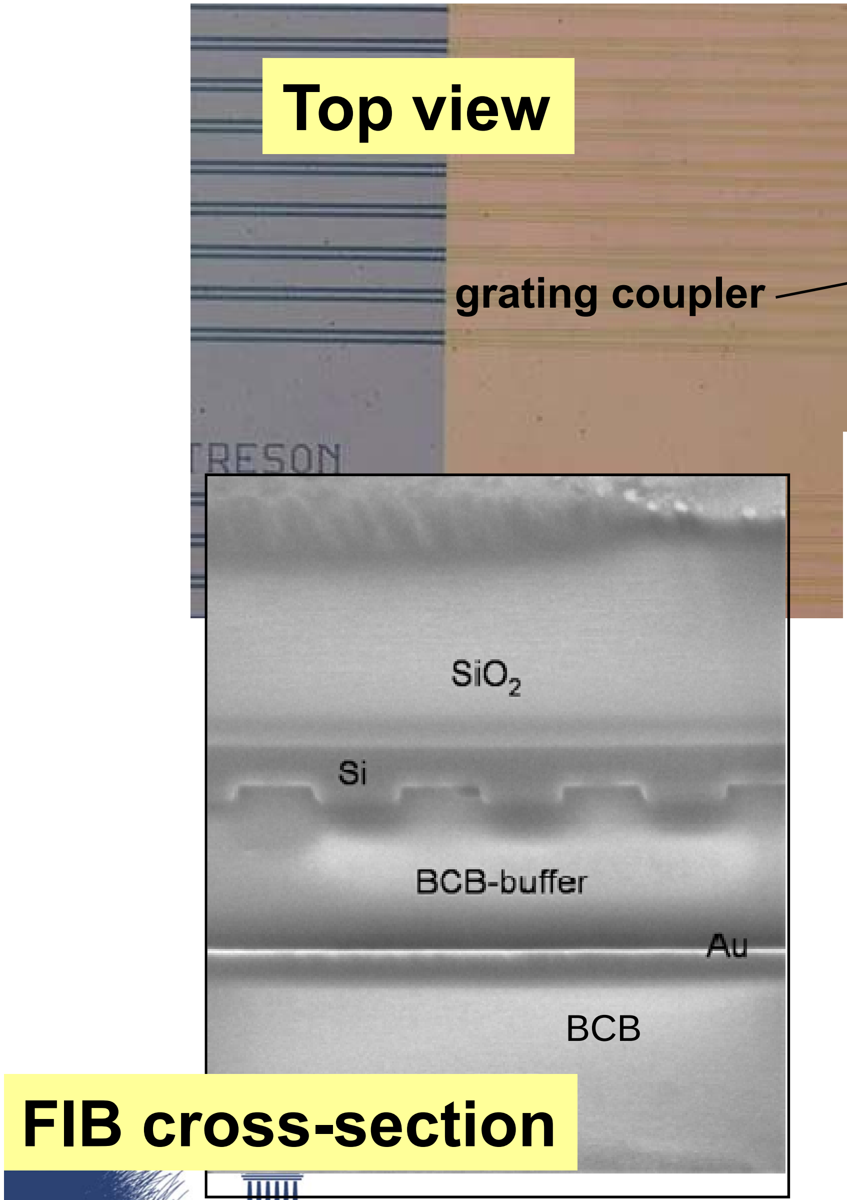
Alternative: Grating couplers

- **Waferscale testing**
- **Waferscale packaging**
- **High alignment tolerance**



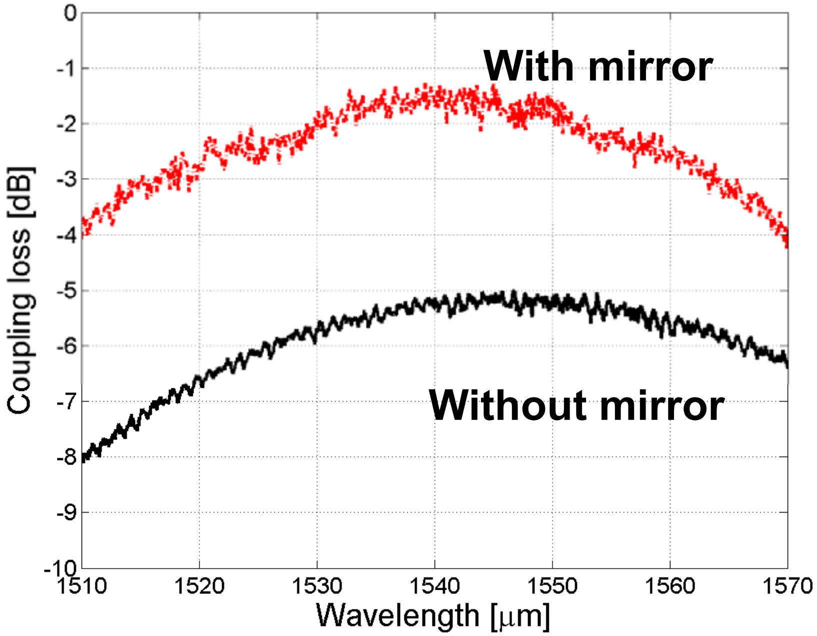
70% efficiency measured

Increase effieciency ?



Improving performance

- Add bottom mirror
- Apodize
- “Other”

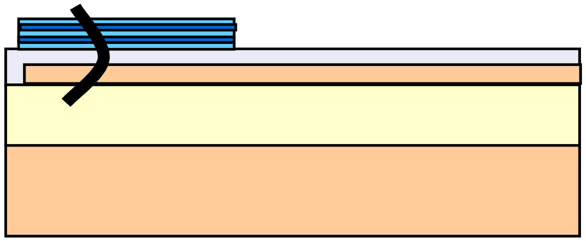


1dB bandwidth > 40nm

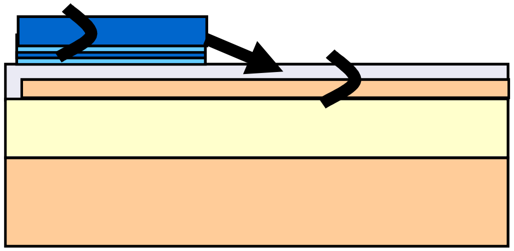
Main Challenges

1. Coupling of light between III-V and Silicon

- **Option 1: evanescent**
  - Guiding in silicon
  - Requires thin bonding layer
  - Requires III-V thinner than <250nm



- **Option 2: other (adiabatic, grating coupler …)**
  - Guiding in III-V
  - Thicker III-V layer
  - Sometimes thicker bonding



Main Challenges

1. Coupling of light between III-V and Silicon

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  - Requires III-V thinner than <250nm
- Opt ting coupler ...)
  - Guiding in III-V
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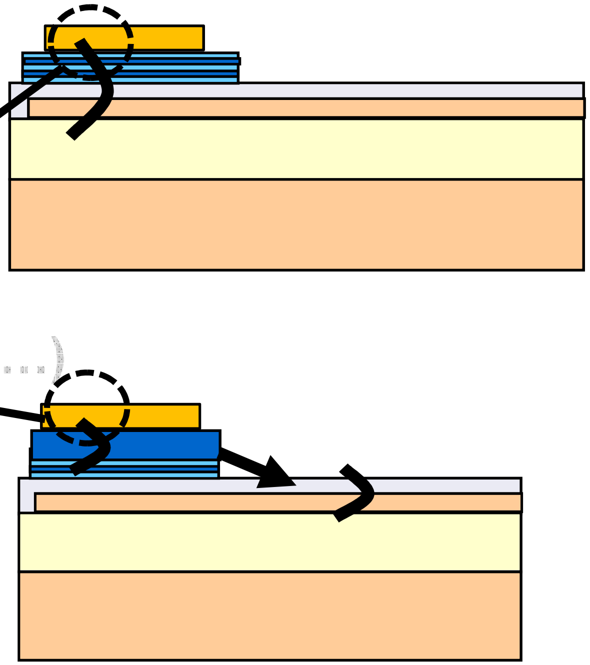
  - Sometimes thicker bonding

Loss at metal contact



2. Electrical injection

- Metal contact on membrane devices without inducing additional loss

Integrated Devices: laser diode

Integrated laser diodes

- Fabry-Perot laser cavity by etching InP/InGaAsP laser facets
- Inverted adiabatic taper coupling approach